LAB 2

GROUP MEMBERS : MUHAMMAD SYAZWAN BIN SAHDAN
MEGAT IRFAN ZACKRY BIN ISMAIL
SECTION : 08

Part 1

1. **Y = AB + BC + AC**

Y = AB(C + C') + BC(A + A') + AC(B + B')

Y = ABC + ABC' + ABC + A'BC + ABC + AB'C

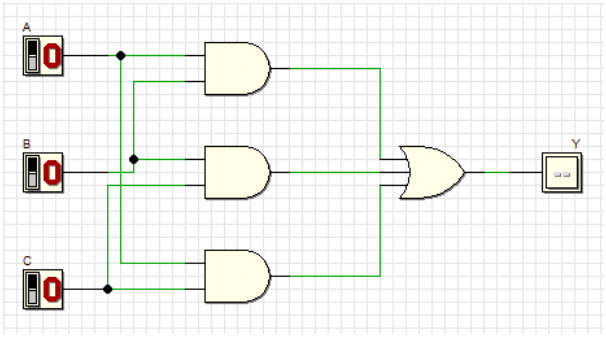
Y = ABC + ABC' + A'BC + AB'C

2.

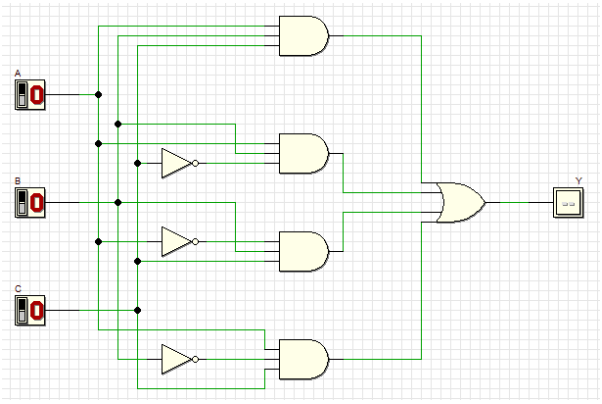
INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3.

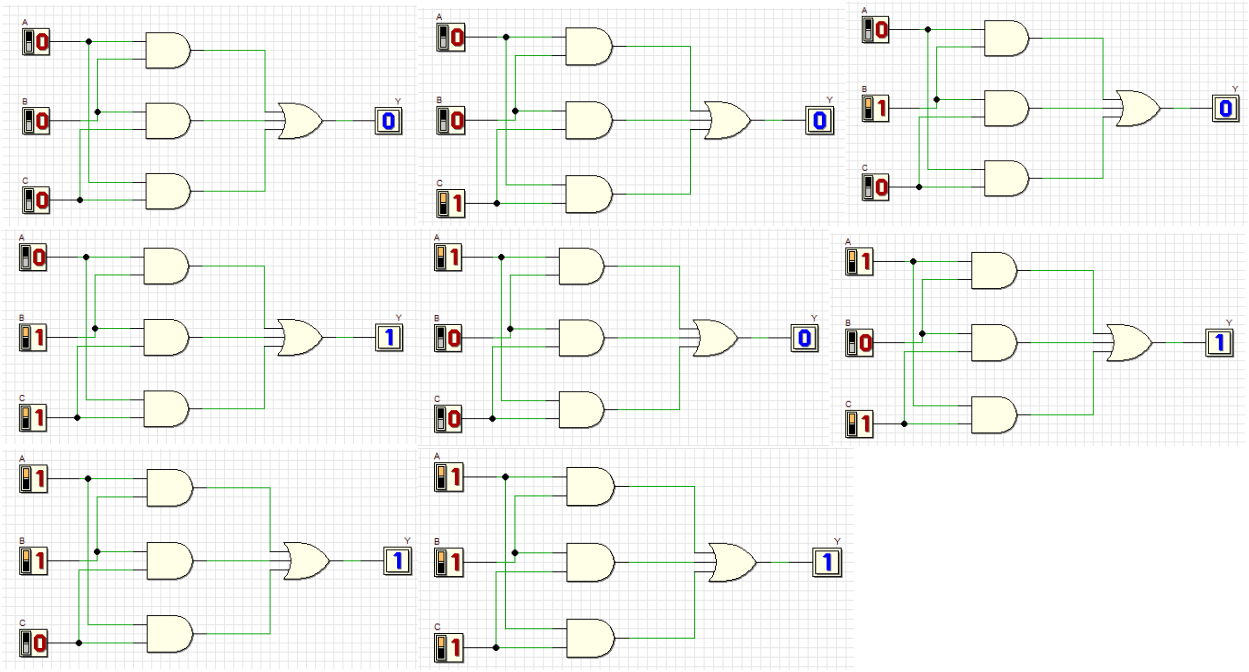
a) **Circuit (i)**



b) **Circuit (ii)**

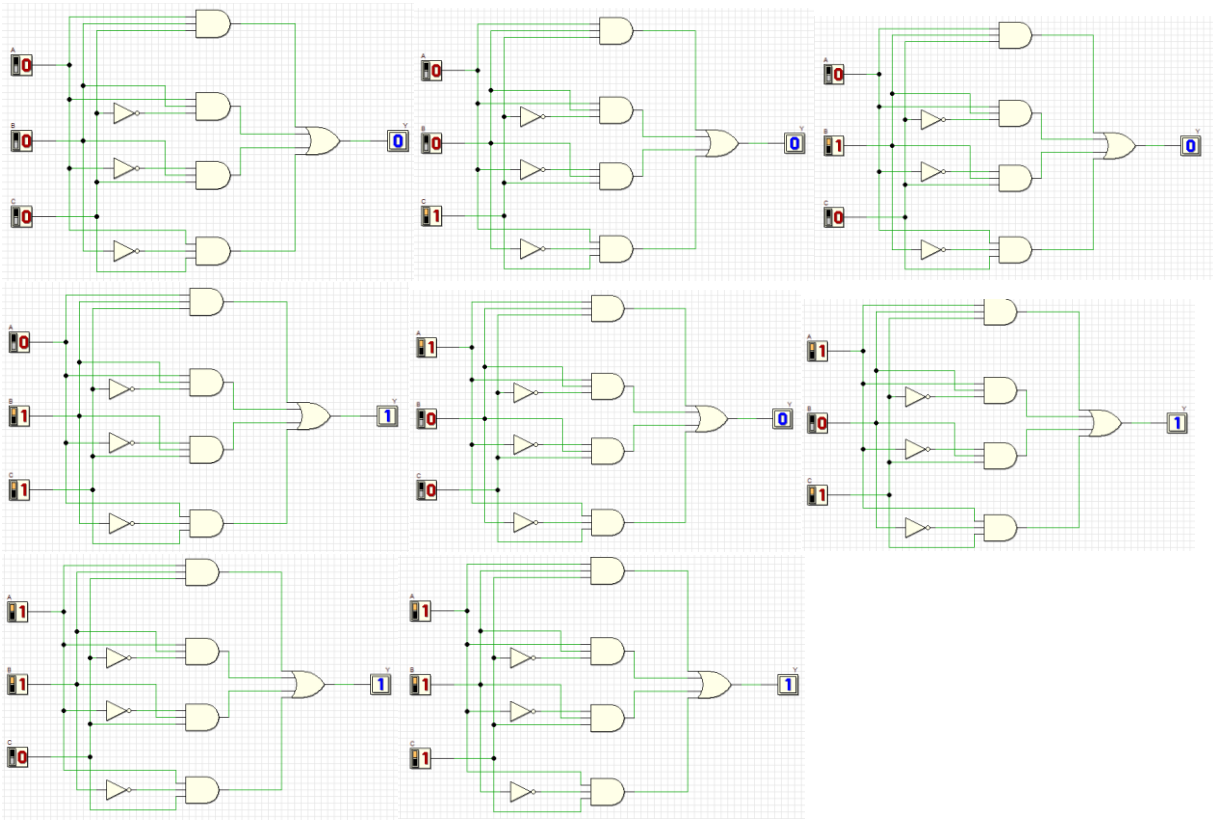


4.



Circuit (i)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



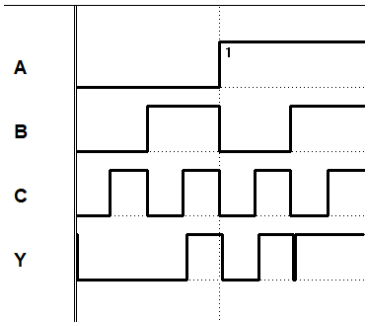
Circuit (ii)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

It concludes that the output of the truth table from the non-standard form Boolean expression is the same as the output of the truth table from the standard from Boolean expression. Standardization of the Boolean expression will not affect the output.

5.



Part 2

1. **Truth Table 1**

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	X	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2.

CD / AB	00	01	11	10
00	0	1	x	0
01	0	x	0	X
11	x	0	0	0
10	0	x	0	X

E1=A'B'D

CD / AB	00	01	11	10
00	1	0	x	1
01	1	x	0	X
11	X	0	0	0
10	0	X	0	X

E2=A'D'

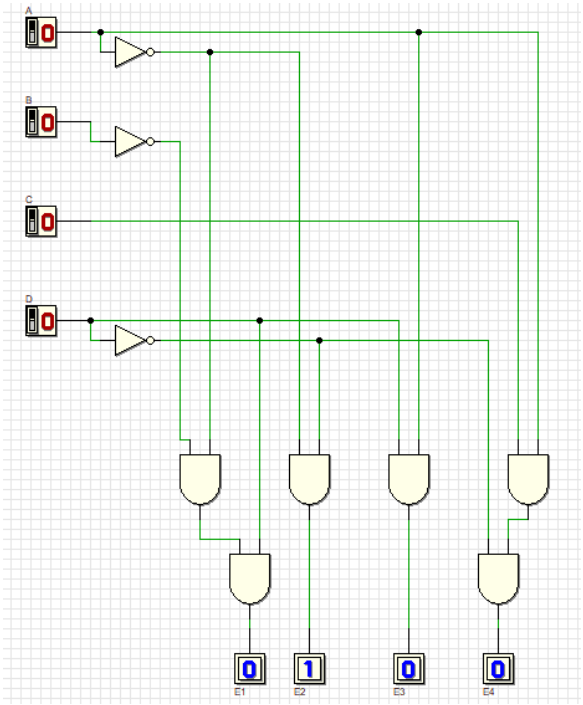
CD / AB	00	01	11	10
00	0	0	x	0
01	0	x	0	0
11	x	1	1	0
10	0	x	1	X

E3=AD

CD / AB	00	01	11	10
00	0	0	x	0
01	0	x	0	1
11	x	0	0	1
10	0	x	0	x

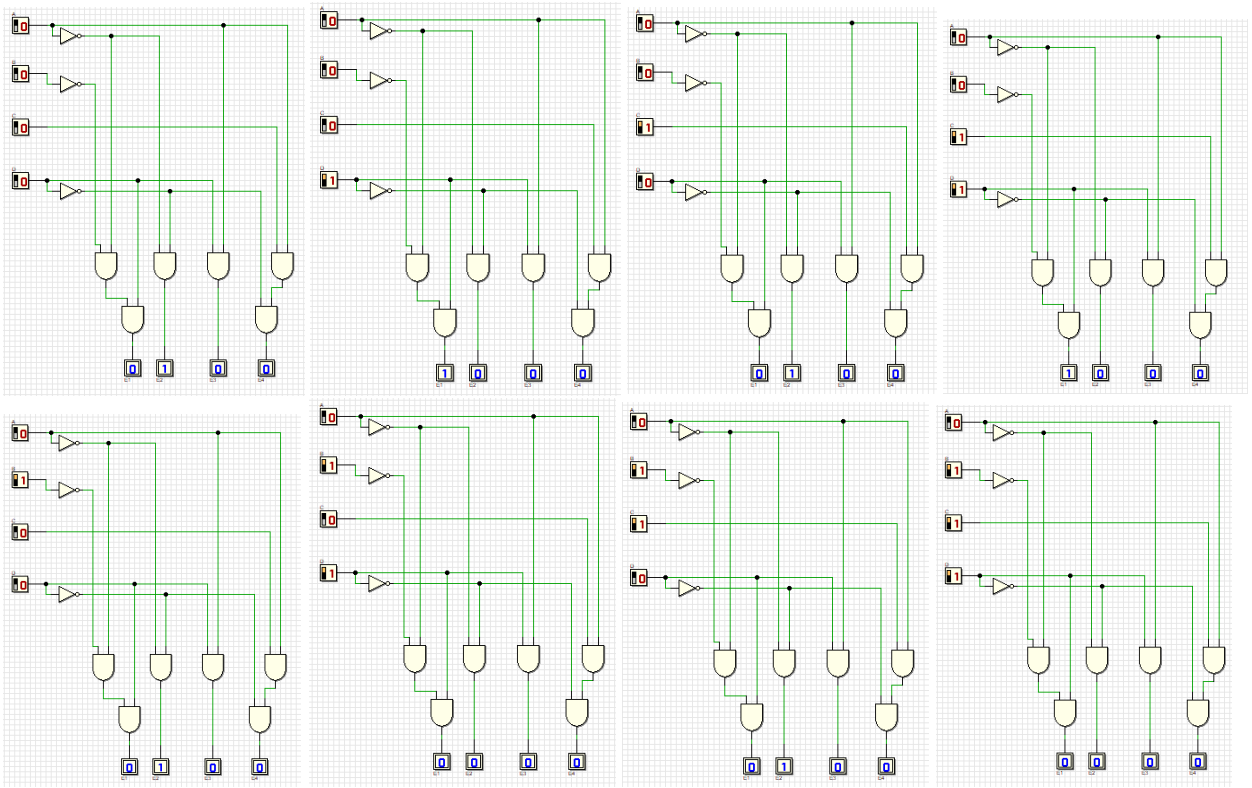
E4=ACD'

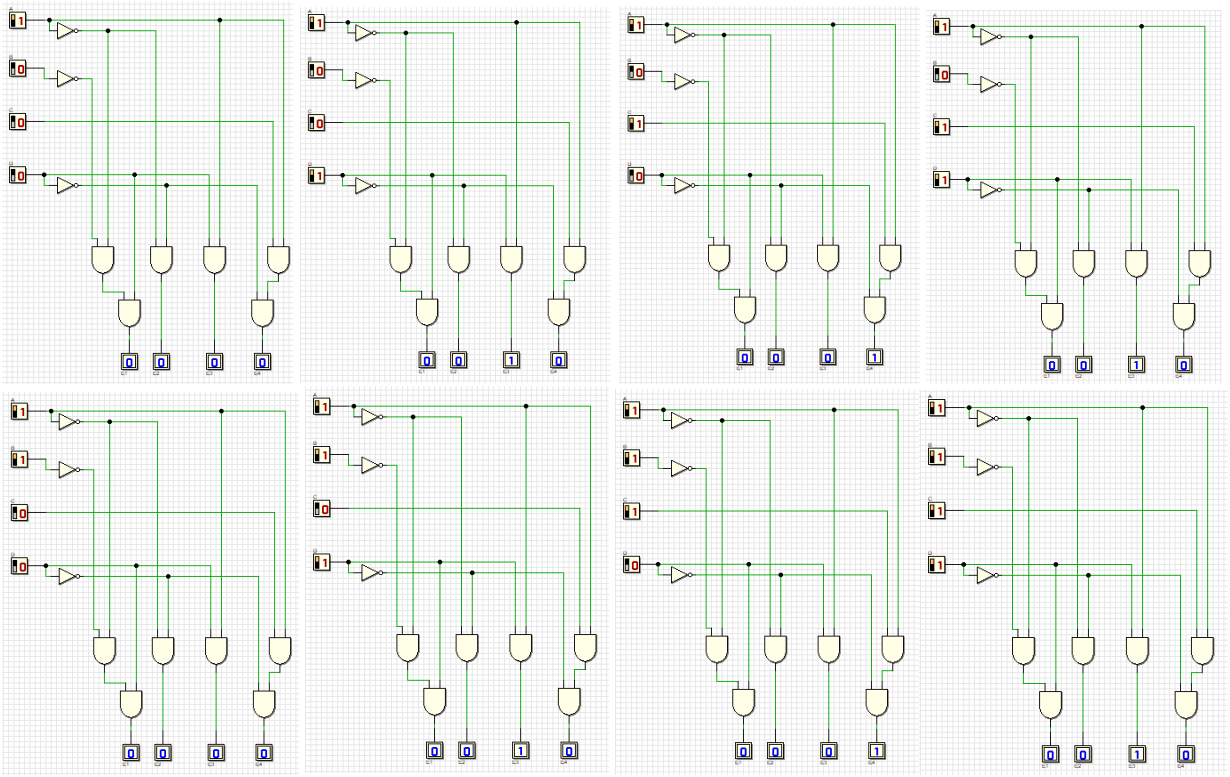
3.



4.

a)



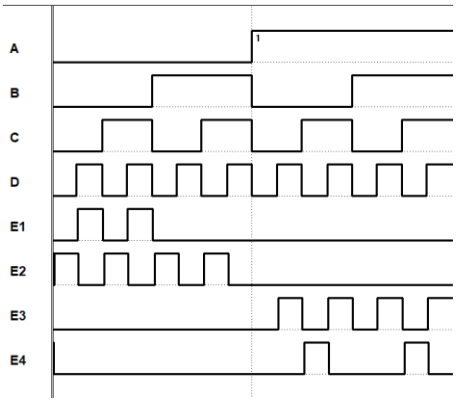


Truth Table 2

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Conclusion : All the outputs in Truth Table 1 and Truth Table 2 are the same except for the don't care, X output in Truth Table 1 can be either 1 or 0 after Truth Table 2 has been formed.

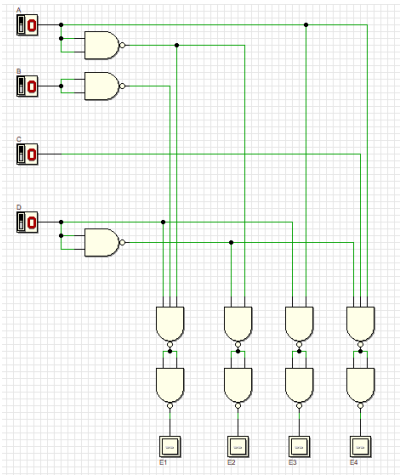
b) Timing Diagram



Explain some analysis values based on your timing diagram

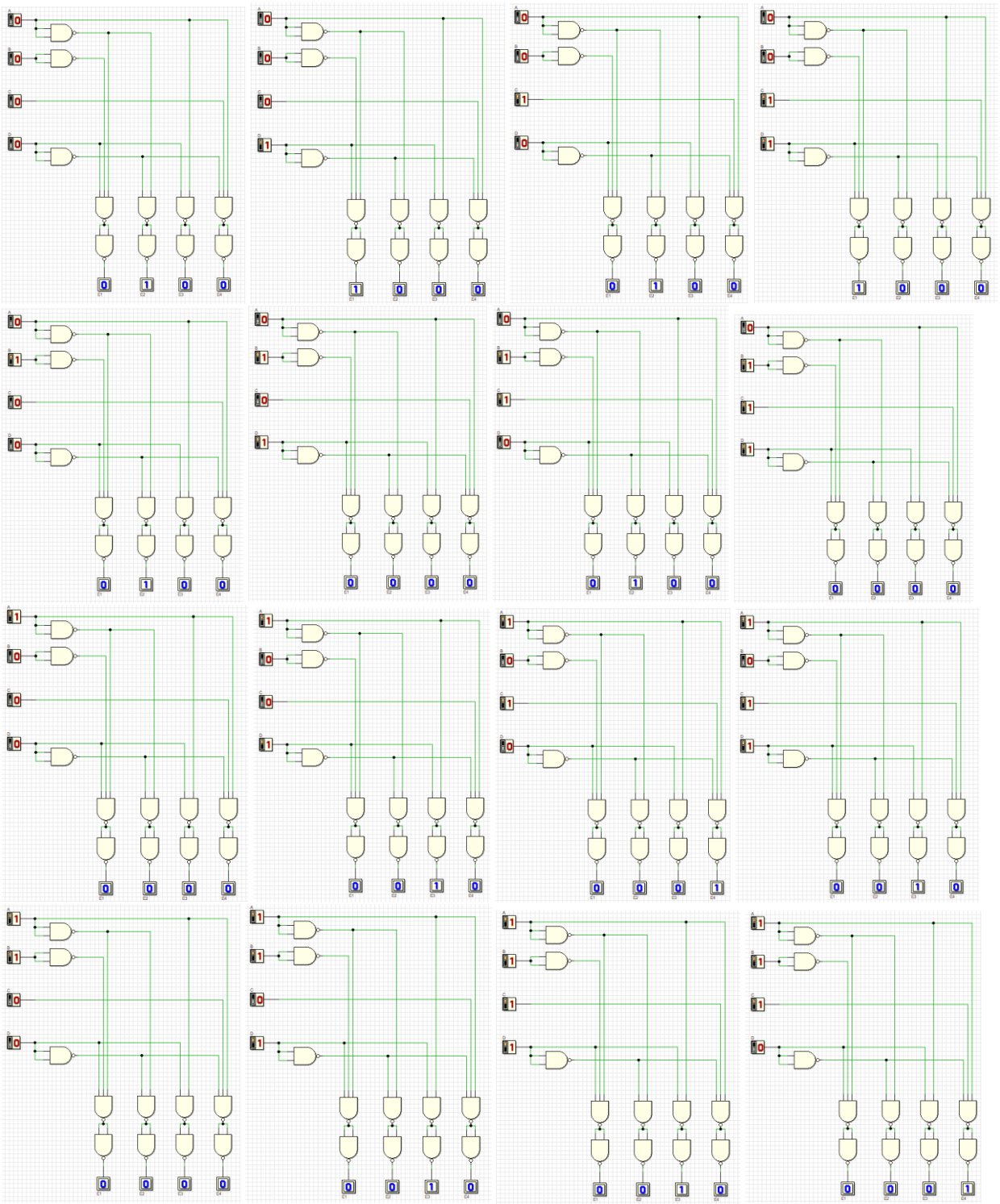
We can see that this the output of this timing diagram which is E1,E2,E3 and E4 follows the output of the truth table of the circuit. It proves that the circuit is functioning well and there are no errors detected during the execution of the circuit.

5.



6.

a)

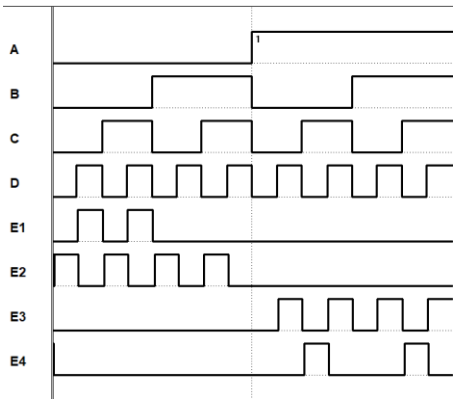


Truth Table 3

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Conclusion : The output results in Truth Table 3 is the same as Truth Table 2. Converting the types of gates used in a circuit will not affects the output results.

b) Timing Diagram



Explain some analysis values based on your timing diagram

We can see that the timing diagram produced by NAND only circuit is similar to the timing diagram produced by the basic gates circuit. It concludes that the replacement of the same wiring structure from using basic gates to NAND only gates does not affect the output of the circuit.