Lab 1

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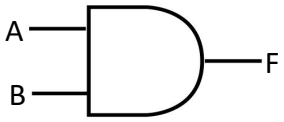
Section : 08

Part D : Preliminary work

1.

AND

Symbol :-



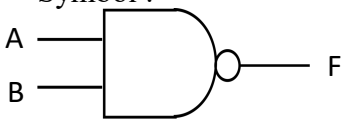
IC Number : 7408

Truth Table 1

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND

Symbol :-



IC Number : 7400

Truth Table 2

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

2.

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

3. C = A . B’

D = A’ . B

F = C + D

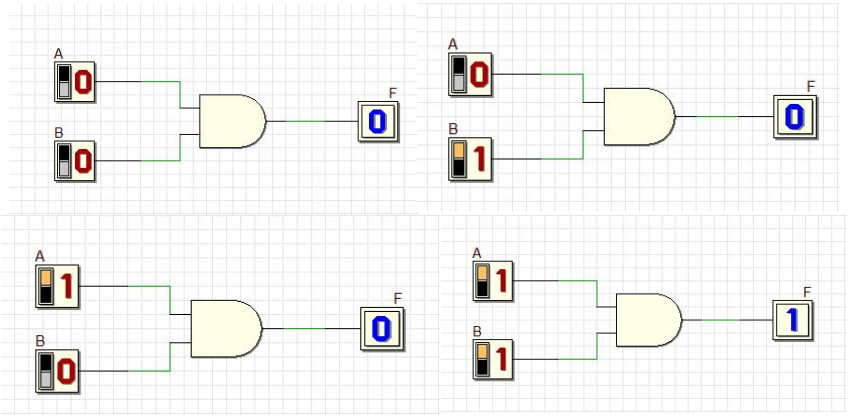
4.

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

Part E : Laboratory Work

Part 1

1.

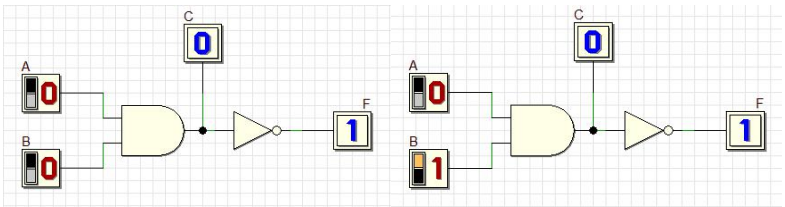


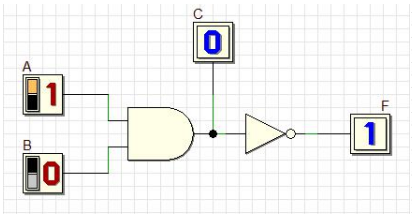
2. Truth Table 5

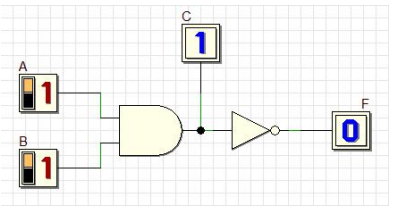
Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Part 2

3.







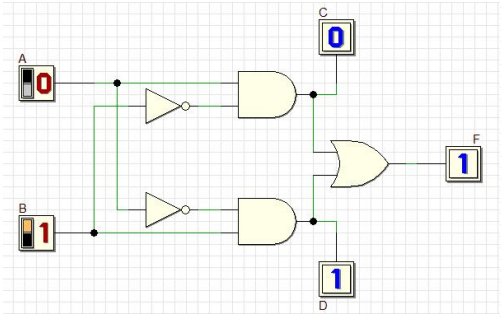
4. Truth Table 6

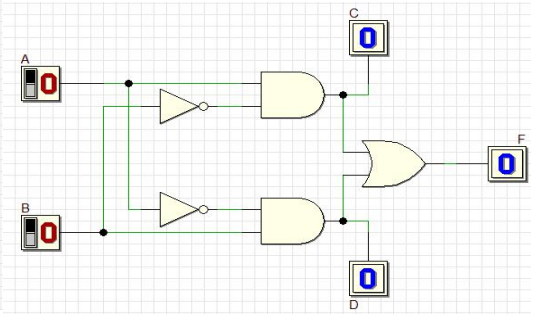
A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

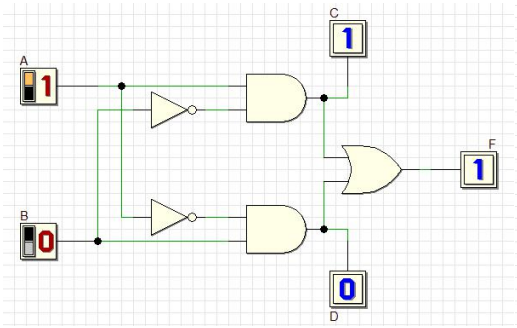
5. It is a NAND gate.

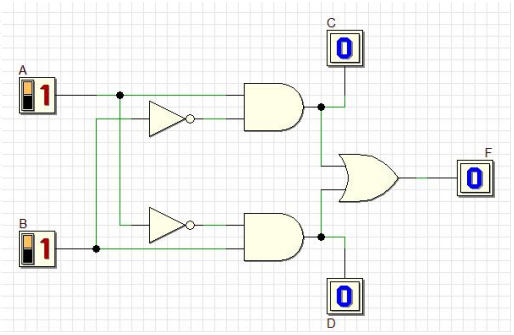
Part 3

6.









7. Truth Table 7

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

8. XOR gate