

Lab 1

Group Members : Muhammad Syazwan bin Sahdan
Megat Irfan Zackry bin Ismail

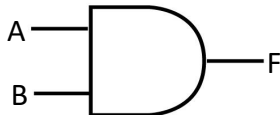
Section : 08

Part D : Preliminary work

1.

AND

Symbol :-



The diagram shows a standard D-shaped AND gate. Two input lines, labeled 'A' and 'B', enter the flat left side of the gate. A single output line, labeled 'F', exits from the curved right side of the gate.

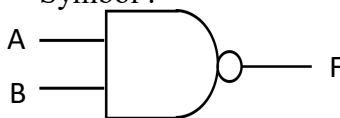
IC Number : 7408

Truth Table 1

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND

Symbol :-



The diagram shows a NAND gate, which is an AND gate with a small circle (bubble) at its output. Two input lines, labeled 'A' and 'B', enter the flat left side of the gate. A single output line, labeled 'F', exits from the curved right side of the gate, passing through the bubble.

IC Number : 7400

Truth Table 2

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

2.

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

3. $C = A \cdot B'$

$D = A' \cdot B$

$F = C + D$

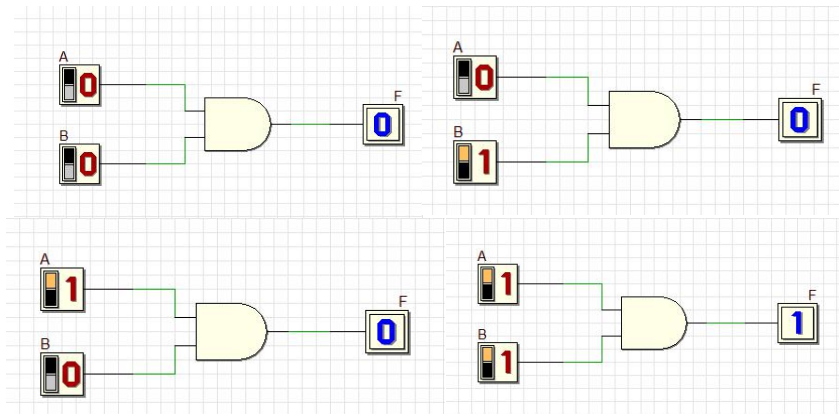
4.

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

Part E : Laboratory Work

Part 1

1.

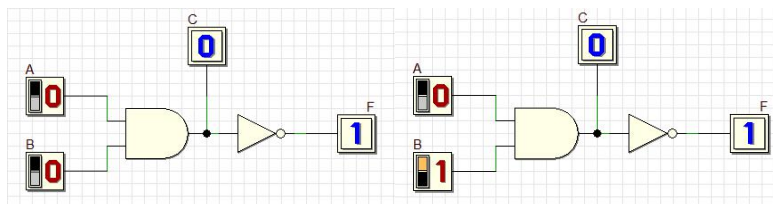


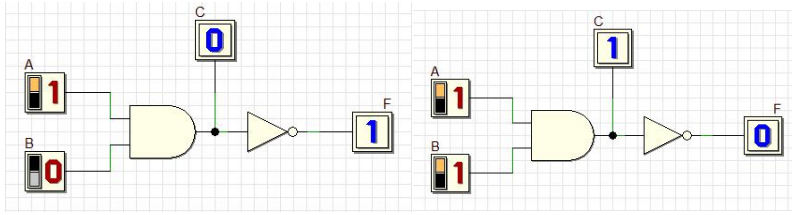
2. Truth Table 5

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Part 2

3.





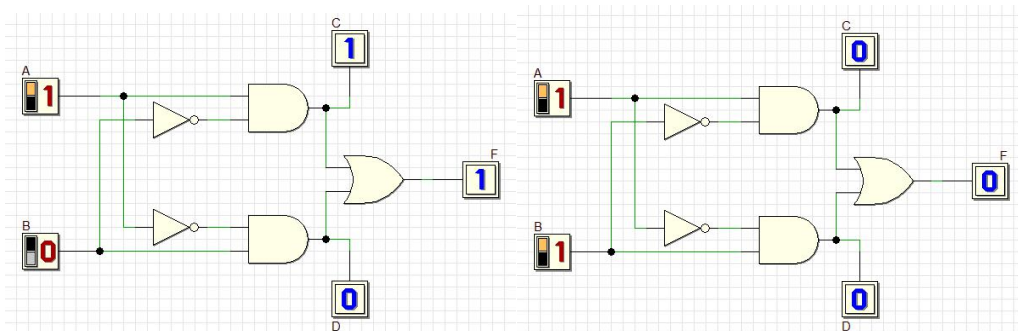
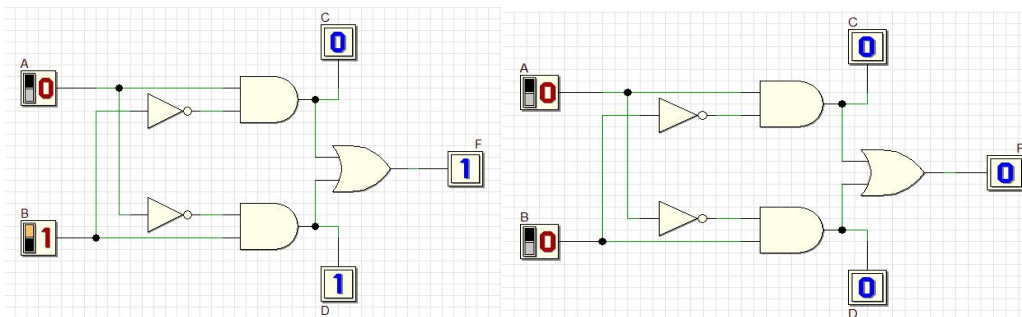
4. Truth Table 6

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

5. It is a NAND gate.

Part 3

6.



7. Truth Table 7

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

8. XOR gate