

SUBJECT : SECR1013 DIGITAL LOGIC

SESSION/SEM : 01/1

LAB 3 : **SYNCHRONOUS DIGITAL COUNTER**

NAME : KESHINIY A/P MOGAN
ROSHINI A/P THAVAN NAIR

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D

1)

Desired Result	$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	J	K	CLK	Q
Set initial value $Q = 1$	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	$\downarrow$	1
Output Q become 0, no change in asynchronous input	1	1	0	1	$\downarrow$	0
Output Q is not the previous Q	1	1	1	1	$\downarrow$	1
RESET Q	1	1	0	1	$\downarrow$	0
SET Q	1	1	0	0	$\downarrow$	1

2)

a) Which state that JK flip-flop has, but not on SR flip-flop.

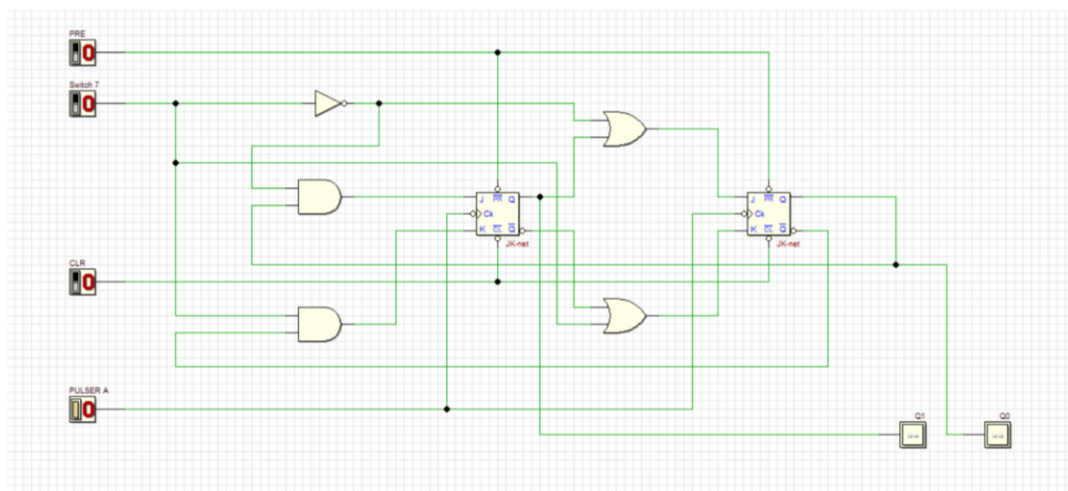
=JK flip-flop has toggle state but not on SR flip-flop.

b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negativeedge triggered flip flop.

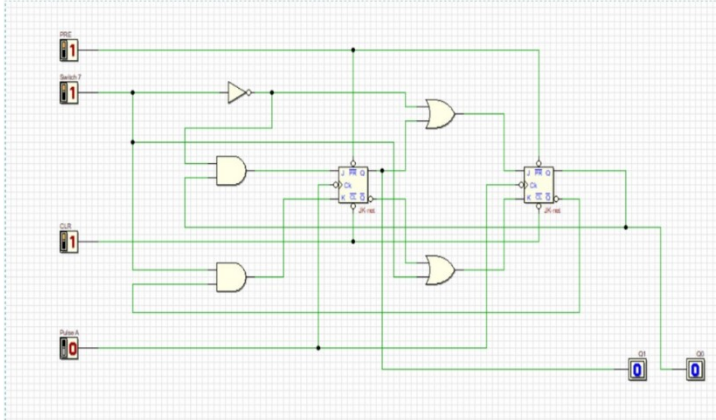
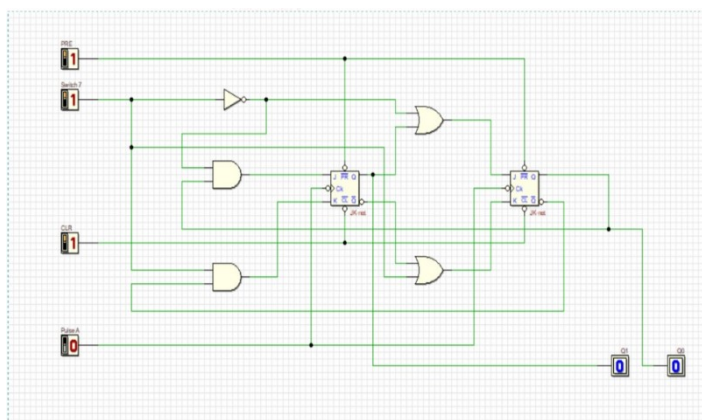
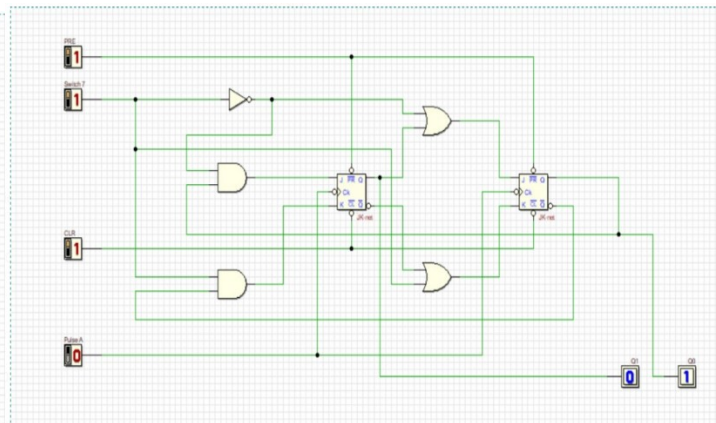
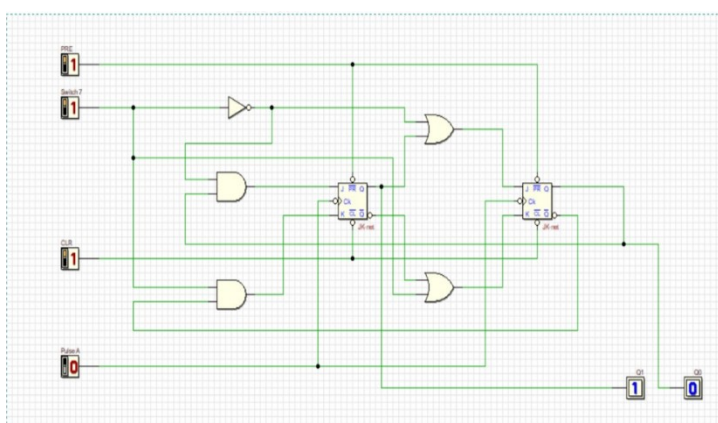
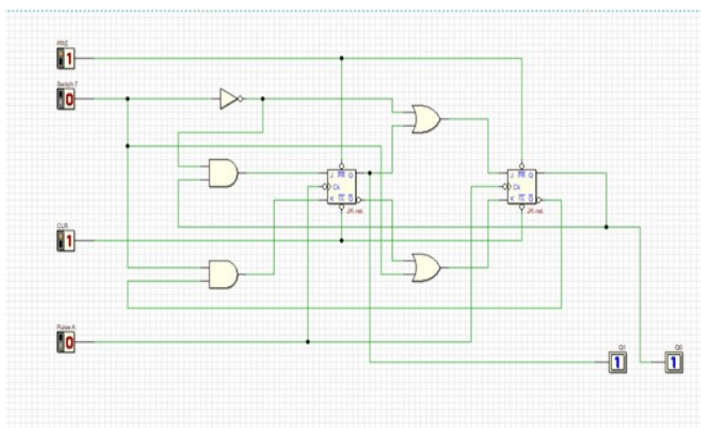
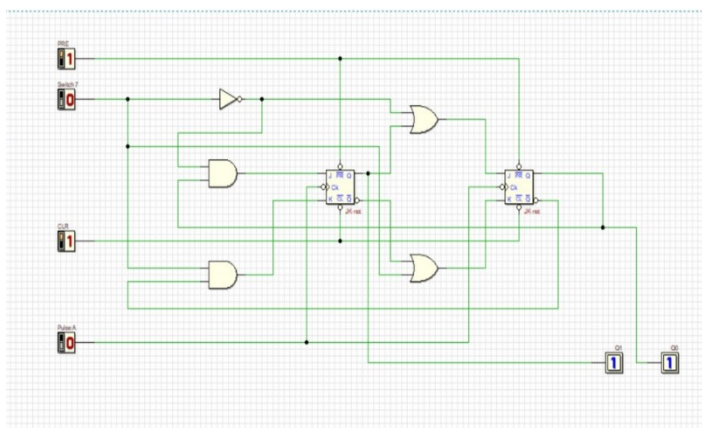
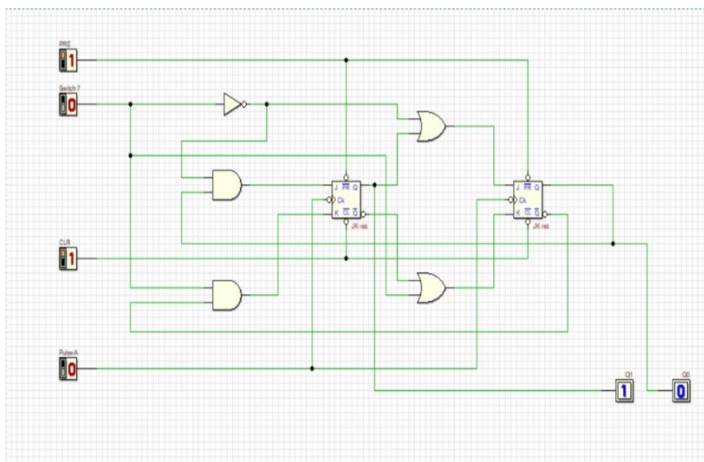
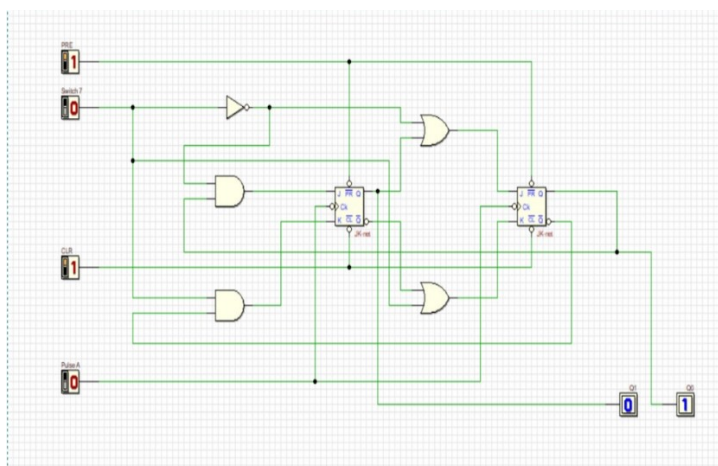
= Negative-edge triggered flip flop.

E

1)



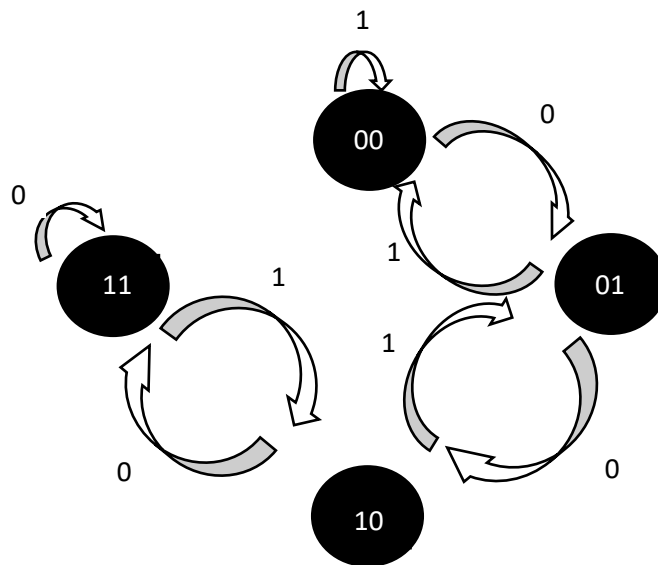
2)



3)

SWITCH 7	PRESENT STATE		NEXT STATE	
X	Q1 LED1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4)



5)

By referring to the Next-State in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?

=It uses clock inputs to synchronize the circuit operation and all clock are from the same source.

b) How many states are available for the counter and what are they?

=Two states. Present state and Next state

c) What is the function of Switch 7 (X) in the circuit?

=To control the count direction.

d) What is the function of Switch 0 and Switch 1 in the circuit?

=Switch 0 act as Preset and Switch 1 act as Clear

e) Is the counter a saturated counter or recycle counter?

=Recycle counter

6)

Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3

INPUT X	PRESENT STATE		NEXT STATE		D FF TRANSITION	
	Q1	Q0	Q1 +	Q0 +	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

b) Get the optimized Boolean expression.

For D1

$$D_1 = \bar{X} Q_0 + \bar{X} Q_1 + Q_1 Q_0$$

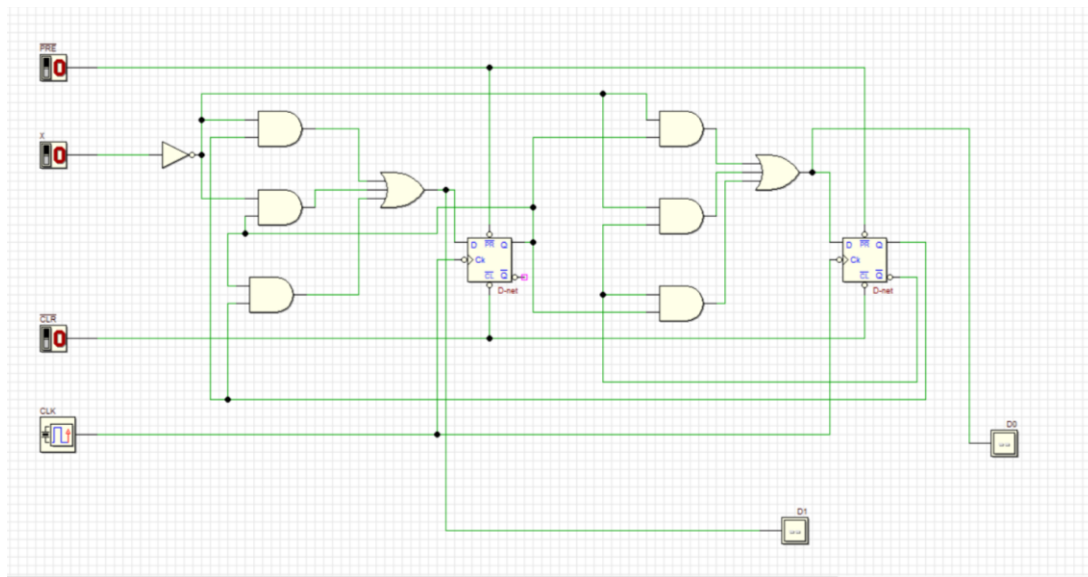
$$D_1 = \bar{X} [Q_0 + Q_1] + Q_1 Q_0$$

For D0

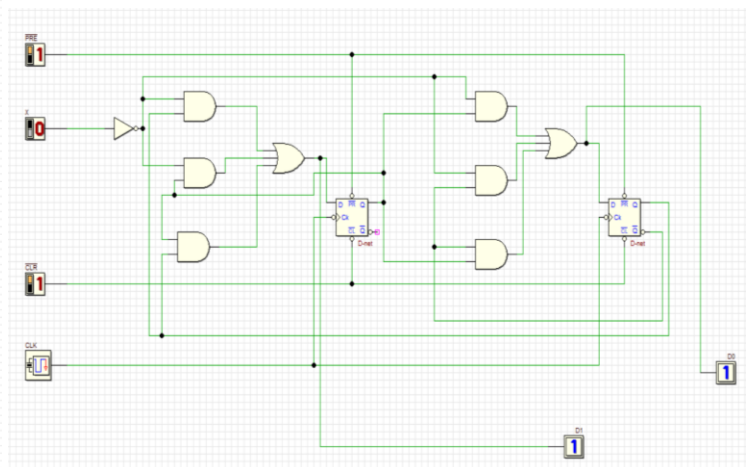
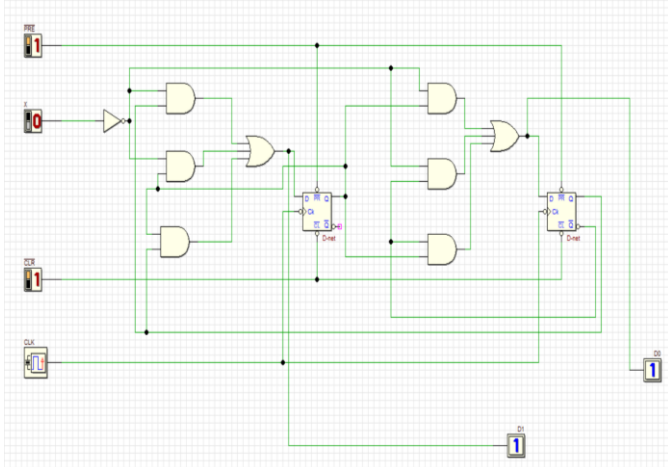
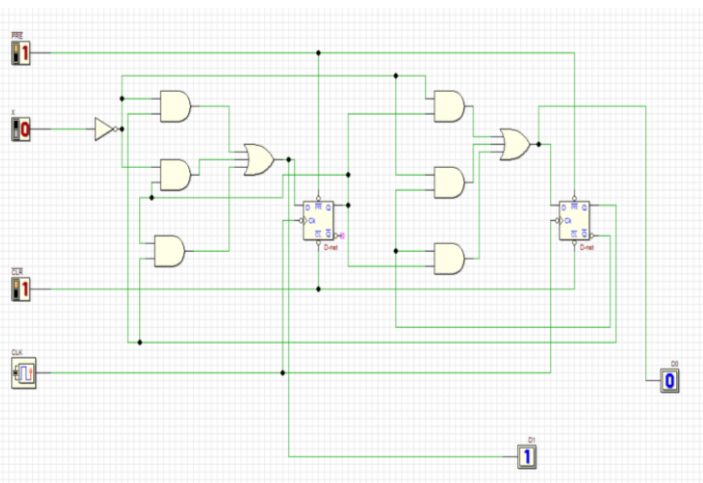
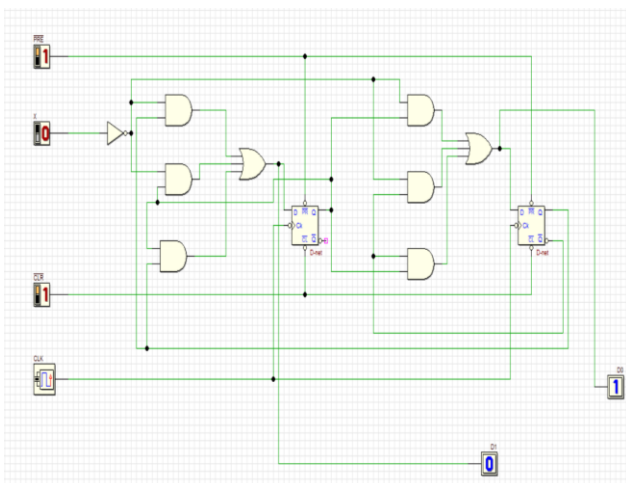
$$D_0 = \bar{X} Q_1 + X \bar{Q}_0 + Q_1 \bar{Q}_0$$

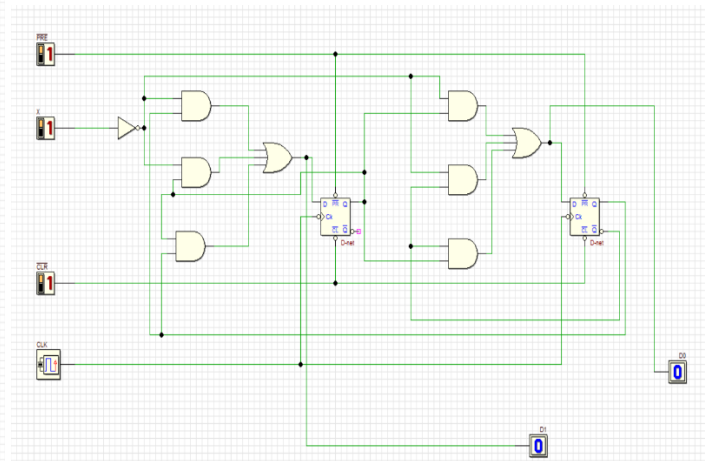
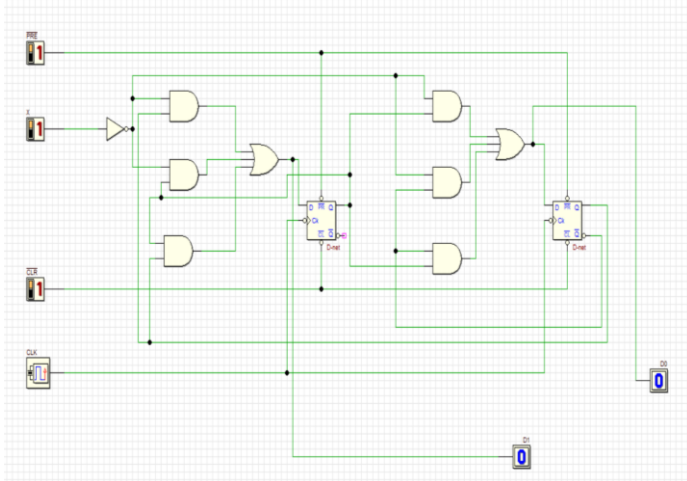
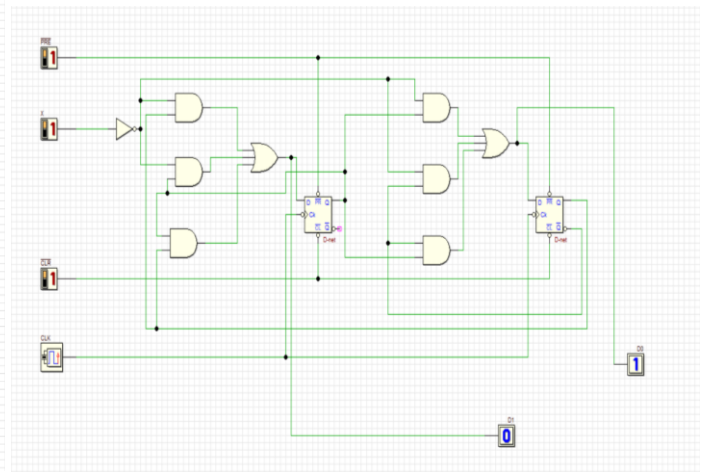
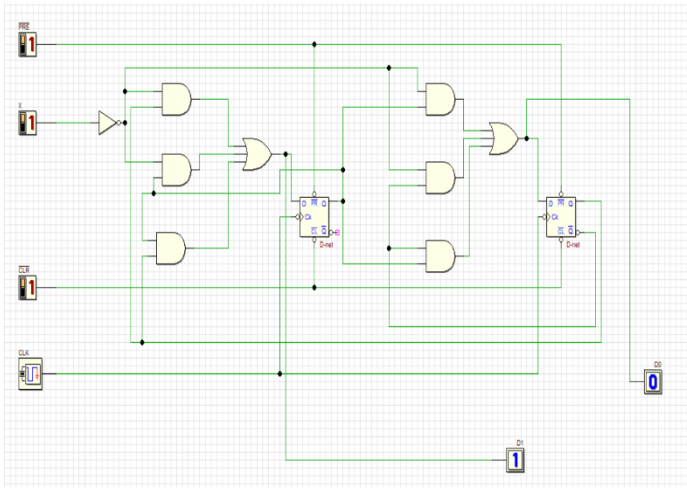
$$D_0 = \bar{X} [\bar{Q}_0 + Q_1] + Q_1 \bar{Q}_0$$

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 3 is correct.



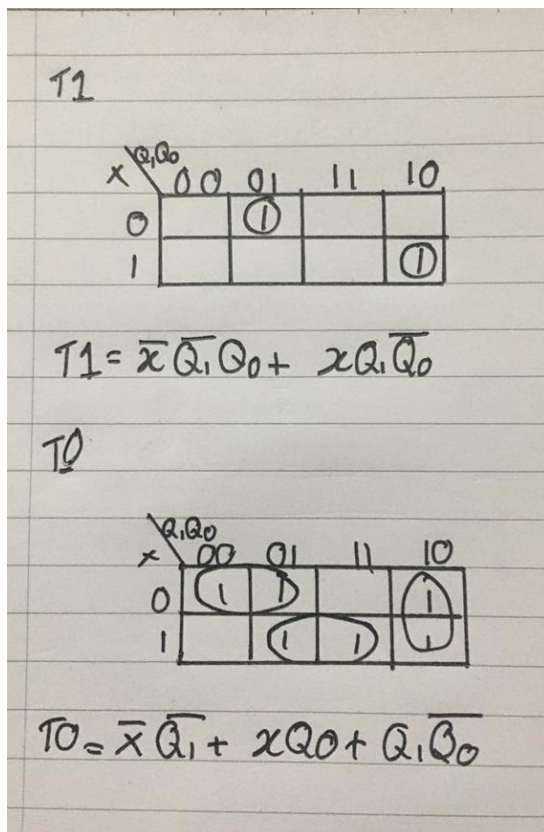


7) Repeat steps in Q(6) using T flip-flop.

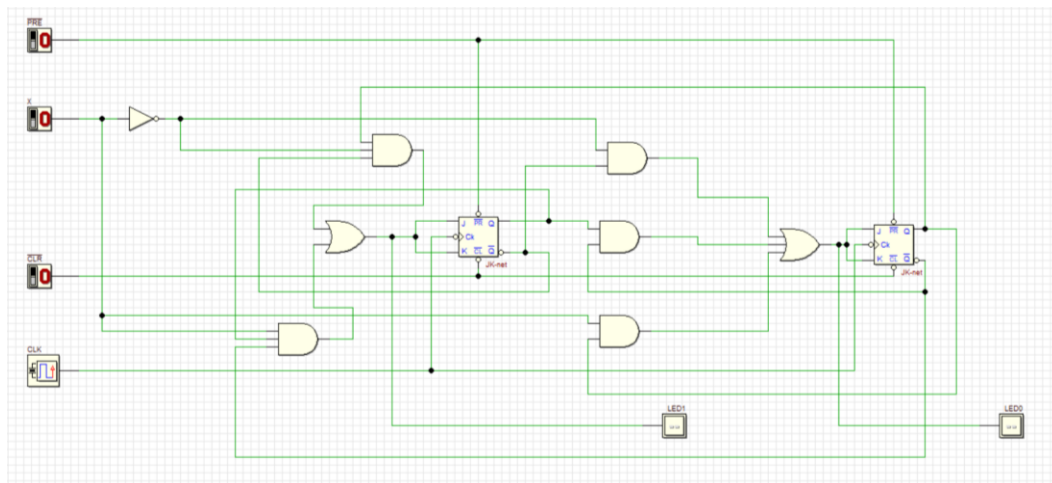
a) Built the next state and transition table using the header in Table 3

INPUT X	PRESENT STATE		NEXT STATE		T FF TRANSITION	
	Q1	Q0	Q1 +	Q0 +	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

b) Get the optimized Boolean expression.



c) Draw the complete final circuit design in Deeds.



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