School of Computing
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SUBJECT	:	SECR1013 DIGITAL LOGIC
SESSION/SEM	:	2020/2021 / SEM1
LAB 3	**:**	**SYNCHRONOUS DIGITAL COUNTER**
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DATE	:	28/1/2021

D. Preliminary Works

1) Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	**J**	**K**	**CLK**	**Q**
Set initial value Q = 1	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	⇓	1
Output Q become 0, no change in asynchronous input	1	1	1	1	⇓	0
Output Q is not the previous Q	1	1	1	1	⇓	1
RESET Q	1	1	0	1	⇓	0
SET Q	1	1	1	0	⇓	1

2) Answer all questions.

a) Which state that JK flip-flop has, but not on SR flip-flop.

In JK flip-flop when both input is equal to 1, the output Q will be toggle. But on SR flip-flop when both input state is equal 1 it is an invalid state. So, we can say that JK flip-flop has a toggle state when both input is equal to 1, but SR flip-flop don't have because it is an invalid state.

b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

Negative-edge triggered flip-flop because the synchronous input change when meet the negative clock edge.

E. Lab Activities

1) You are given a counter circuit as shown in Figure 4.

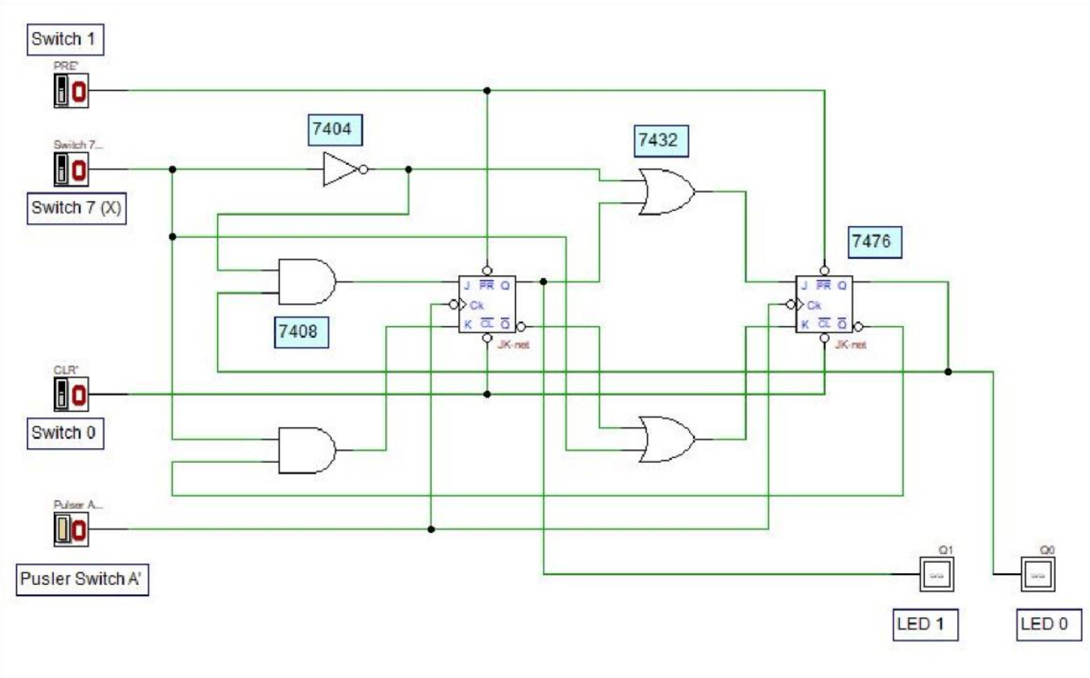
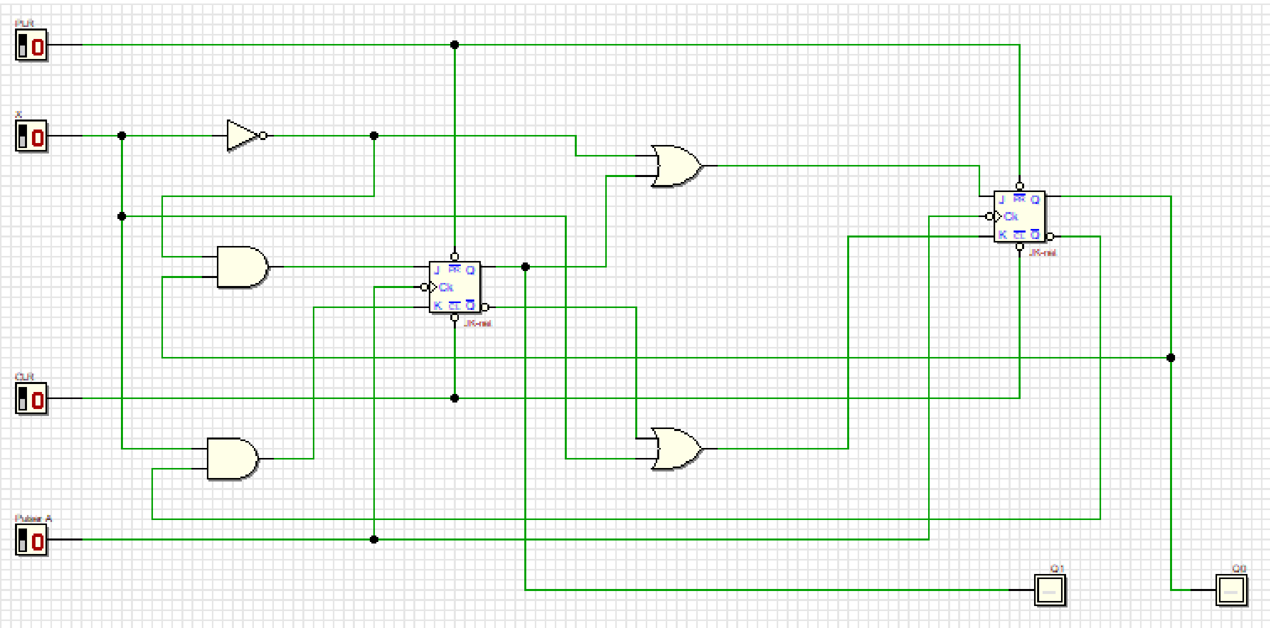


Figure 4: A Synchronous Counter Circuit

2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).

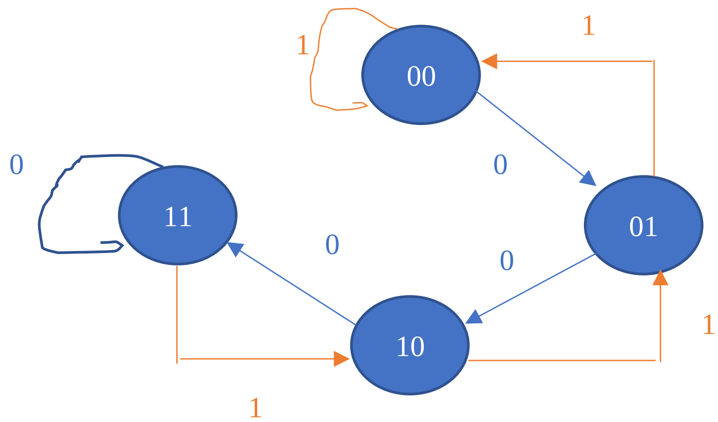


3) Investigate the behaviour of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the *NextState* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state.
(0=LOW, 1=HIGH)

Table 2

Switch 7	**Present State**		**Next State**	
X	**Q1** **LED 1**	**Q0** **LED 0**	**Q1** **LED 1**	**Q0** **LED 0**
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?

The state of PLE' and CLR'. When the state of PLE' and CLR' is equal to 1 then the counter will be a synchronous counter.

b) How many states are available for the counter and what are they?

4 states : 00, 01, 10, 11

c) What is the function of Switch 7 (X) in the circuit?\

Act as an input mode selector to select the counter to be up counter (when x =0) or down counter (when x=1)

d) What is the function of Switch 0 and Switch 1 in the circuit?

Switch 1 act as preset, PRE' to set initial value of 1 to the output.
Switch 0 act as clear, CLR' to reset the output to 0.

e) Is the counter a saturated counter or recycle counter?

Saturated counter

6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3

Table 3

Input	**Present State**		**Next State**		**D FF Transition**	
X	**Q1**	**Q0**	**Q1+**	**Q0+**	**D1**	**D0**
0	**0**	**0**	**0**	**1**	**0**	**1**
0	**0**	**1**	**1**	**0**	**1**	**0**
0	**1**	**0**	**1**	**1**	**1**	**1**
0	**1**	**1**	**1**	**1**	**1**	**1**
1	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**0**	**0**
1	**1**	**0**	**0**	**1**	**0**	**1**
1	**1**	**1**	**1**	**0**	**1**	**0**

b) Get the optimized Boolean expression.

K-map for D1:

Q1Q0

X		00	01	11	10
	0	0	1	1	1
	1	0	0	1	0

D1= X'Q0 + X'Q1 + Q1Q0

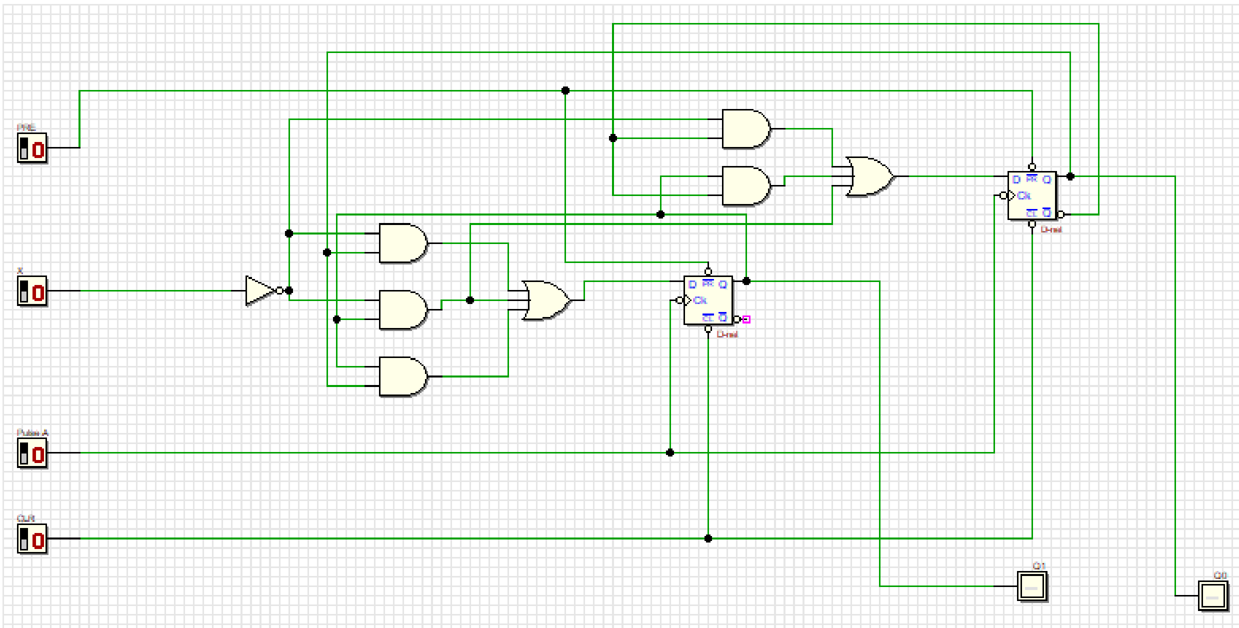
K-map for D0:

Q1Q0

X		00	01	11	10
	0	1	0	1	1
	1	0	0	0	1

D0 = X'Q0' + X'Q1 + Q1Q0'

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 3 is correct.

Table 4

Input	Present State		Next State		D FF Transition	
X	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

Since Table 3 and Table 4 show the same output, we proved that Table 3 is correct

7) Repeat steps in Q(6) using T flip-flop.

a) Built the next state and transition table.

Table 5

Input	**Present State**		**Next State**		**T FF Transition**	
X	**Q1**	**Q0**	**Q1+**	**Q0+**	**T1**	**T0**
0	**0**	**0**	**0**	**1**	**0**	**1**
0	**0**	**1**	**1**	**0**	**1**	**1**
0	**1**	**0**	**1**	**1**	**0**	**1**
0	**1**	**1**	**1**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**1**	**0**	**0**	**0**	**1**
1	**1**	**0**	**0**	**1**	**1**	**1**
1	**1**	**1**	**1**	**0**	**0**	**1**

b) Get the optimized Boolean expression.

K-map for T1:

Q1Q0

X		00	01	11	10
	0	0	1	0	0
	1	0	0	0	1

T1 = X'Q1'Q0 + XQ1Q0'

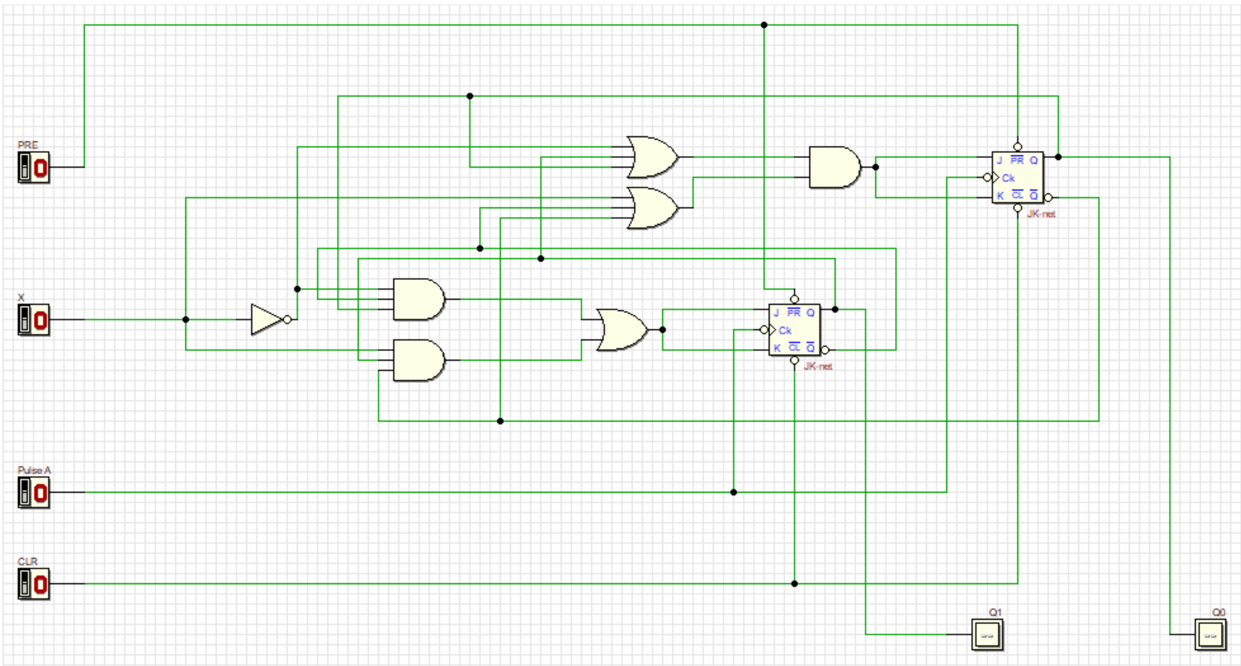
K-map for T0:

Q1Q0

X		00	01	11	10
	0	1	1	0	1
	1	0	1	1	1

T0 = (X'+Q1+Q0)(X+Q1'+Q0')

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table is correct.

Table 6

Input	Present State		Next State		T FF Transition	
X	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

Since Table 5 and Table 6 show the same output, we proved the table 5 is correct.