Department of Computer Science
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SUBJECT: SCSR1013 DIGITAL LOGIC

SESSION/SEM: 2020-21-01

LAB 2 : COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION

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REMARKS :

MARKS:

D. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

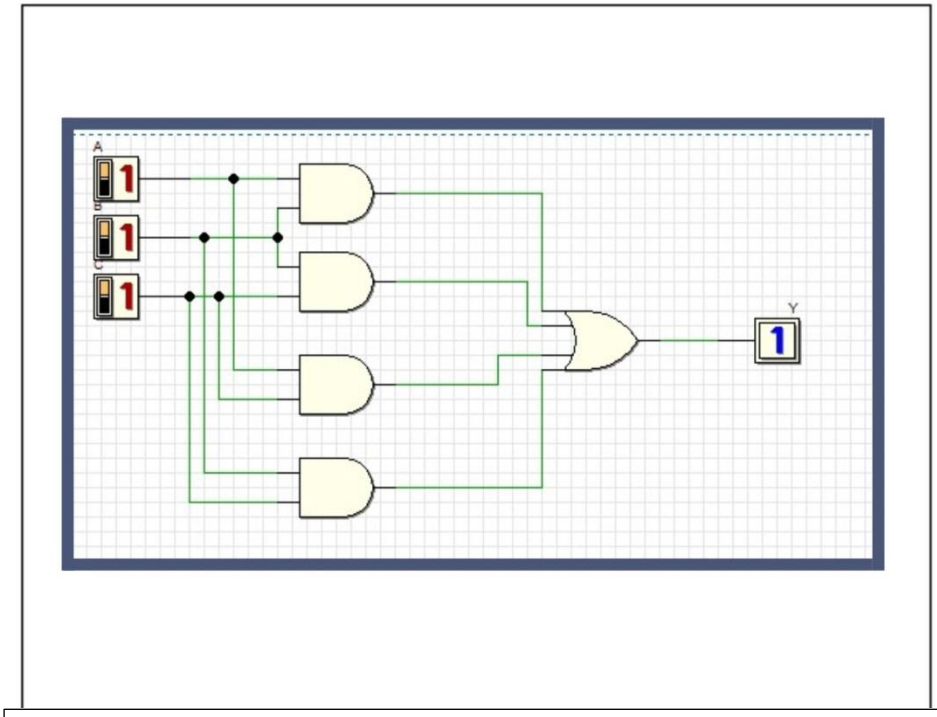
$Y=AB\ (C+\overline{C})+BC\ (A+\overline{A})+AC\ (B+\overline{B})$
$=ABC+AB\overline{C}+ABC+\overline{A}BC+ABC+A\overline{B}\ C$
$=ABC+AB\overline{C}+\overline{A}BC+A\overline{B}\ C$

2. Based on standard form expression, complete the following truth table.

INPUT			**OUTPUT**
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

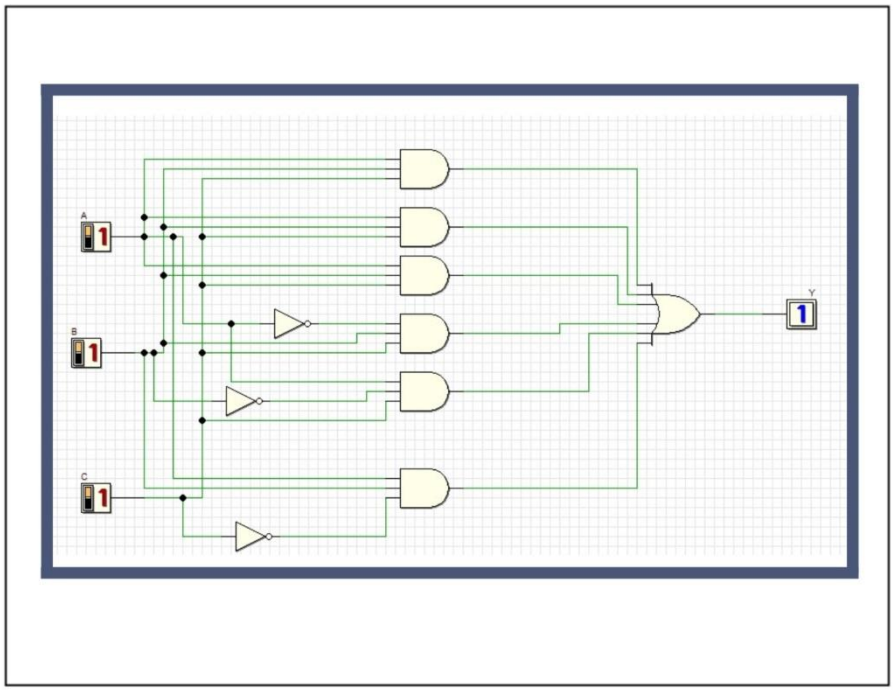
3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



Both of the truth tables are same so the equation is also same,Only non-standard form is simplified version of standard form

b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

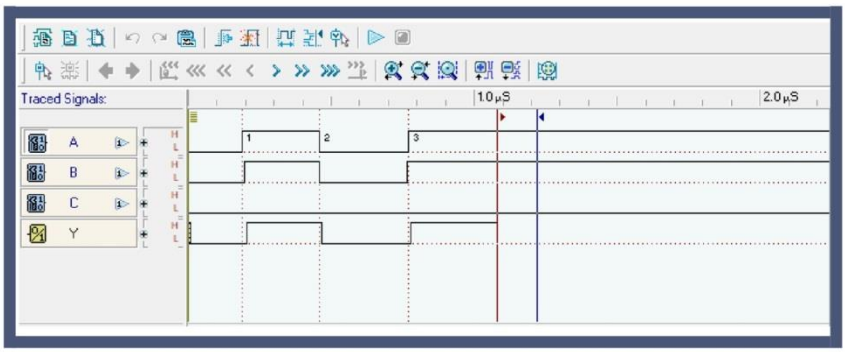
Circuit (ii)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

Both of the truth tables are same so the equation is also same.Only non-standard form is simplified version of standard form

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



Part 2

Combinational circuit design process and simulate with Deeds Simulator.

Design Process

i) Determine Parameter Input / Output and their relations.

ii) Construct Truth Table. iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.

iv) Draw the circuit and use duality symbol; convert AND-OR circuit to NAND gates ONLY.

v) Simulate the design using Deeds Simulator. Check the results according to Truth Table and Timing Diagram Operation.

Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.

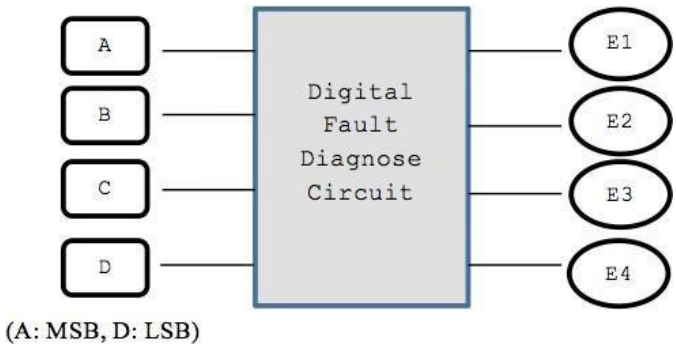


Figure 5

The following rules are used to activate the error's signal type:

RULE 1: E1 is activated if the input number is positive ODD and the majority of the bits is '0'.

RULE 2: E2 is activated if the input number is positive EVEN and the majority of the bits is '0'.

RULE 3: E3 is activated if the input number is negative ODD and the majority of the bits is '1'.

RULE 4: E4 is activated if the input number is negative EVEN and the majority of the bits is '1'.

RULE 5: The output of error signal is invalid if the input has equal bit '0' and bit '1'.

(**NOTE:** Positive ODD is positive numbers that are odd and negative EVEN is negative numbers that are even).

Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 1

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	x	x	x	X
0	1	0	0	0	1	0	0
0	1	0	1	x	x	x	X
0	1	1	0	x	x	x	x
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	x	x	x	X
1	0	1	0	x	x	x	x
1	0	1	1	0	0	1	0
1	1	0	0	x	x	x	x
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

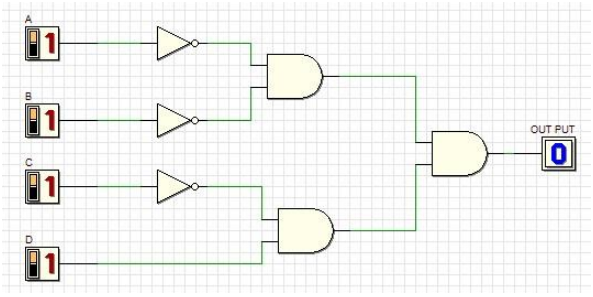
2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.

CD / AB	00	01	11	10
00	$E2_{(i)}$	$E1_{(i)}$	X	E2
01	$E2_{(i)}$	X		X
11	X	$E3_{(i)}$	$E3_{(1)}$	$E4_{(i)}$
10	0	X	$E3_{(i)}$	X

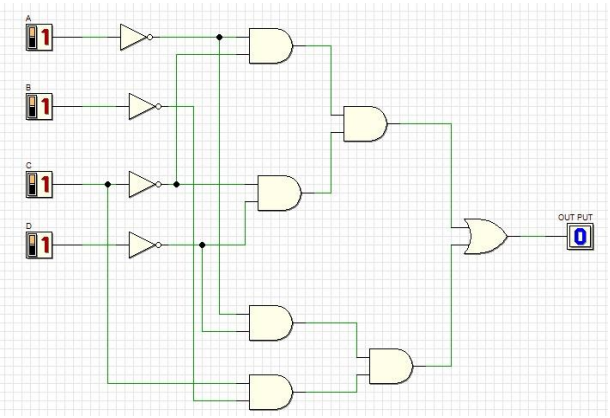
$$E1 = \bar{A}\,\bar{B}\,\bar{C}\,D$$
$$E2 = A\bar{B}\,\bar{C}\,\bar{D} + \bar{A}\,\bar{B}\,C\bar{D}$$
$$E3 = ABD + A\bar{B}\,CD$$
$$E4 = ABC\bar{D}$$

3.From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.

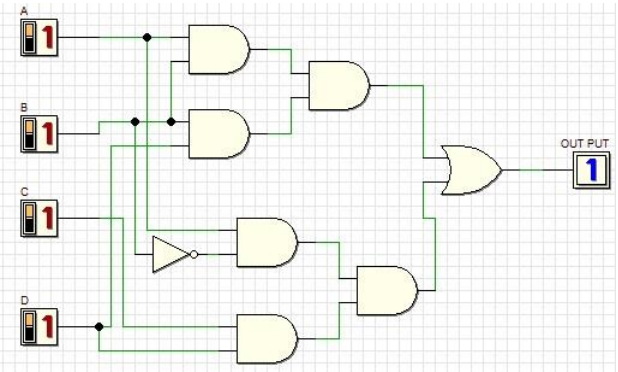
E1:



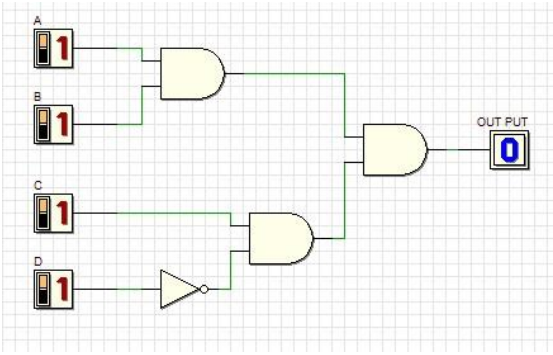
E2:



E3:



E4:



4.Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

Truth Table 2

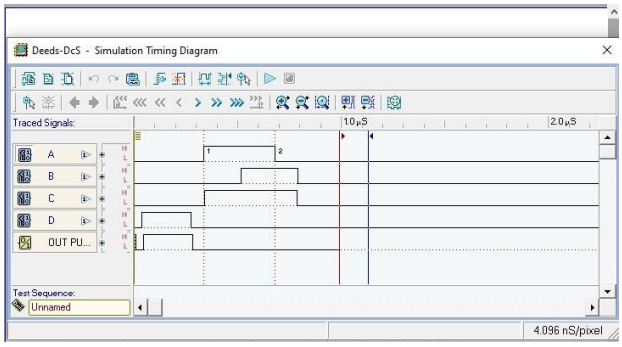
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

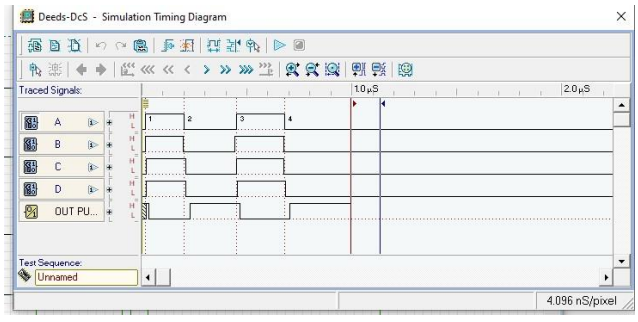
Same result as the equations were derived from the previous table.

b) Timing Diagram:

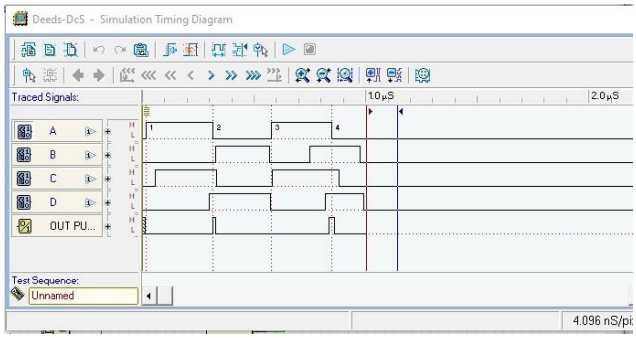
E1:



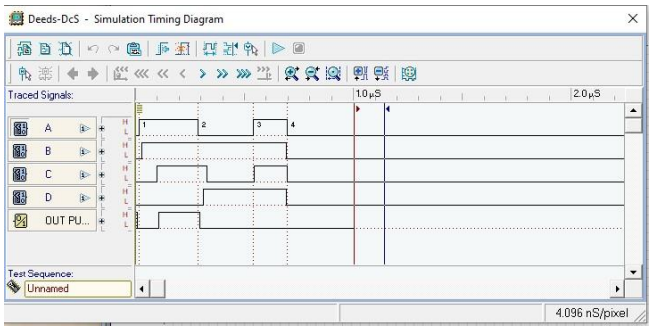
E2:



E3:



E4:

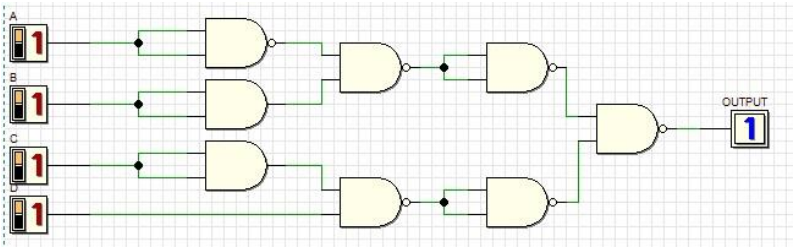


Explain some analysis values based on your timing diagram:

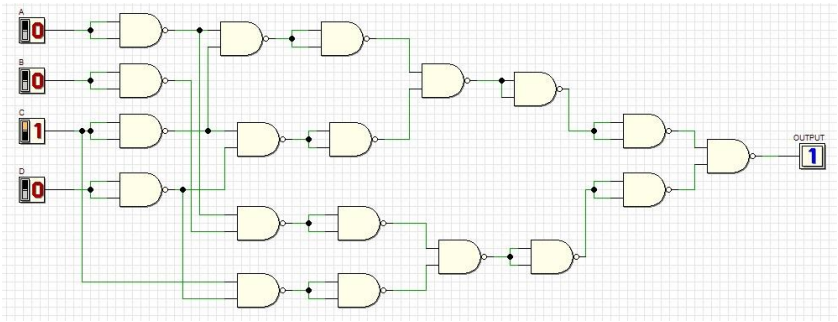
In the E1 only D value comes out as an output while for E2: If all inputs are low then output will be high, and for E3: if all input is high then output will be high and For E4: if the input for A, B, C is high and D is low then the output will be High.

5.Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.

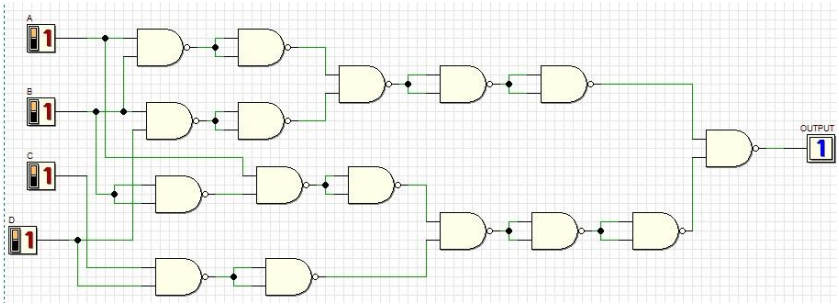
E1:



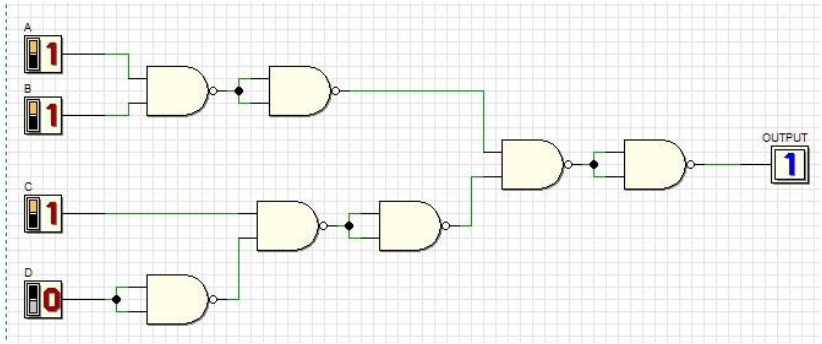
E2:



E3:



E4:



6.Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

Truth Table 3

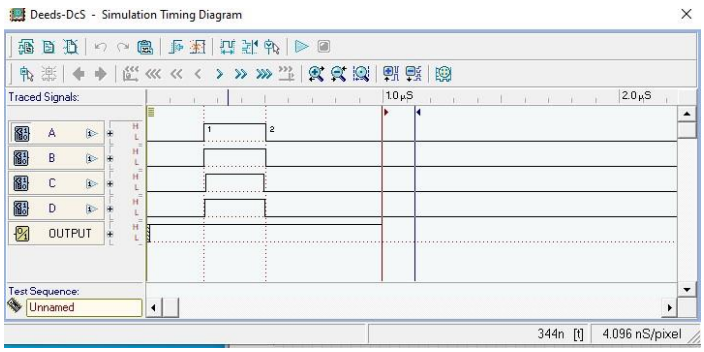
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	x	x	x	X
0	1	0	0	0	1	0	0
0	1	0	1	x	x	x	X
0	1	1	0	x	x	x	x
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	x	x	x	X
1	0	1	0	x	x	x	x
1	0	1	1	0	0	1	0
1	1	0	0	x	x	x	x
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

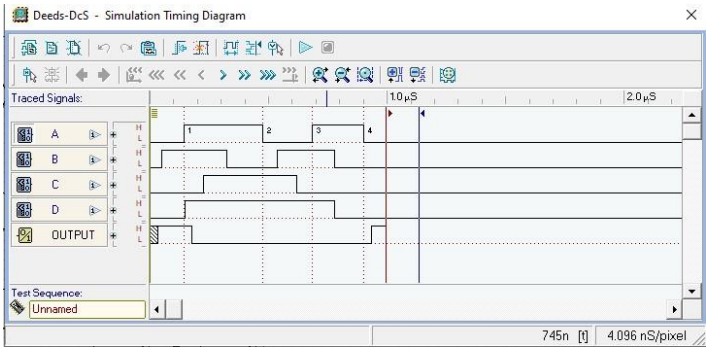
Same because NAND gates are universal gates. It has been used to replace The basic gates here.

b) Timing Diagram

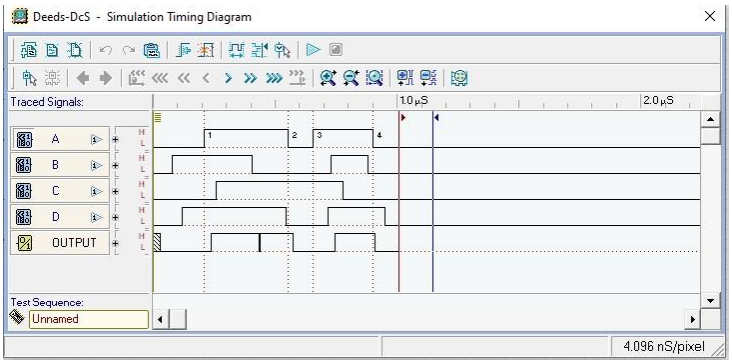
E1:



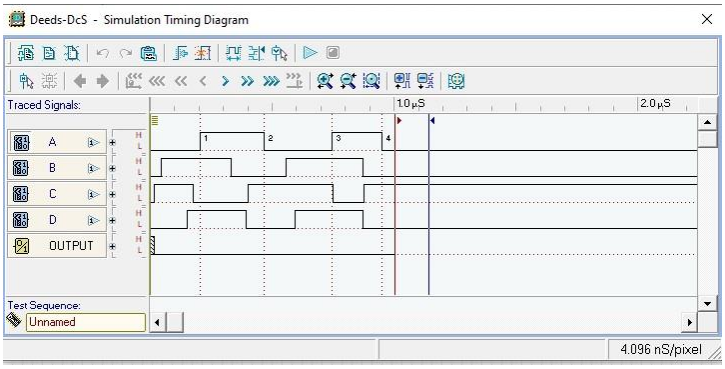
E2:



E3:



E4:



Explain some analysis values based on your timing diagram:

The timing diagram shows that the input value for A, B, C, D for each circuit

Fully Completed

Partially Completed

Checked by: _____