UTM

UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT : SECR1013 DIGITAL LOGIC

SESSION/SEM : 2020/2021 SEM 1

LAB 2 : COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION

NAME 1 : HUDA NAJIHAH BINTI AHMAD ASRI (A20EC0045)

NAME 2 : SAIDAH BINTI SAIFUL BAHARI (A20EC0141)

LECTURER : SIR FIROZ BIN YUSUF PATEL DAWOODI

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$\mathbf{Y = AB + BC + AC}$$

1. Convert the non-Boolean expression into standard form.

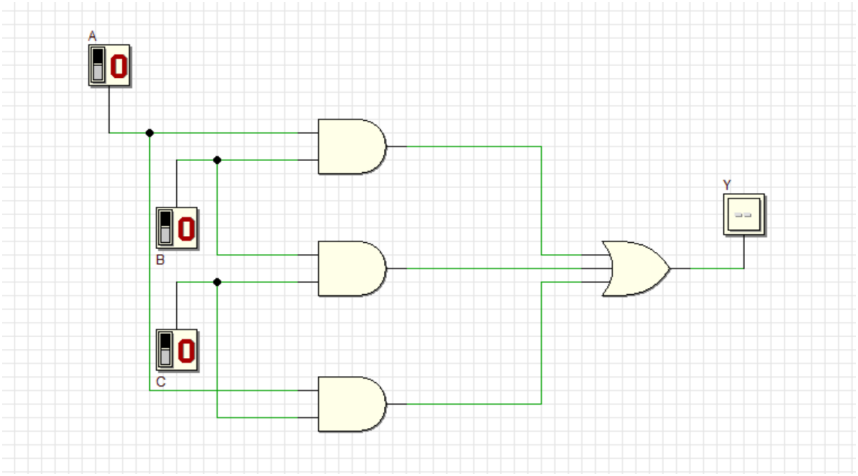
$$\begin{aligned} Y &= AB(C + \bar{C}) + BC(A + \bar{A}) + AC(B + \bar{B}) \\ &= ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C \\ &= ABC + \bar{A}BC + A\bar{B}C + AB\bar{C} \end{aligned}$$

2. Based on standard form expression, complete the following truth table.

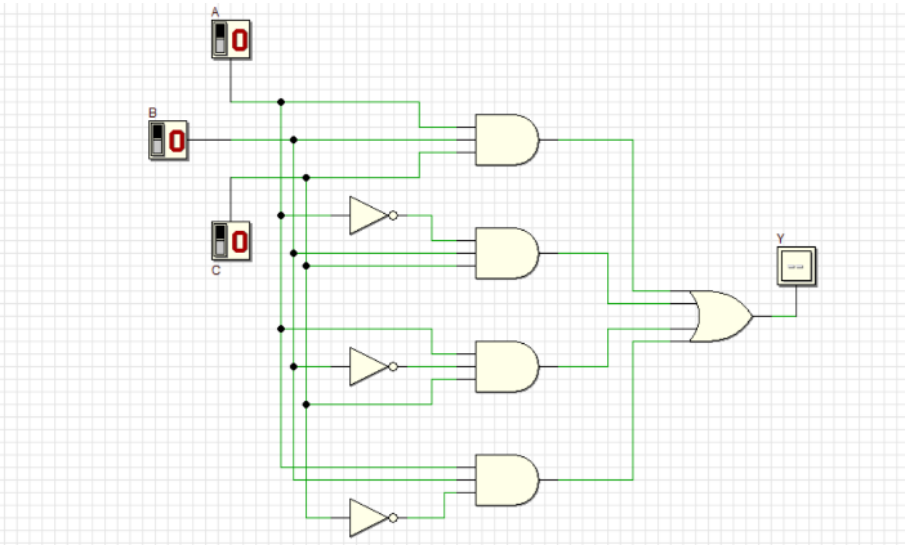
INPUT			**OUTPUT**
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. Using Deeds Simulator, draw the following circuit:

a) Circuit (i) for non-standard form (based on the given expression)

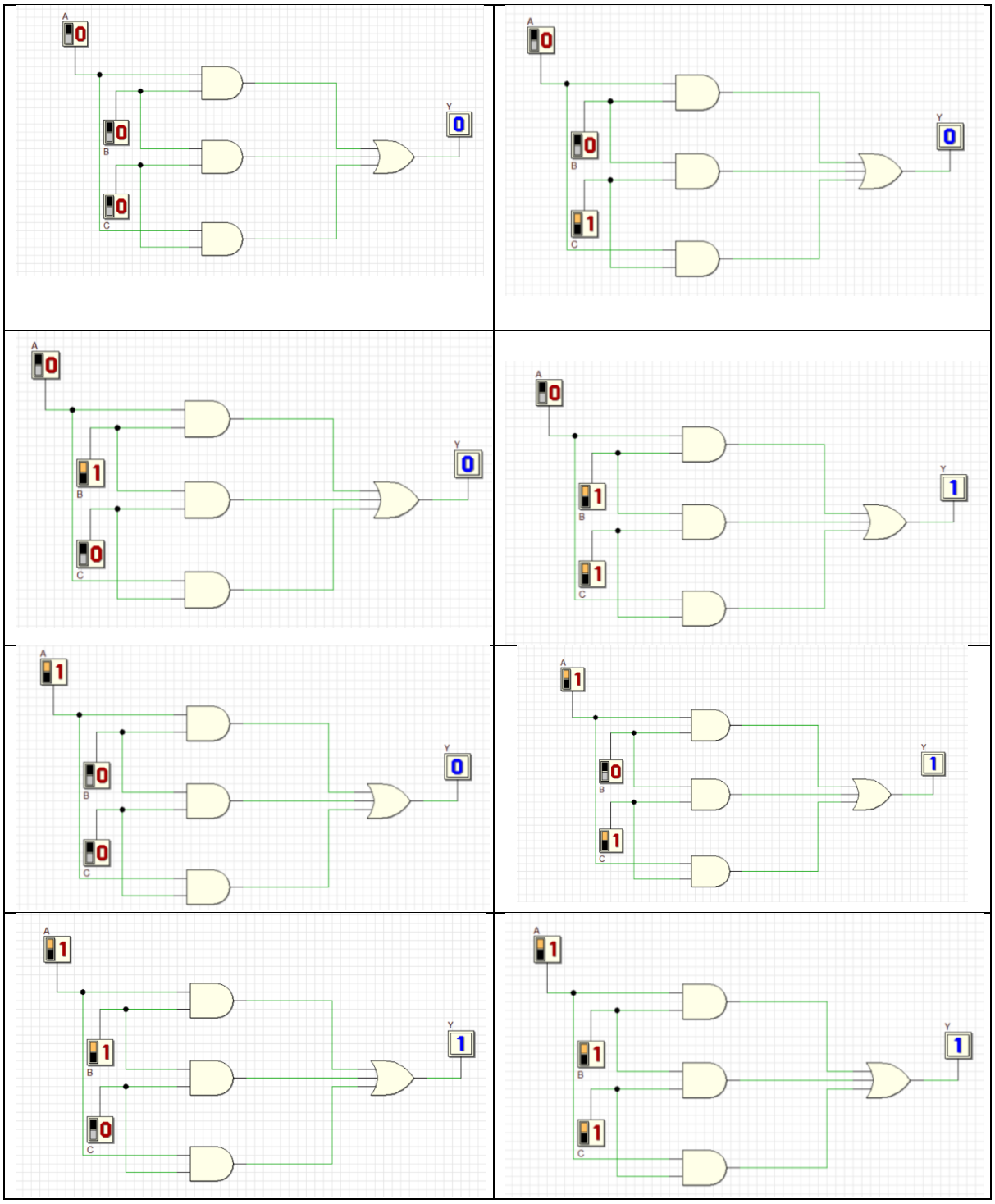


b) Circuit (ii) for standard form (from your answer in question (1))



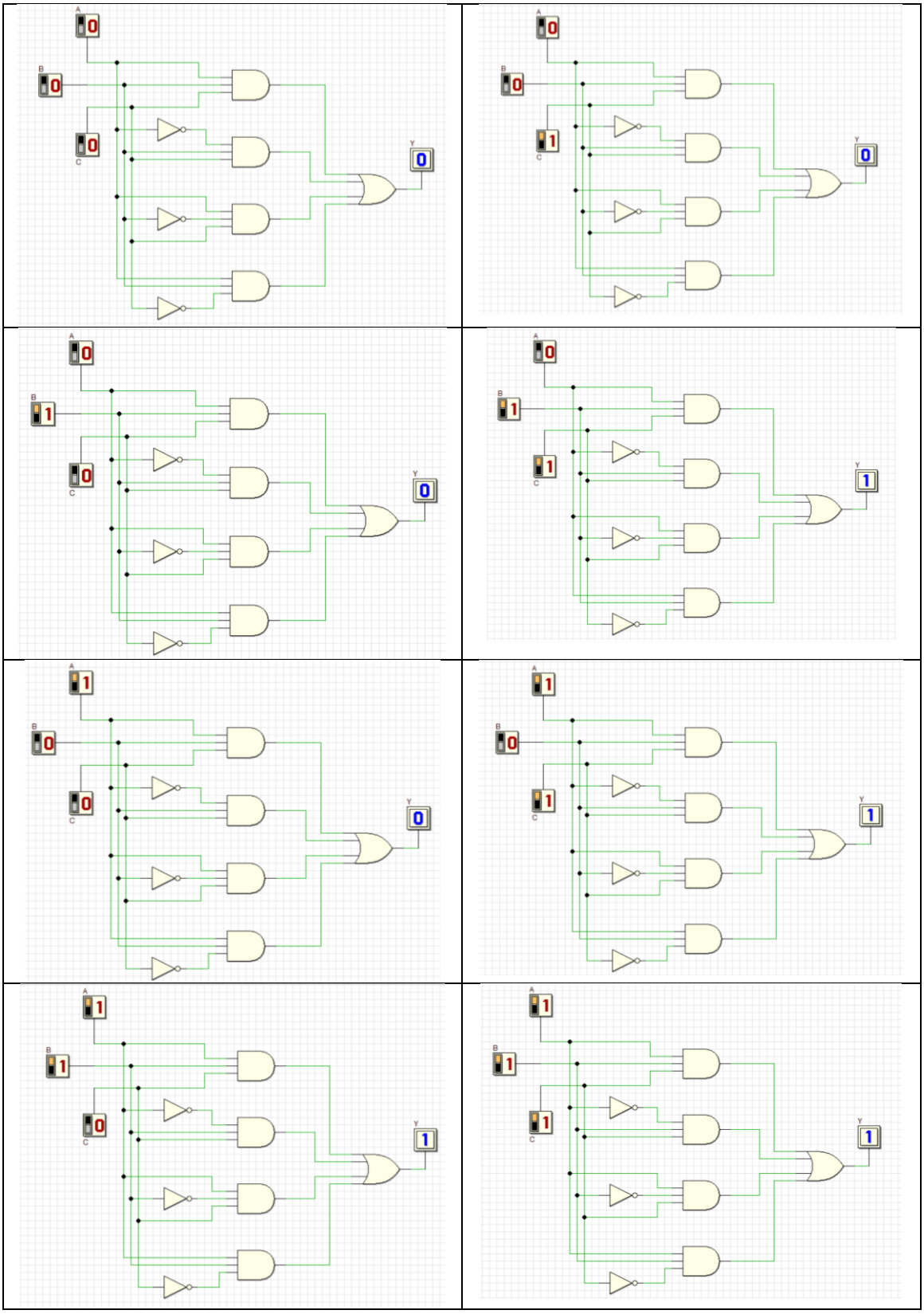
4. Simulate these two circuits in step (3) and complete their truth table.
   Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)



INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Circuit (ii)

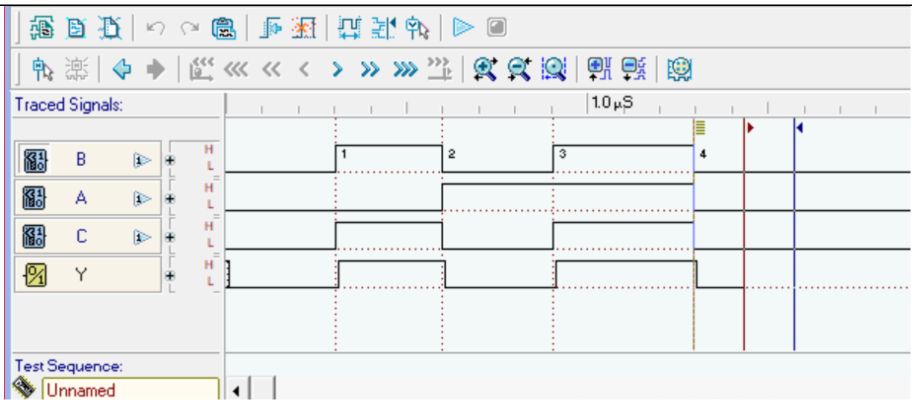

A
B
C
Y
0
0
0
0
A
B
C
Y
0
0
1
0
A
B
C
Y
0
1
0
0
A
B
C
Y
0
1
1
1
A
B
C
Y
1
0
0
0
A
B
C
Y
1
0
1
1
A
B
C
Y
1
1
0
1
A
B
C
Y
1
1
1
1

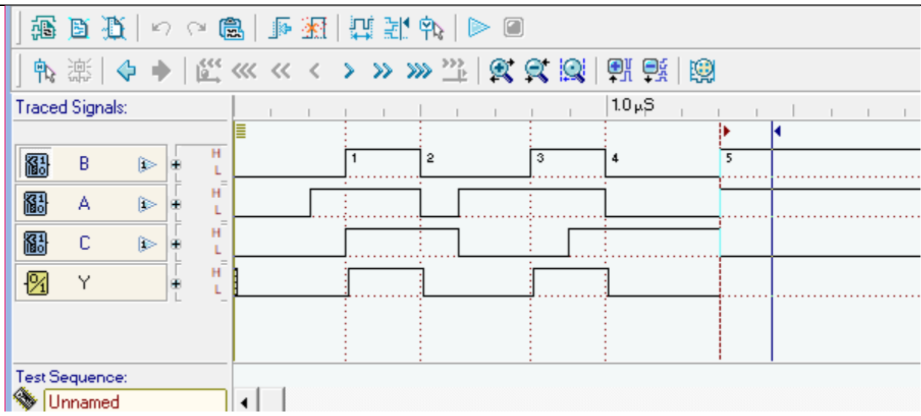
INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

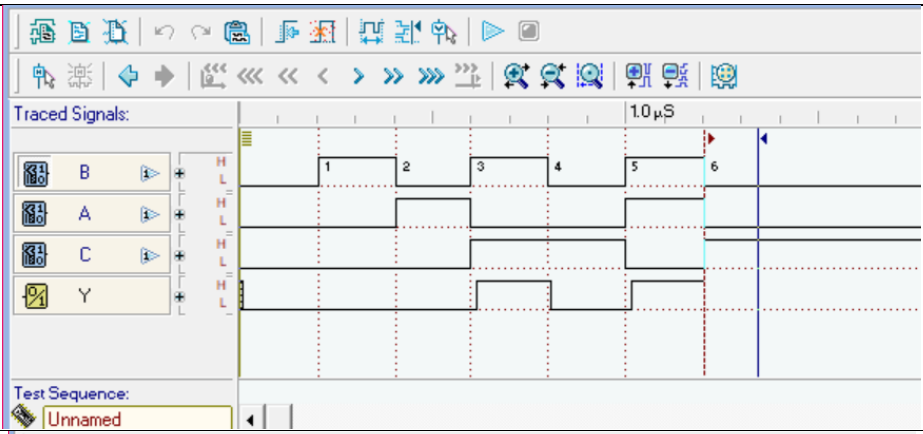
Conclusion:

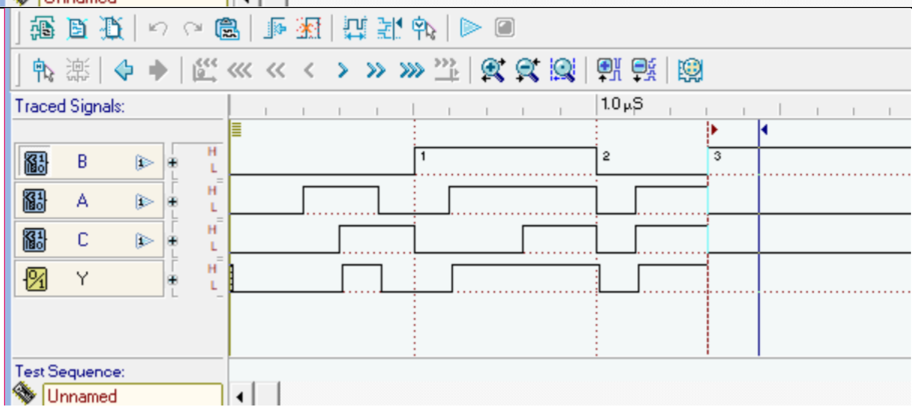
The output for non-standard and standard Boolean expression are the same. The non-standard Boolean expression is the simplification of the standard Boolean expression.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.









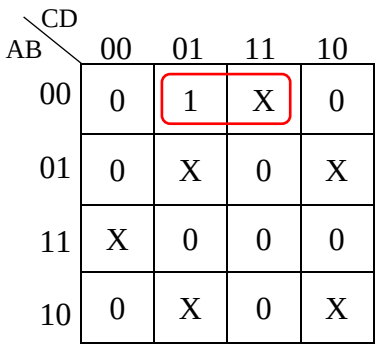
Part 2

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

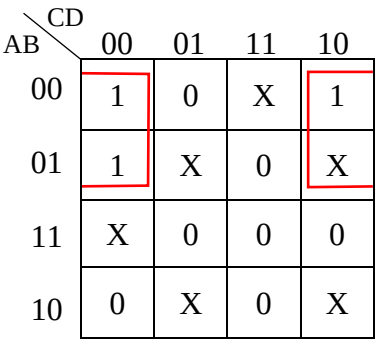
Truth Table 1

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

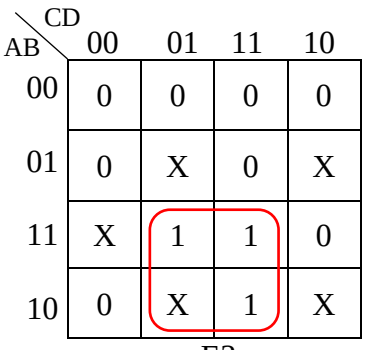
2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.



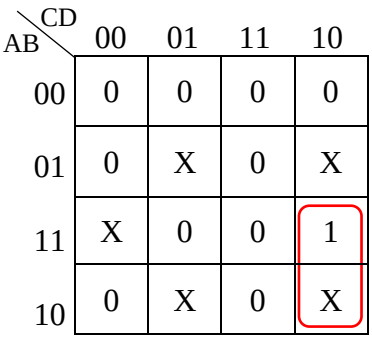
E1



E2



E3



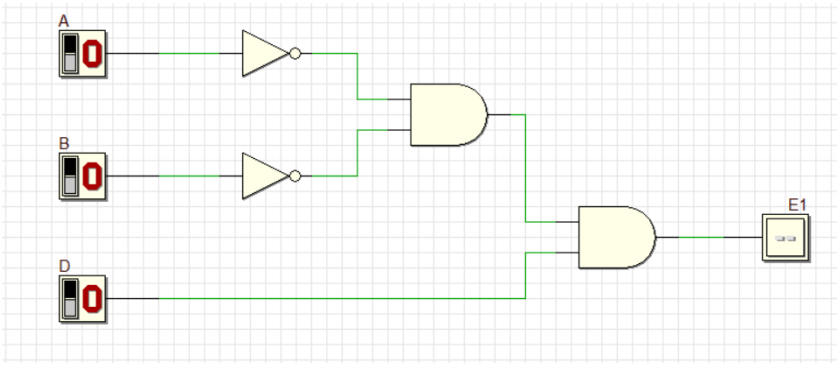
E4

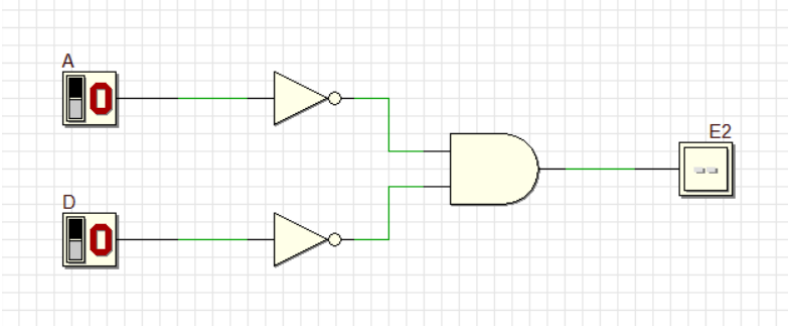
Minimized SOP Boolean Expression

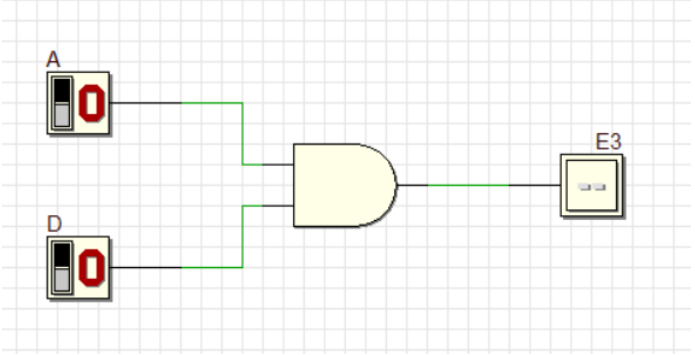
E1: $\bar{A}\bar{B}D$ E2: $\bar{A}\bar{D}$

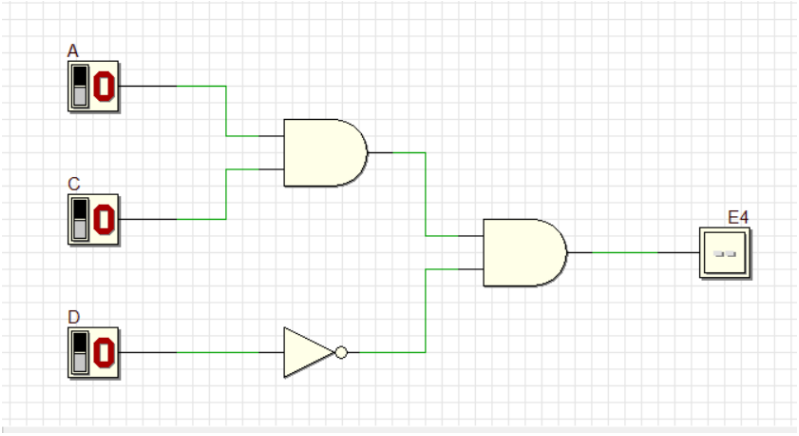
E3: AD E4: $AC\bar{D}$

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.

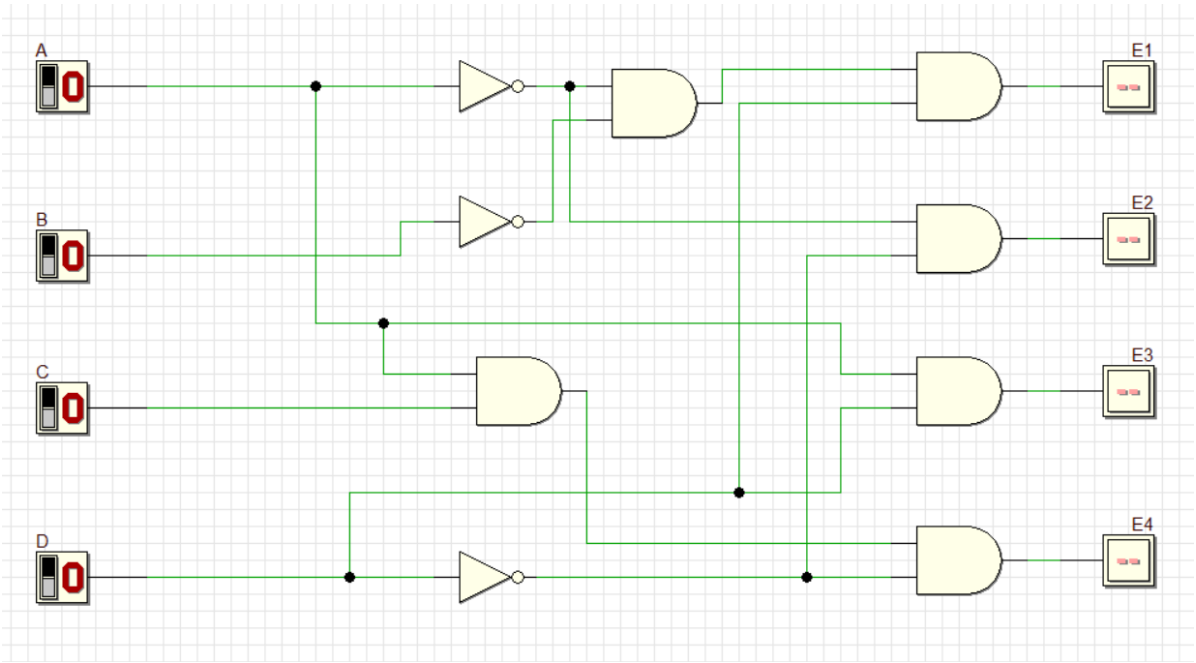




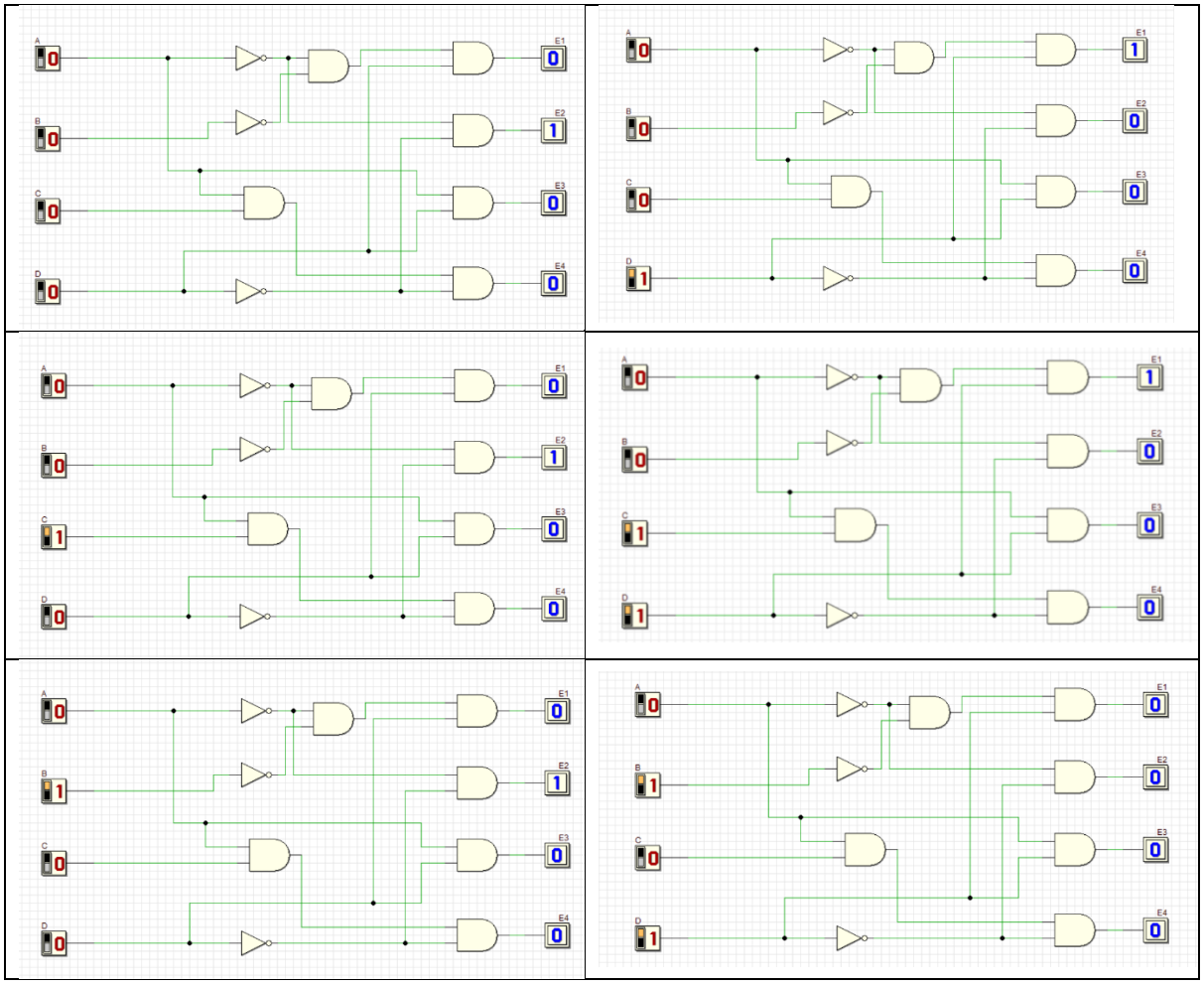


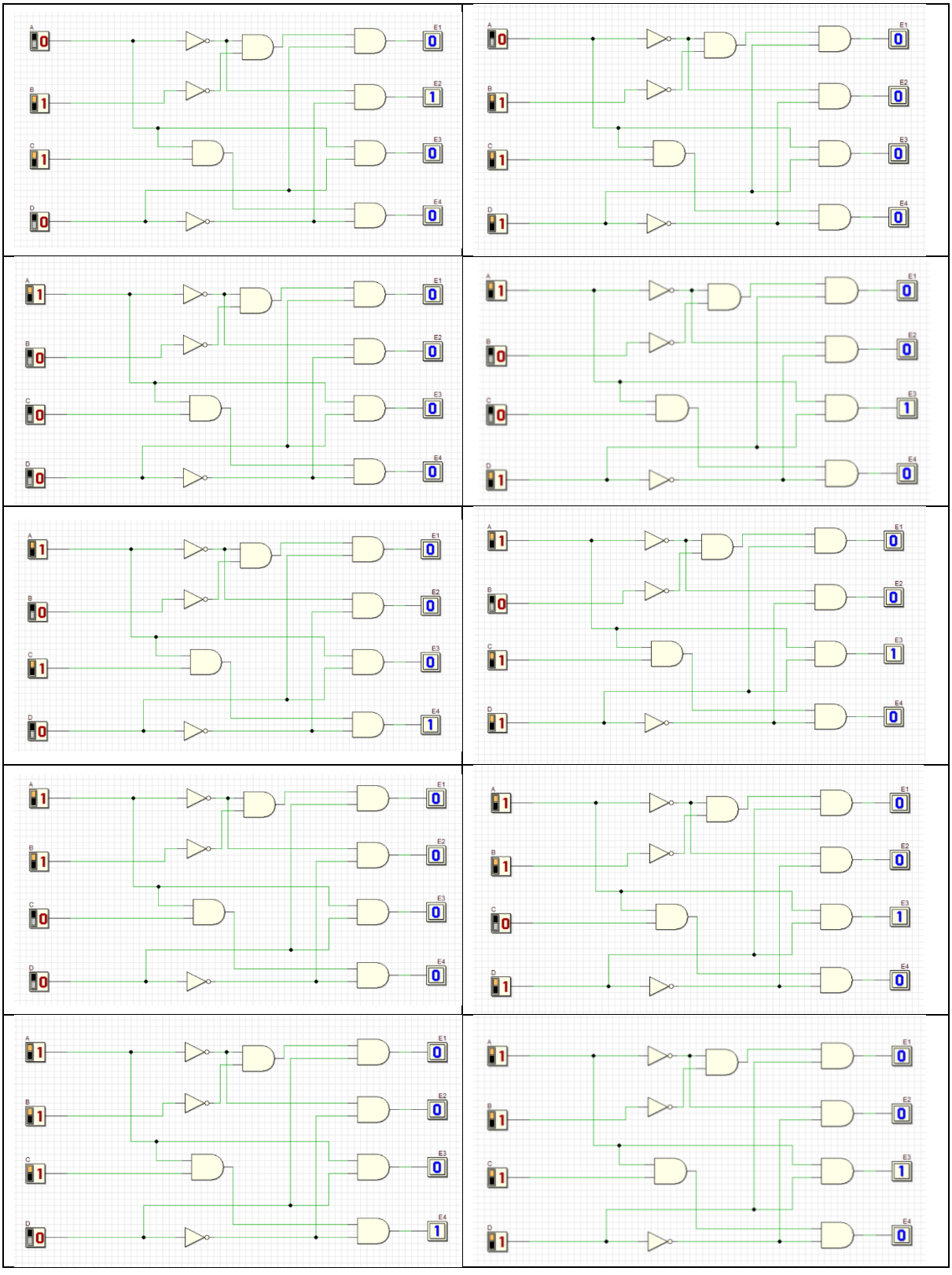


Combined circuits of E1, E2, E3 and E4:



4. Simulate the Deeds circuit in step (3):




A 0
B 1
C 1
D 0
E1 0
E2 1
E3 0
E4 0
A 0
B 1
C 1
D 1
E1 0
E2 0
E3 0
E4 0
A 1
B 0
C 0
D 0
E1 0
E2 0
E3 0
E4 0
A 1
B 0
C 0
D 1
E1 0
E2 0
E3 1
E4 0
A 1
B 0
C 1
D 0
E1 0
E2 0
E3 0
E4 1
A 1
B 0
C 1
D 1
E1 0
E2 0
E3 1
E4 0
A 1
B 1
C 0
D 0
E1 0
E2 0
E3 0
E4 0
A 1
B 1
C 0
D 1
E1 0
E2 0
E3 1
E4 0
A 1
B 1
C 1
D 0
E1 0
E2 0
E3 0
E4 1
A 1
B 1
C 1
D 1
E1 0
E2 0
E3 1
E4 0

a) Update Truth Table 2 based on the simulation result.

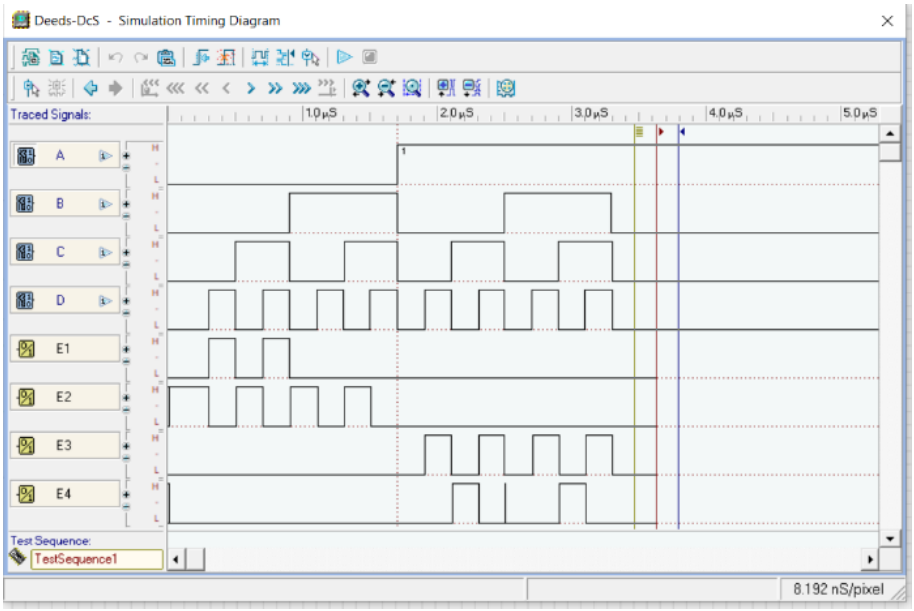
Truth Table 2

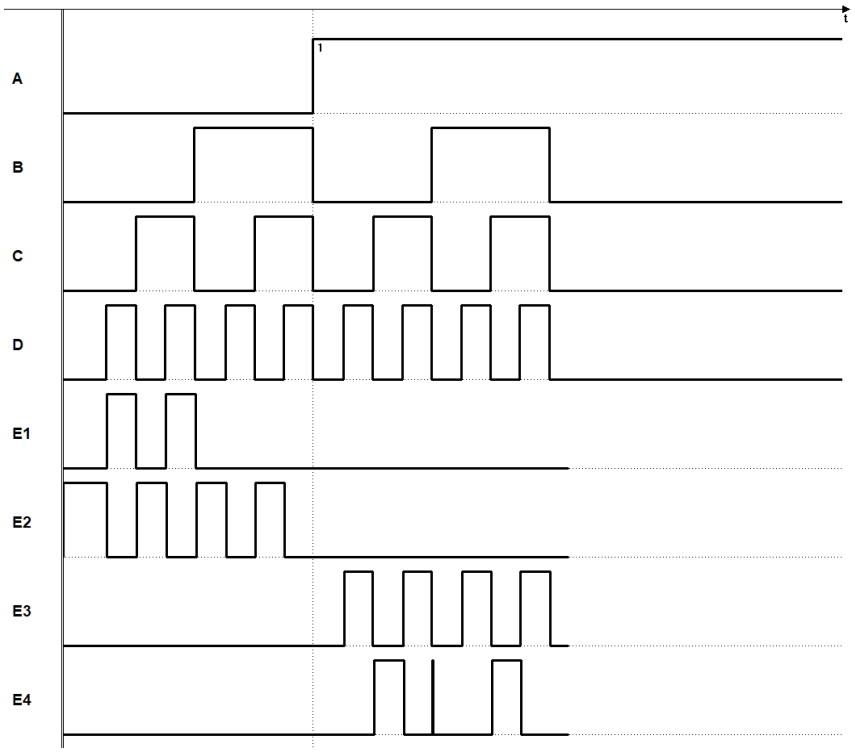
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

In Truth Table 1, the outputs for input that qualified in Rule 5 are considered as *Don't Care*, meanwhile in Truth Table 2, there are outputs for inputs that fulfilled the Rule 5. But those outputs can be cancelled because as stated in Rule 5, the output is invalid if the input has equal bit '0' and bit '1'. Putting aside the outputs for inputs that have the equal bit '0' and '1', the output results are the same.

b) Timing Diagram

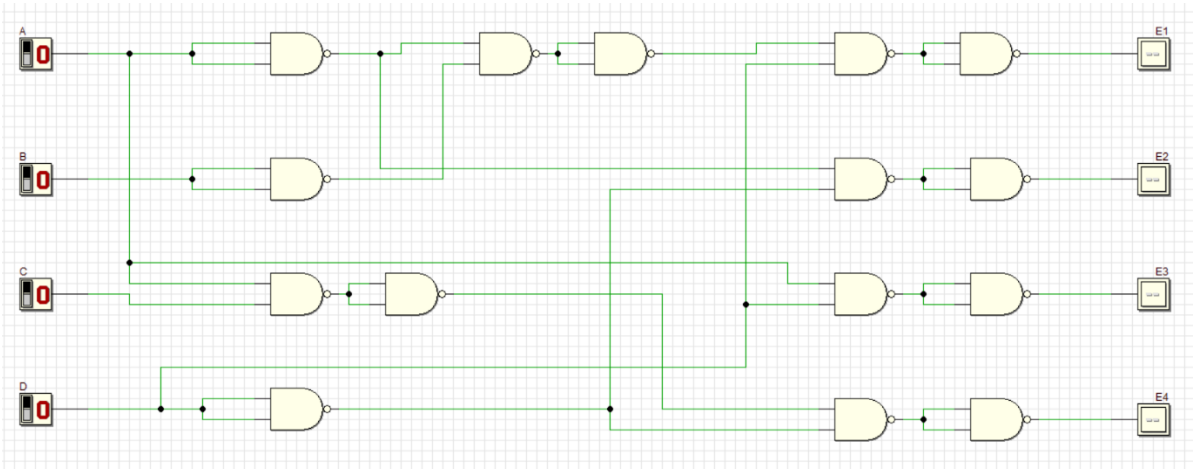




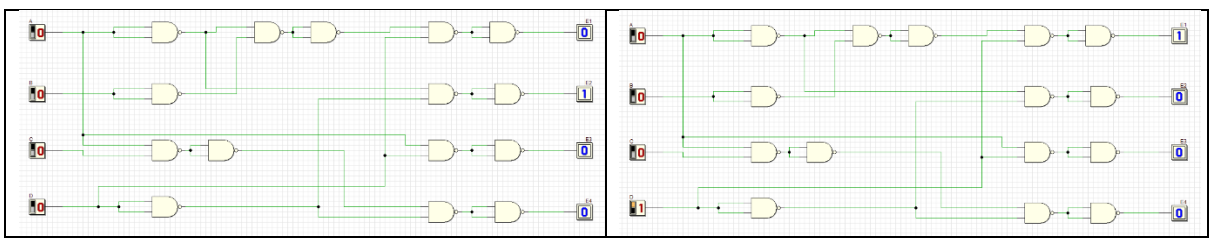
Explain some analysis values based on your timing diagram:

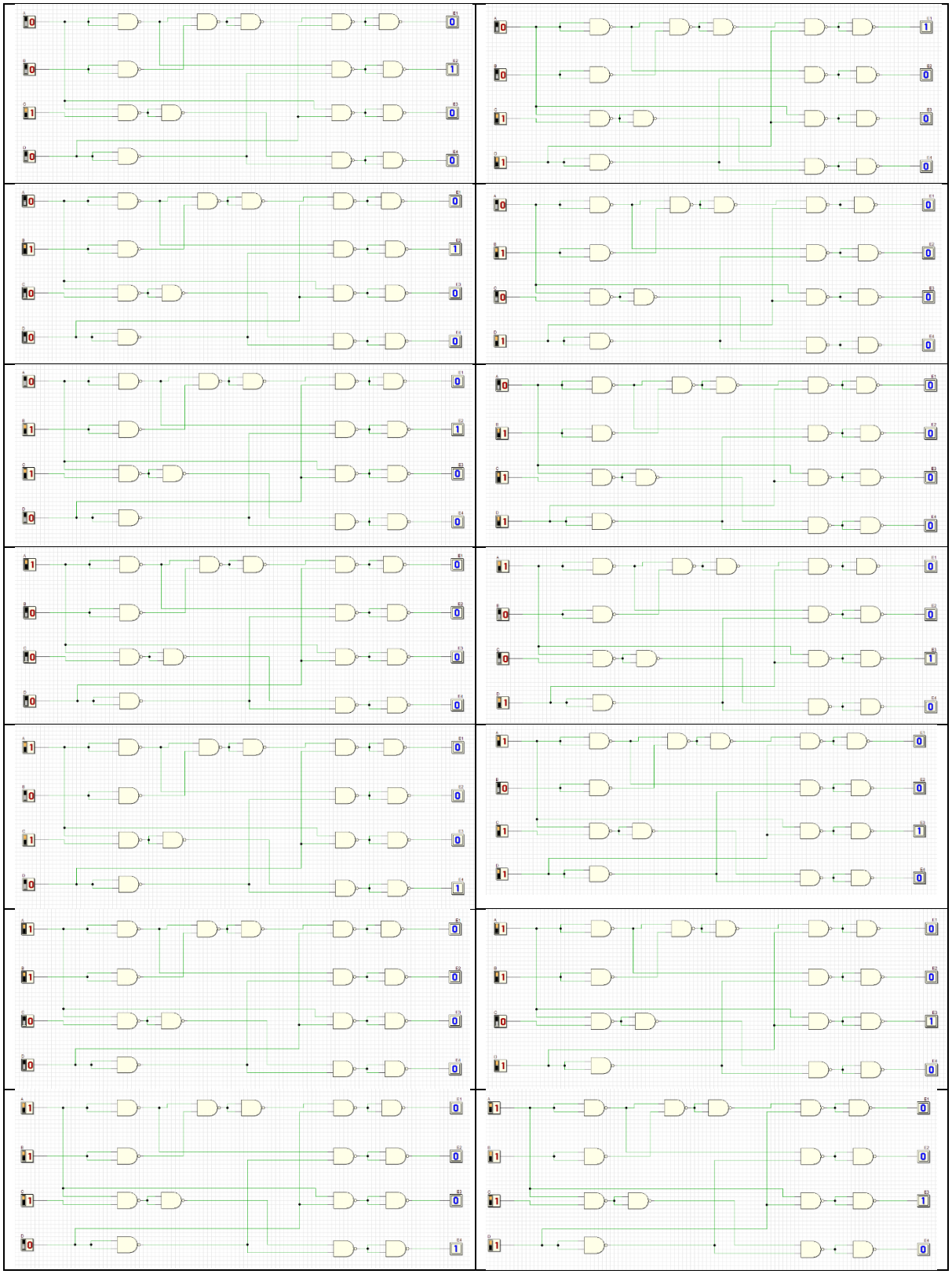
The timing diagram has the same output values as in Truth Table 2. Each waveform from inputs A, B, C and D affect the output in E1, E2, E3 and E4. As example when A, B and C is LOW while B is HIGH, only E2 is HIGH and the other outputs are LOW.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):





a) Update Truth Table 3 based on the simulation result.

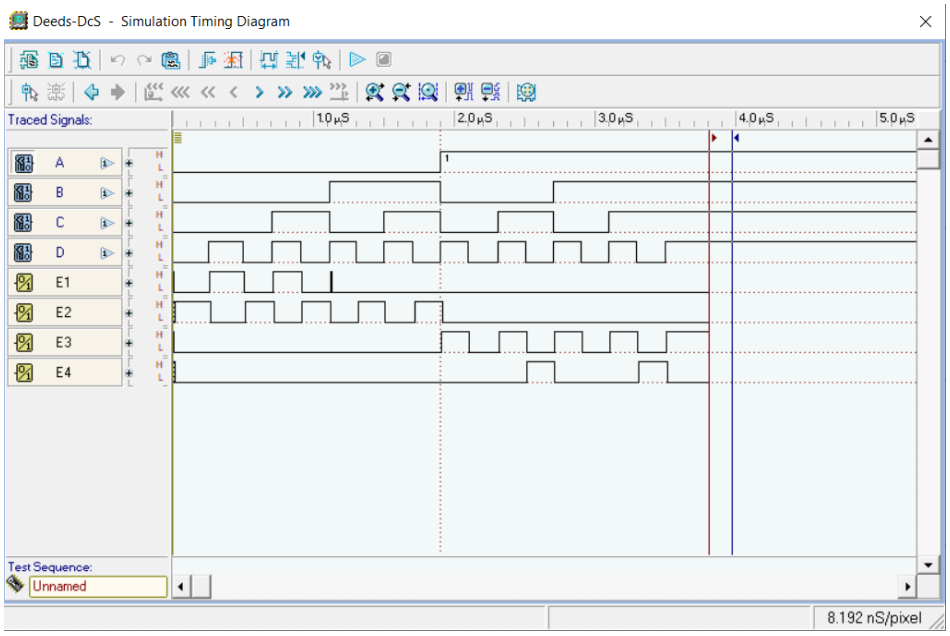
Truth Table 3

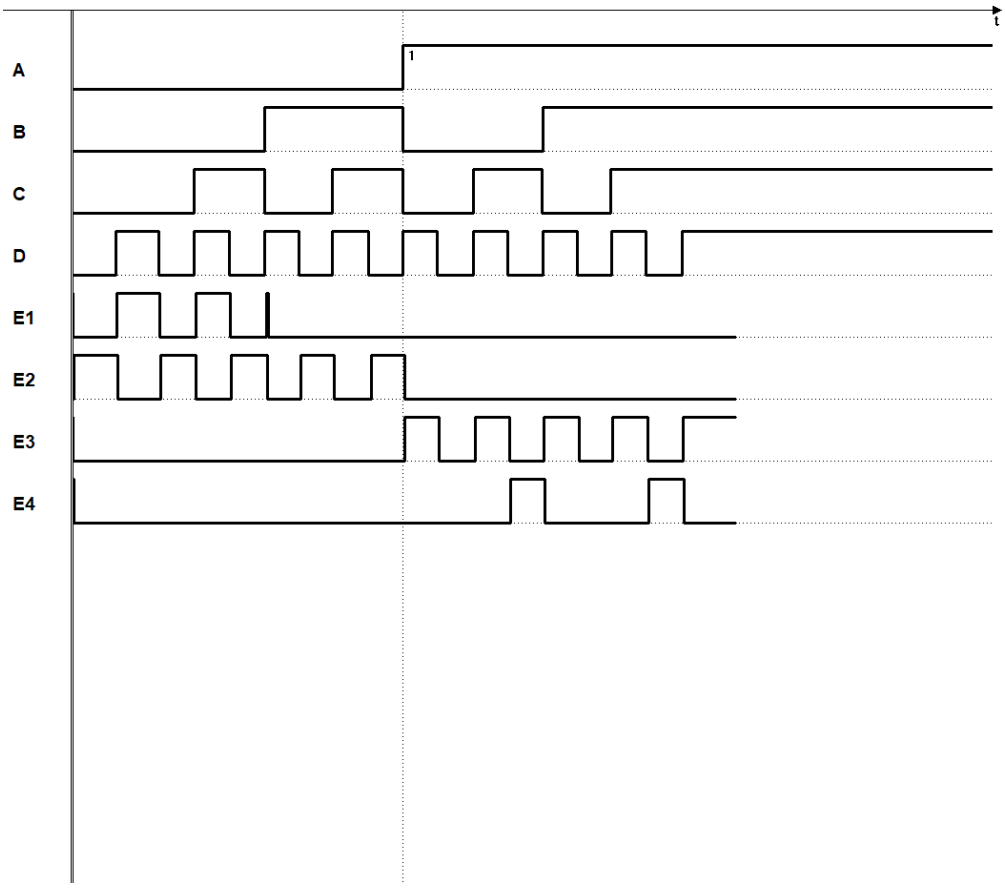
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

The output results in both Truth Table 3 and Truth Table 2 are the same. Thus, NAND is a universal gate that can replace basic gates.

b) Timing Diagram





Explain some analysis values based on your timing diagram.

The waveforms at E1, E2, E3 and E4 reflect the outputs for the circuit. As example when A and D are HIGH, while B and C are LOW, only E3 is HIGH while the other outputs are LOW. There are more waveforms that made E2 and E3 HIGH compared to E1 and E4.