Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT	:	SCSR1013 DIGITAL LOGIC
SESSION/SEM	:	01
LAB 3	:	**SYNCHRONOUS DIGITAL COUNTER**
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DATE	:	26/1/2021

REMARKS :

MARKS:

Lab #3

Identifying The Properties of a Synchronous Counter

A. Aims

1) Expose the student with experience on constructing synchronous counter circuit using Flip-Flop IC, Basic Gate ICs, Breadboard and ETS-5000 Digital Kit.
2) Promote critical thinking among students by analyzing the given circuit and identifying the behavior of the digital circuit.

B. Objectives

The objectives of this lab activity are to:

1) Implement a synchronous counter circuit into physical circuit using Breadboard, Flip-Flops, Basic Gates and Switches.
2) Completing the next-state table of the counter circuit.
3) Sketch the state diagram of the counter circuit.
4) Identify the properties of the counter.

C. Materials And Equipments

Materials and equipment required for this lab are as follows:

Item Name	Number of Item
1. Breadboard	1
2. 7408 Quad 2-Input AND	1
3. 7404 Hex Inverter	1
4. 7432 Quad 2-input OR	1
5. 7476 Dual J-K Flip Flop	1
6. ETS-5000 Digital Kit	1

D. Introduction

Flip-Flops

A flip-flop is the simplest type of memory cell. Its output, Q, does not depend solely upon its inputs, but also depends on the order in which they are applied. Thus, the flip-flop is not a combinational circuit, but is a sequential circuit. The flip-flop is the key building block of most synchronous sequential circuits. There are four common types of flip-flops. The symbol and truth table for each is shown in Figure 1.

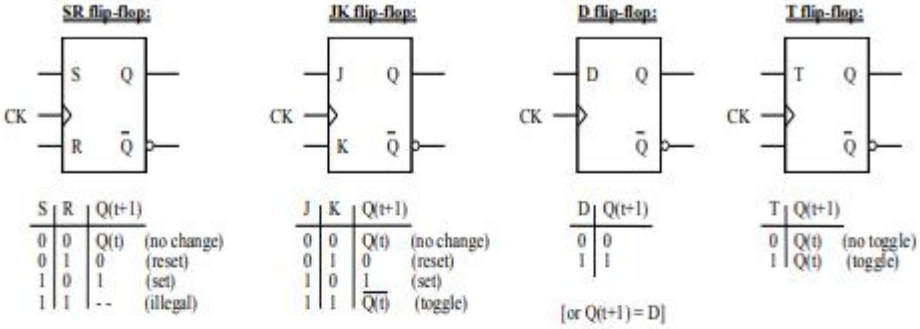


Figure 1: Four common types of flip-flops

Flip-flops are synchronous devices meaning that the output responds to the synchronous inputs (S, R, J, K, D or T) only on certain clock edges. There are three main types of triggering:

1) **positive-edge triggering** - the output Q can only change on the positive (rising) edge of the clock (due to the values of the synchronous inputs).
2) **negative-edge triggering** - the output Q can only change on the negative (falling) edge of the clock (due to the values of the synchronous inputs).
3) **master-slave triggering** - the synchronous inputs are "*read*" on the positive edge of the clock, but the output Q does not respond until the negative edge of the clock.

The type of triggering is sometimes indicated by the symbol. Shown below in Figure 2 are JK flip-flops with all three types of triggering.

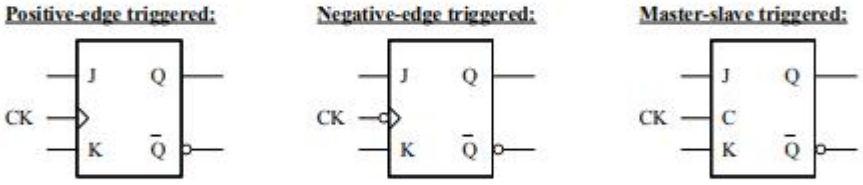


Figure 2: JK Flip-flops with different types of triggering

Flip-flops often have asynchronous inputs available also. These inputs are not synchronized with the clock, therefore, the output may respond immediately to changes in these inputs. There are two types of asynchronous inputs commonly used:

1) **PRESET** (also called **SET**) - used to preset the output Q to 1
2) **CLEAR** (also called **RESET**) - used to clear the output (set Q to 0)

Asynchronous inputs are often active-LOW. Therefore, they are typically tied HIGH for normal flip-flop operation. The PRESET or CLEAR may be momentarily set LOW to initialize the flip-flop to some desired initial value.

The symbol for a flip-flop often shows the asynchronous inputs as indicated below in Figure 3.

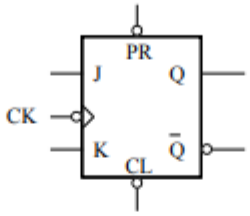


Figure 3: JK Flip-flops with asynchronous PRESET and CLEAR inpu

E. Preliminary Works

1) Using 7476 IC, connect the synchronous input (J, K) of a JK flip-flop to switches and its output (Q) to an LED. Connect the CLK input to a pulser switch, $\overline{A}$. Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	J	K	CLK	Q
Set initial value Q = 1	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	⇓	1
Output Q become 0, no change in asynchronous input	1	1	0	1	⇓	0
Output Q is not the previous Q	1	1	1	1	⇓	1
RESET Q	1	1	0	1	⇓	0
SET Q	1	1	1	1	⇓	1

2) Answer all questions.

a) Which state that JK flip-flop has, but not on SR flip-flop.

JK flip-flop has toggle when both J and K input is '1', while SR flip-flop does not have toggle and getting '1' on both S and R is invalid.

b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

JK flip-flop in 7476 is a negative-edge triggered flip-flop.

F. Lab Activities

1) You are given a counter circuit as shown in Figure 4.

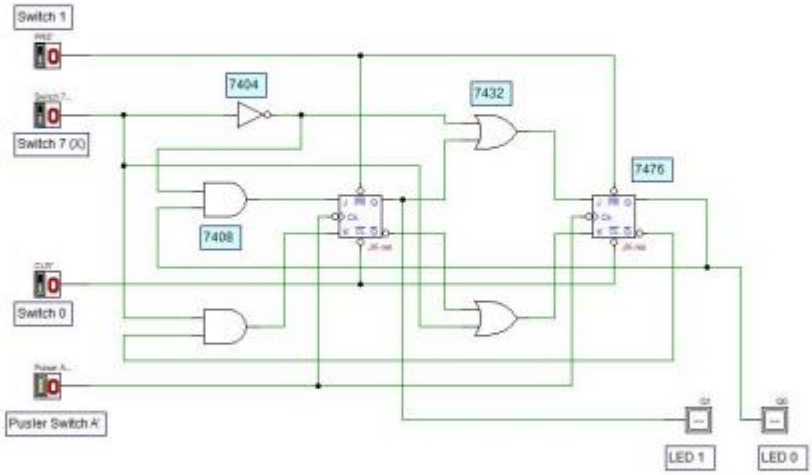
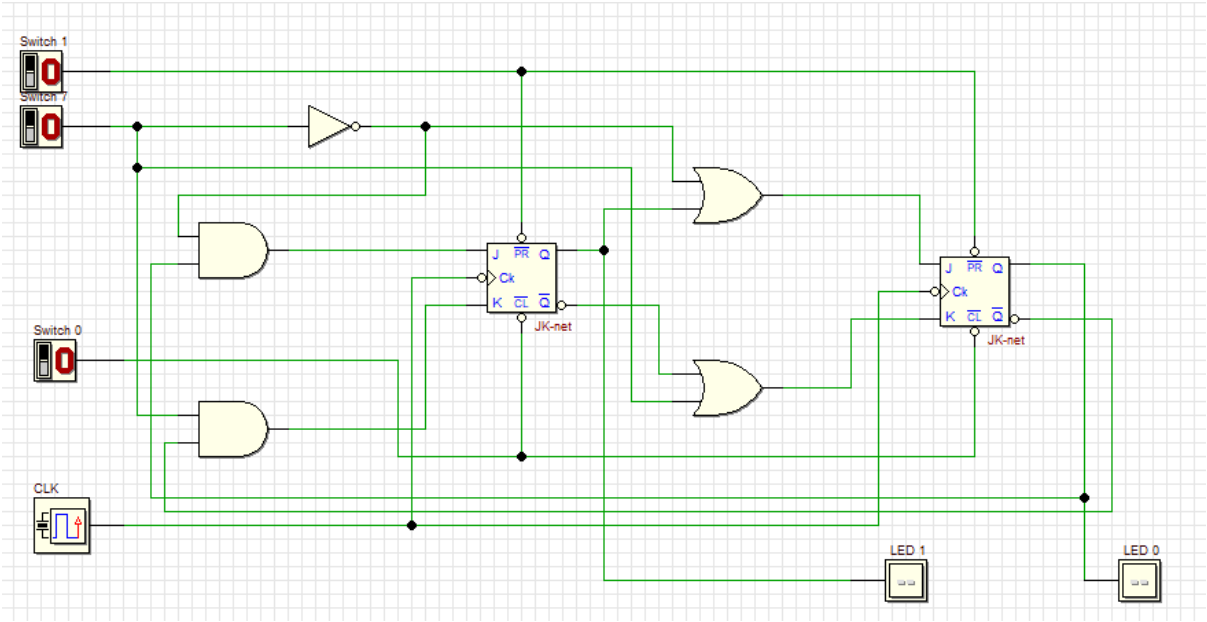


Figure 4: A Synchronous Counter Circuit

2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).

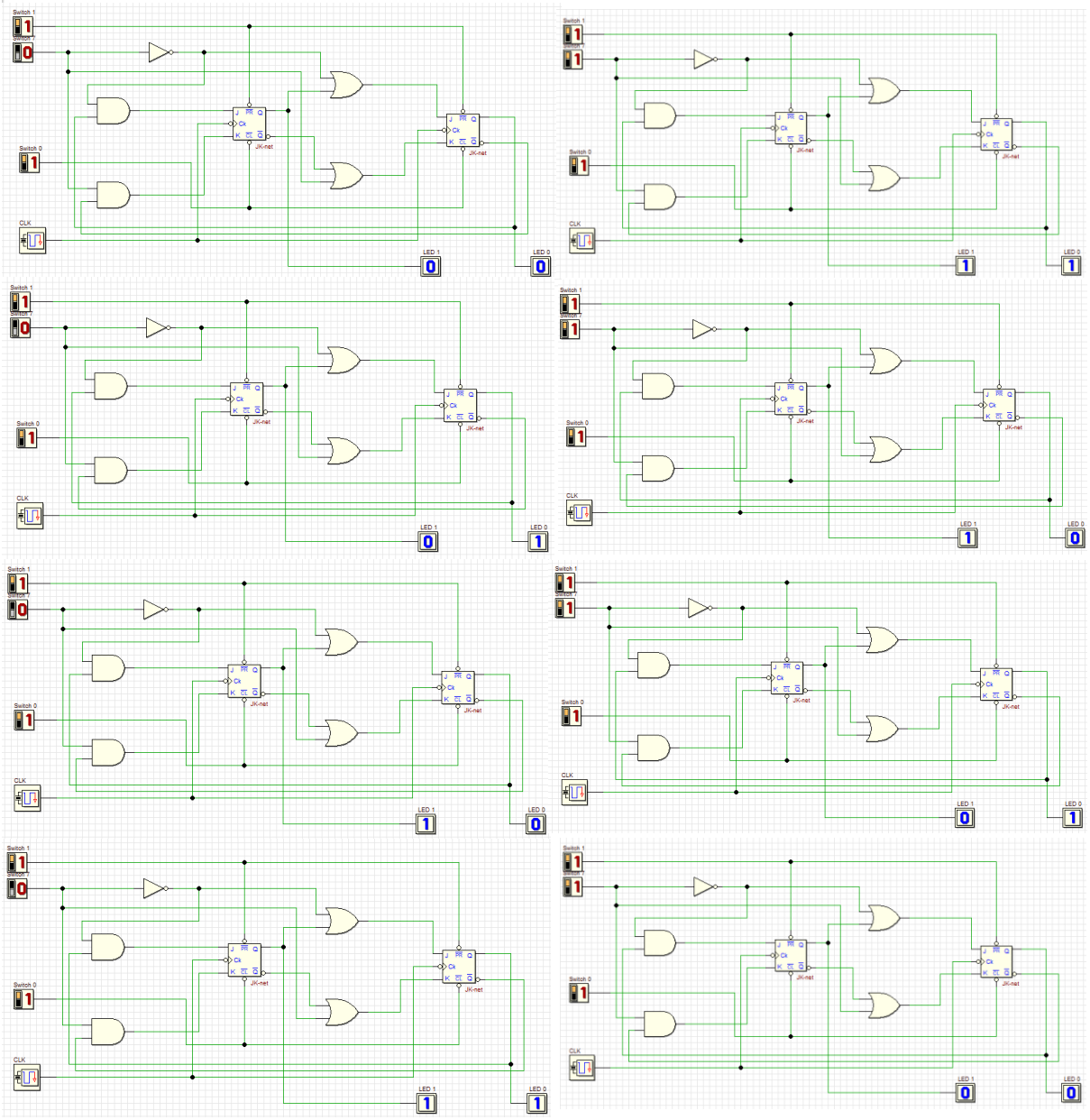


3) Investigate the behavior of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the *Next-State* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state. (0=LOW, 1=HIGH)

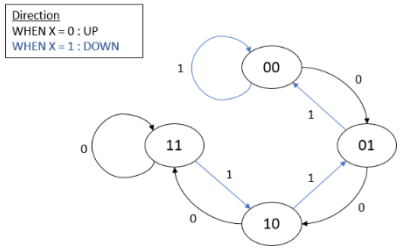
Table 2

Switch 7	Present State		Next State	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* _____



4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?

= The flip flops in the circuit are triggered with same clock simultaneously.

b) How many states are available for the counter and what are they?

= 4 states which are 00, 01, 10, and 11.

c) What is the function of Switch 7 (X) in the circuit?

= Switch 7 (X) determines which direction the counter will be, which is either up (increment) or down (decrement).

d) What is the function of Switch 0 and Switch 1 in the circuit?

= Switch 0 is CLR while switch 1 is PRE. Switch 0 functions to force the output to '0' while switch 1 functions to force the output to '1'. When both of the switches are set to '1', then the counter will function normally.

e) Is the counter a saturated counter or recycle counter?

= The counter is a saturated counter because when the counter reaches the minimum or maximum value, it will stay at that value instead of recycling back.

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* _____

6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3

Table 3

Input	Present State		Next State		D FF Transition	
X	Q1	Q0	Q1+	Q0+	D1	D0

b) Get the optimized Boolean expression.

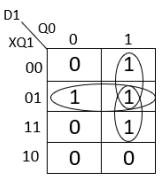
c) Draw the complete final circuit design in Deeds.

d) Simulate the circuit to prove that your Table 3 is correct.

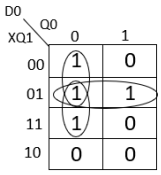
6) a)

Input,	Present State		Next State		D FF Transition	
X	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

b)

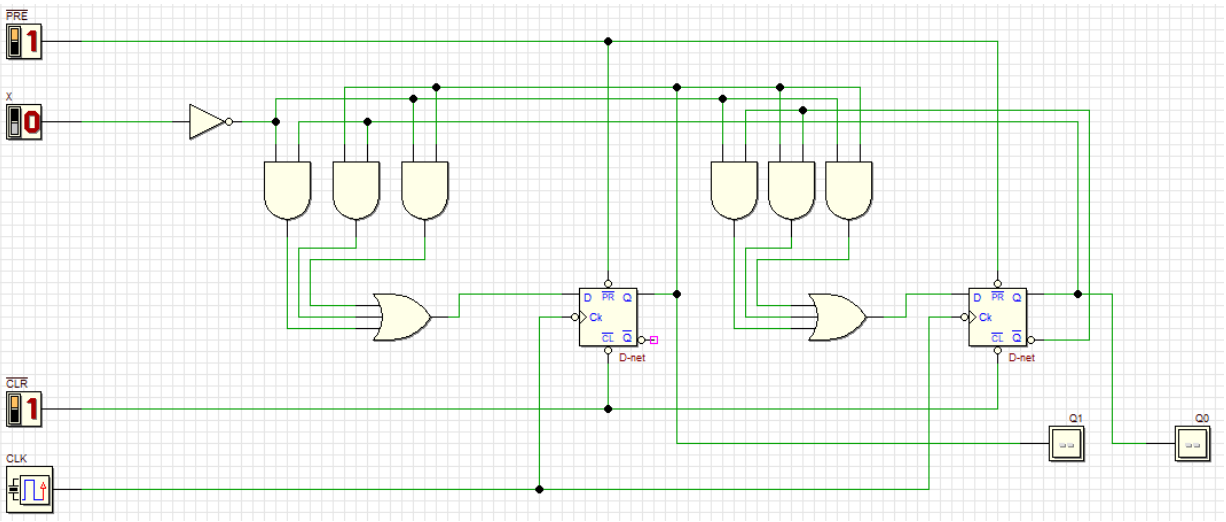


D1 = $\overline{X}$Q0 + Q1Q0 + $\overline{X}$Q1

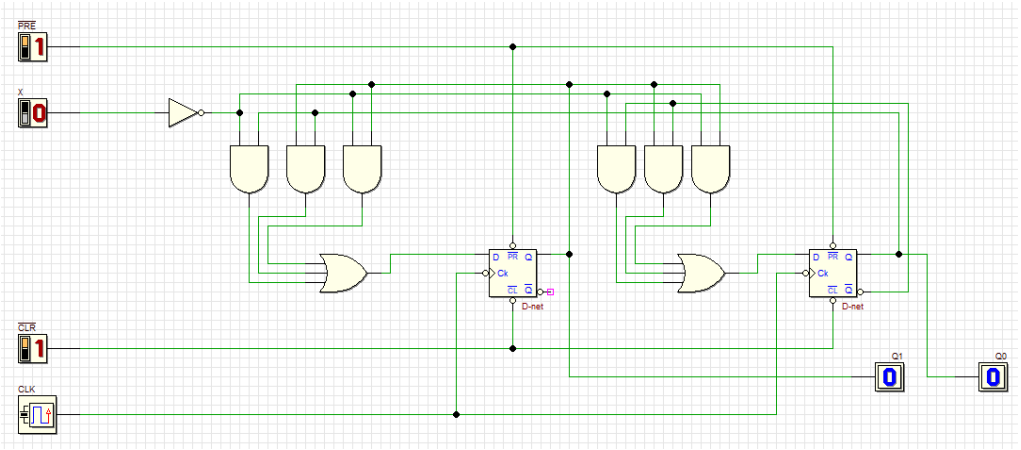


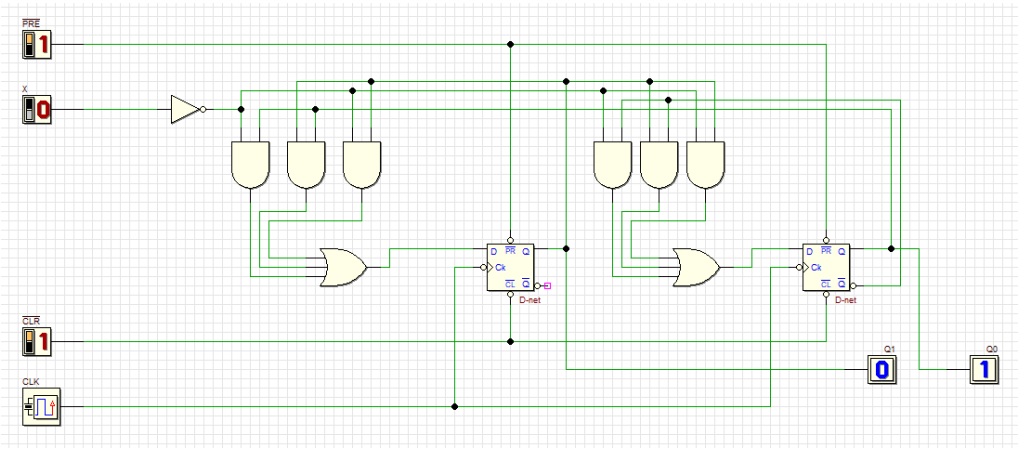
D0 = $\overline{X}$ $\overline{Q0}$ + Q1$\overline{Q0}$ + $\overline{X}$Q1

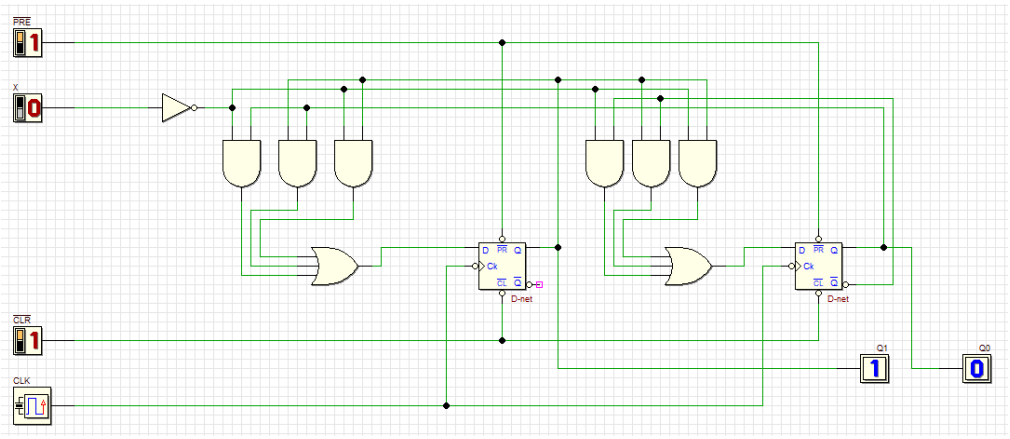
c)



d)


PRE
1
X
0
CLR
1
CLK
D-net
D-net
Q1
0
Q0
0


PRE
1
X
0
CLR
1
CLK
D-net
D-net
Q1
0
Q0
1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CLR
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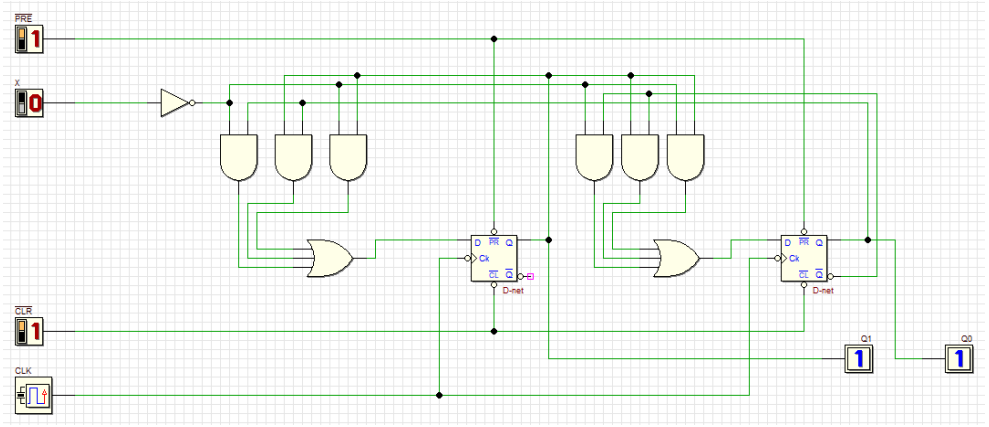
CLK
D-net
D-net
Q1
1
Q0
0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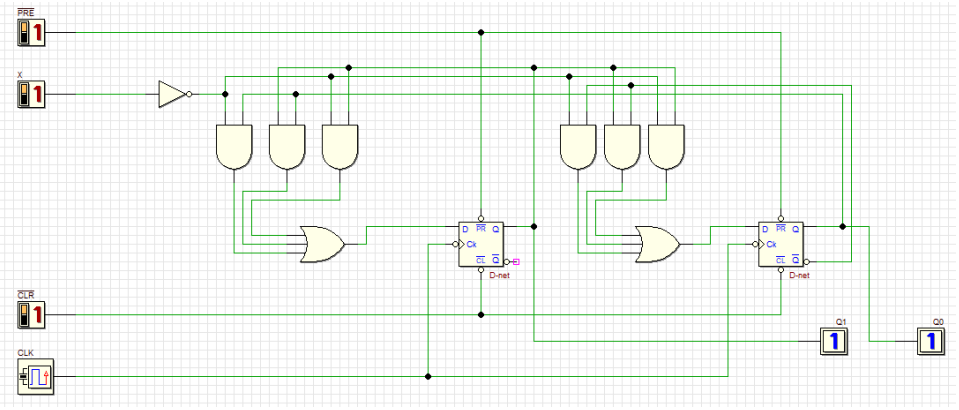
CLK
D-net
D-net
Q1
1
Q0
1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CLR
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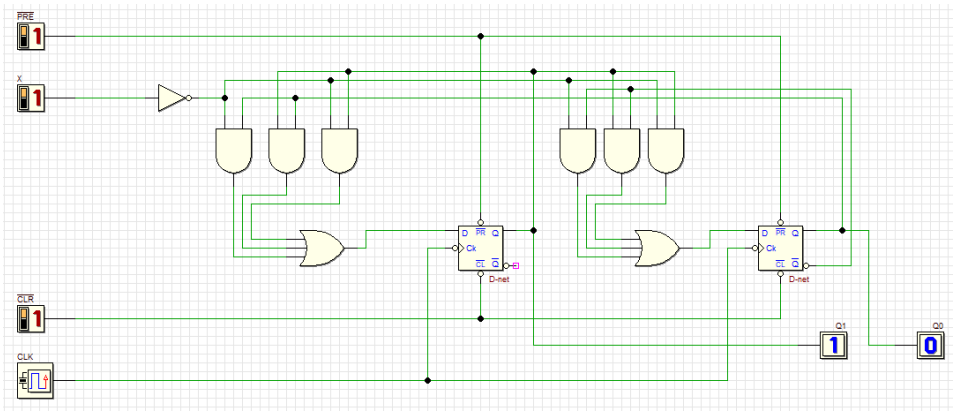
Ck
CL
D-net
Q1
1
Q0
1


PRE
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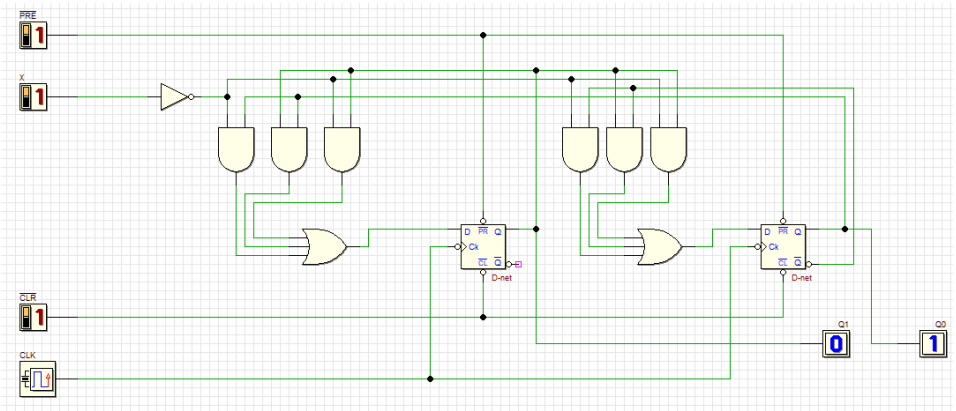
X
1
CLR
1
CLK
D
PR
Q
Ck
CL
D-net
Q1
1
Q0
0


PRE
1
X
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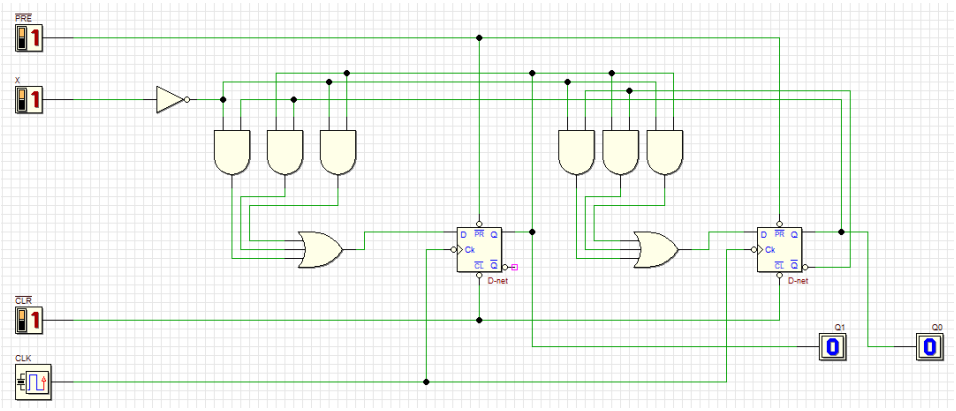
CLR
1
CLK
D
PR
Q
Ck
CL
D-net
Q1
0
Q0
1

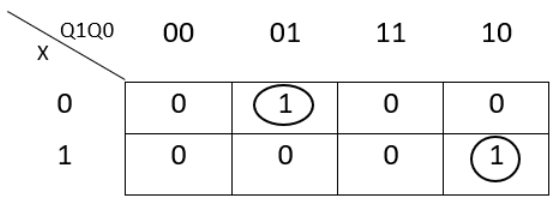

PRE
1
X
1
CLR
1
CLK
D
PR
Q
Ck
CL
D-net
Q1
0
Q0
0

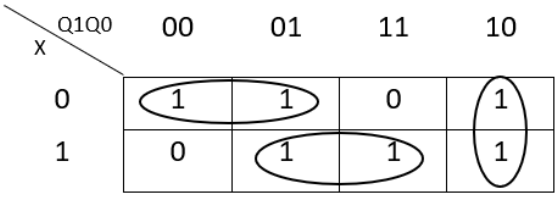
7) Repeat steps in Q(6) using T flip-flop

a) Built the next state and transition table using the header in Table 4.

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

b) Get the optimized Boolean expression

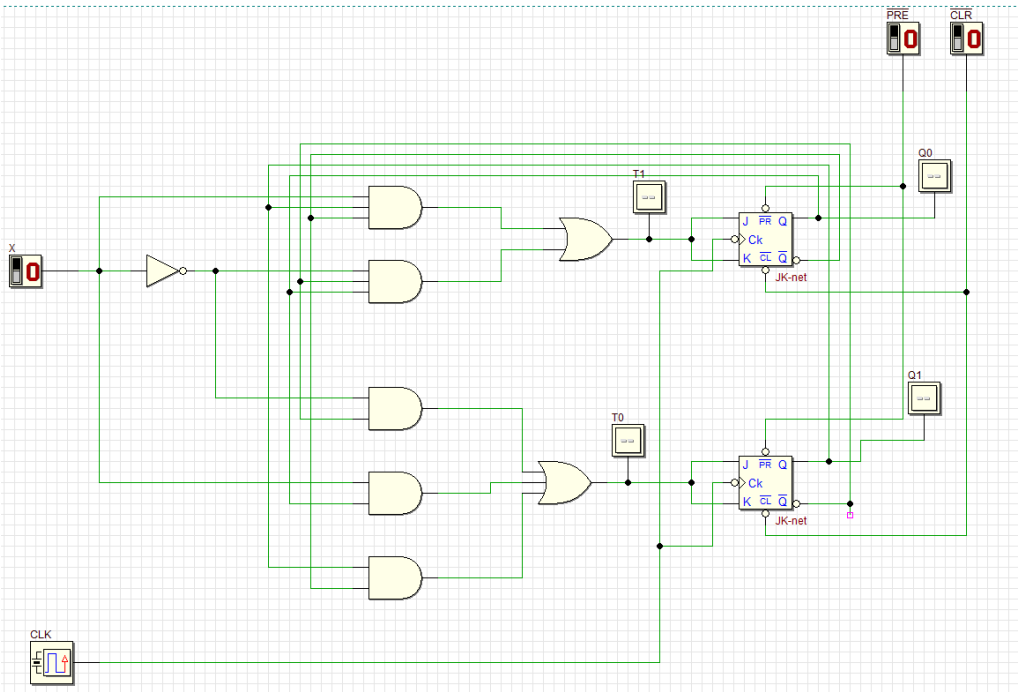




$T1=\overline{X}\,\overline{Q1}Q0 + XQ1\overline{Q0}$

$T0=\overline{X}\,\overline{Q1} + XQ0 + Q1\overline{Q0}$

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 4 is correct.