DIGITAL LOGIC, SECR1013
LAB-2

Members:
MD SIRAJUM MUNEER (A20EC4035)
MD MAHI ANAN (A19EC4050)

Part-1:

1. GIVEN , Y=$AB+BC+AC$

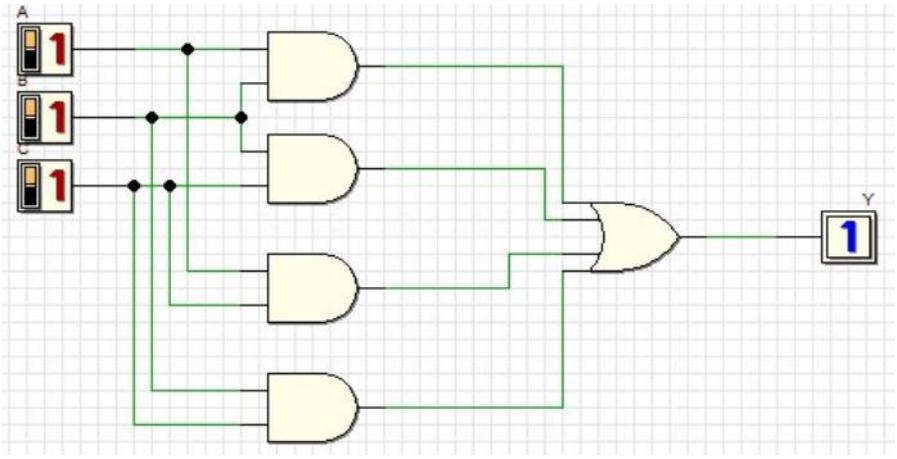
   Converting to the standard form,

Y=AB+AC+AC
=AB(C+$\bar{C}$)+BC(A+A)+(AC)(B+B)
=ABC+AB$\bar{C}$+ABC+B$\bar{C}$A+CAB+AC$\bar{B}$
=ABC+$\bar{A}$BC+ABC+ABC

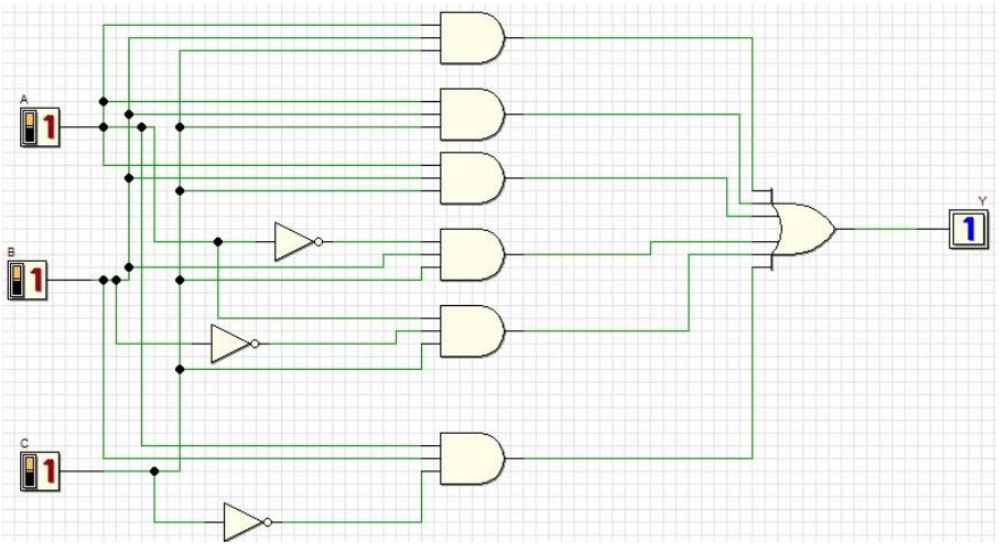
2. Truth Table on standard expression :

INPUT			***OUTOUT***
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. (a) Circuit for non-standard form (Q1)



(b) Circuit on non standard form (in answer from question 2)



4. Truth Table for Non-standard and Standard form:

Circuit-1:

INPUT			*OUTPUT*
A	B	C	*Y*
0	0	0	*0*
0	0	1	*0*
0	1	0	*0*
0	1	1	*1*
1	0	0	*0*
1	0	1	*1*
1	1	0	*1*
1	1	1	*1*

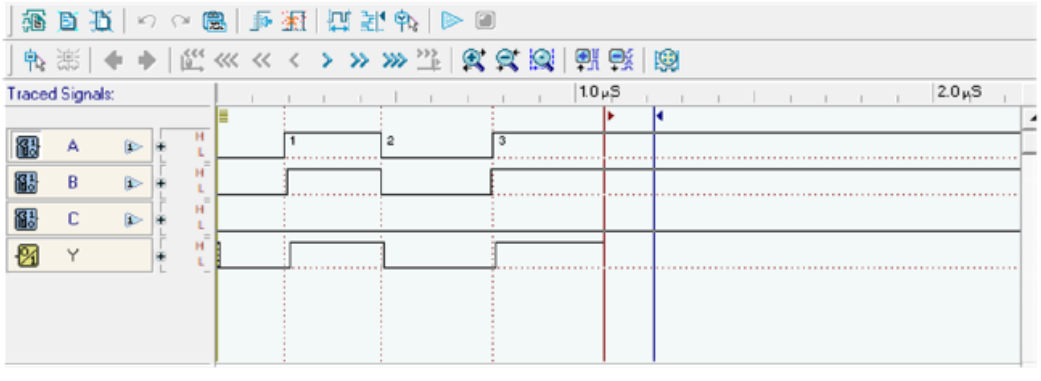
0	0	0	*0*
0	0	1	*0*
0	1	0	*0*
0	1	1	*1*
1	0	0	*0*
1	0	1	*1*
1	1	0	*1*
1	1	1	*1*

Circuit-2:

INPUT			*OUTPUT*
A	B	C	*Y*

Conclusion : It can be seen that ,the two tables of output from circuit 1 and circuit is is totally same but the forms are different

5.



Part 2

Combinational circuit design process and simulate with Deeds Simulator.

Design Process

i) Determine Parameter Input / Output and their relations.
ii) Construct Truth Table. iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.
iv) Draw the circuit and use duality symbol; convert AND-OR circuit to NAND gates ONLY.
v) Simulate the design using Deeds Simulator. Check the results according to Truth Table and Timing Diagram Operation.

Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.

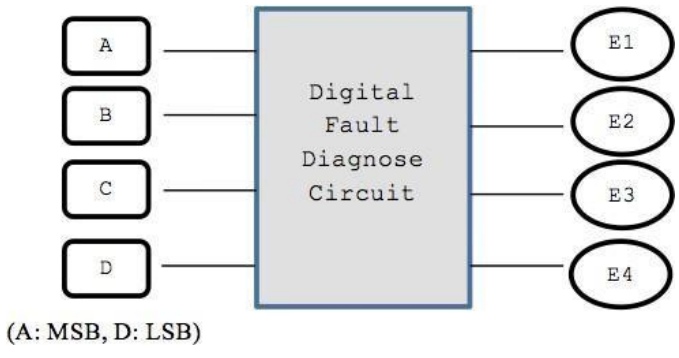


Figure 5

The following rules are used to activate the error's signal type:

RULE 1: E1 is activated if the input number is positive ODD and the majority of the bits is '0'.
RULE 2: E2 is activated if the input number is positive EVEN and the majority of the bits is '0'.
RULE 3: E3 is activated if the input number is negative ODD and the majority of the bits is '1'.
RULE 4: E4 is activated if the input number is negative EVEN and the majority of the bits is '1'.
RULE 5: The output of error signal is invalid if the input has equal bit '0' and bit '1'.
(**NOTE:** Positive ODD is positive numbers that are odd and negative EVEN is negative numbers that are even).

Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0

0	0	1	0	0	1	0	0
0	0	1	1	x	x	x	X
0	1	0	0	0	1	0	0
0	1	0	1	x	x	x	X
0	1	1	0	x	x	x	x
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	x	x	x	X
1	0	1	0	x	x	x	x
1	0	1	1	0	0	1	0
1	1	0	0	x	x	x	x
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.

AB \ CD	00	01	11	10
00	E2 (i)	E1 (i)	X	E2
01	E2 (i)	X		X
11	X	E3 (i)	E3 (1)	E4 (i)
10	0	X	E3 (i)	X

$E1 = \overline{A}\,\overline{B}\,\overline{C}\,D$

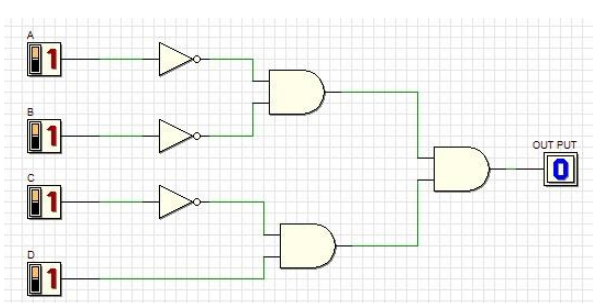
$E2 = A\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,C\overline{D}$

$E3 = ABD + A\overline{B}\,CD$

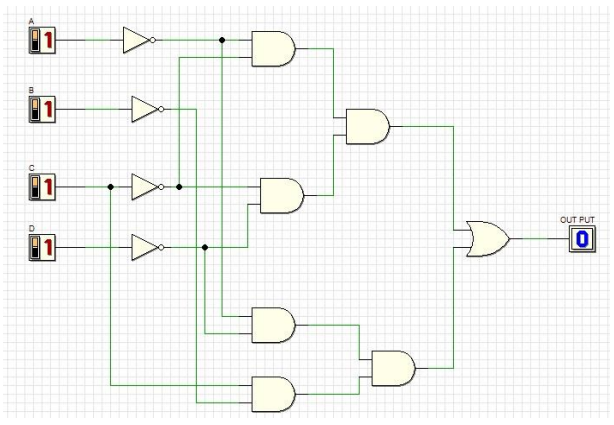
$E4 = ABC\overline{D}$

3.From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.

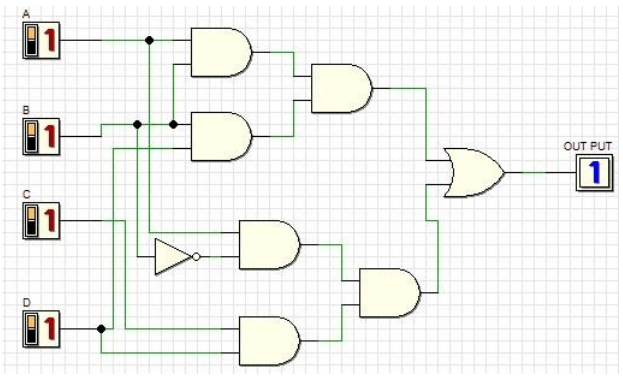
E1:



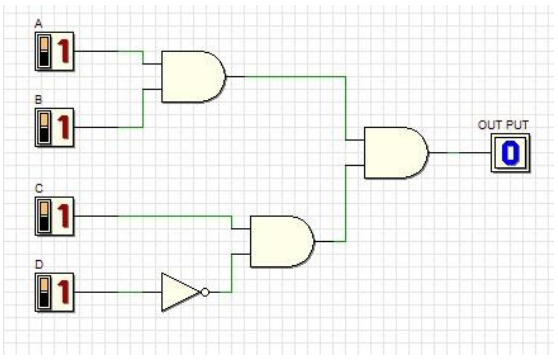
E2:



E3:



E4:



4.Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

Truth Table 2

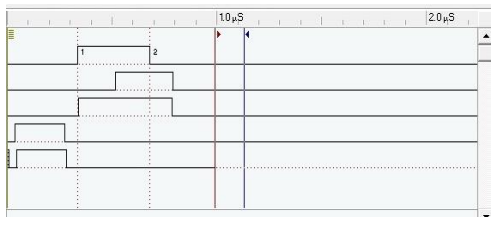
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

Conclusion : we can see that ,the output in the both of the truth tables are same and they have same outputs.

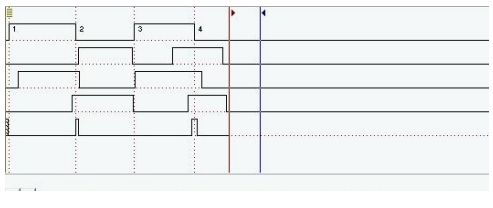
b) Timing Diagram:

E1:

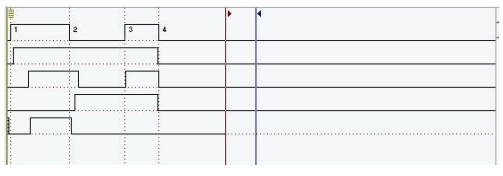


E2:

E3:



E4:



Explain some analysis values based on your timing diagram:

For E1: only input d value has an output

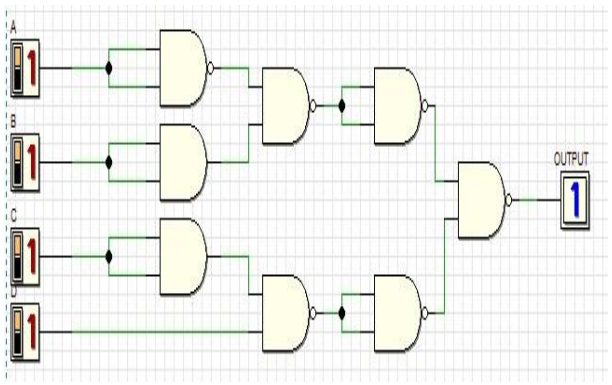
E2: if all the input is low then all the outputs will be high .

E3:if all the input is high then all the output is high

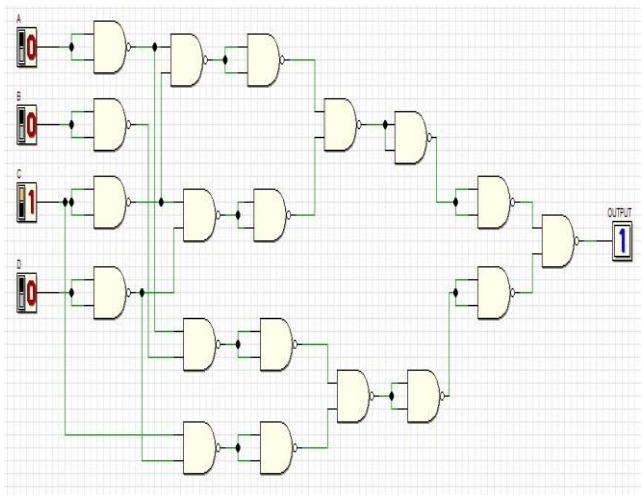
E4: if the input for A, B, C is high and D is low then the output will be High.

5.Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.

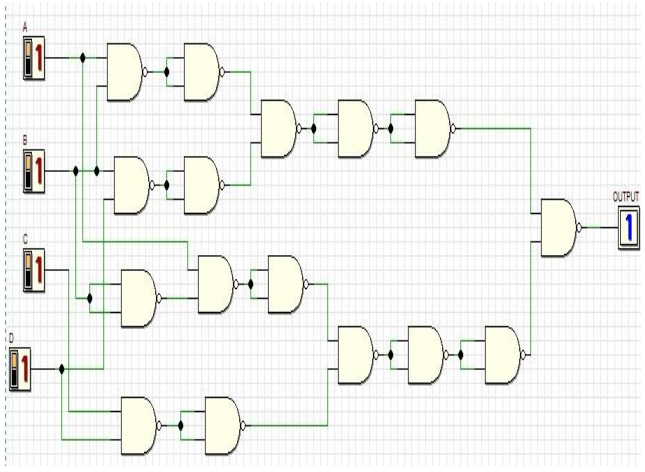
E1:



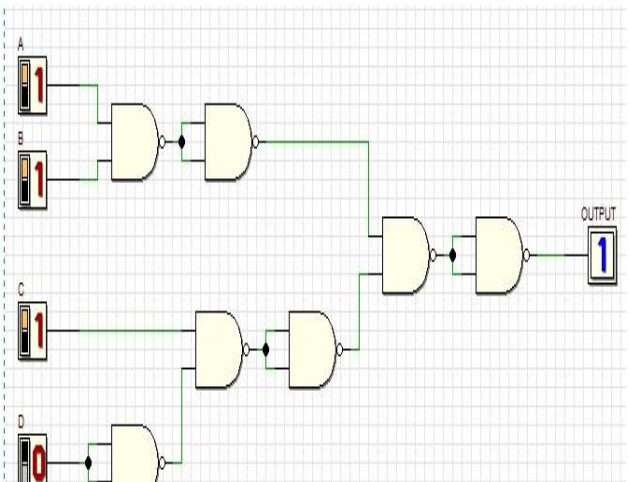
E2:



E3:



E4:



6.Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

Truth Table 3

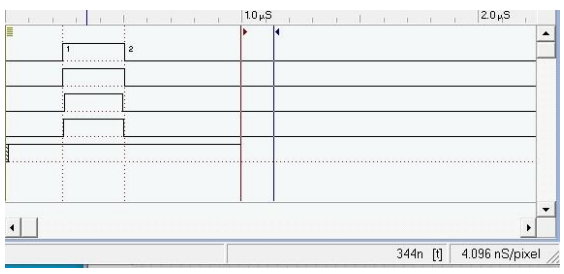
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	x	x	x	X
0	1	0	0	0	1	0	0
0	1	0	1	x	x	x	X
0	1	1	0	x	x	x	x
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	x	x	x	X
1	0	1	0	x	x	x	x
1	0	1	1	0	0	1	0
1	1	0	0	x	x	x	x
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

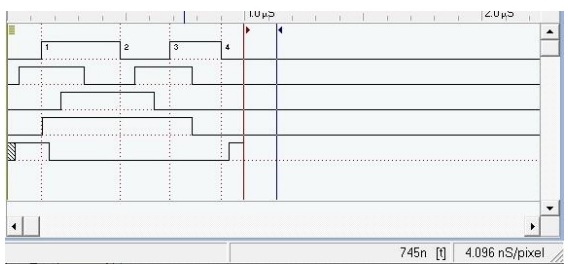
Ans : all the same because nand gates are universal gates.

b) Timing Diagram

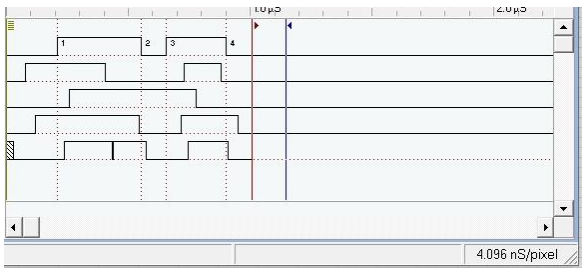
E1:



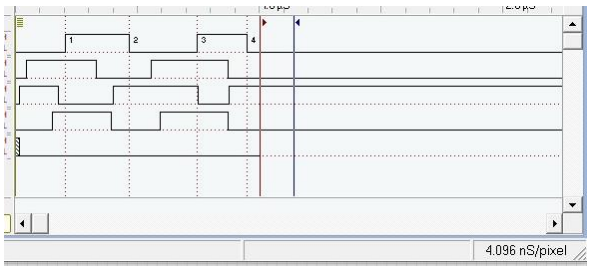
E2:



E3:



E4:



Explanation: we can see that the output of E1 and E2 is low when most of the input is low.