Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT : SCSR1013 DIGITAL LOGIC

SESSION/SEM : 2020/2021- Sem 1

LAB 2 : COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION

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REMARKS :

MARKS:

Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y=AB+BC+AC$$

1. Convert the non-standard Boolean expression into standard form.

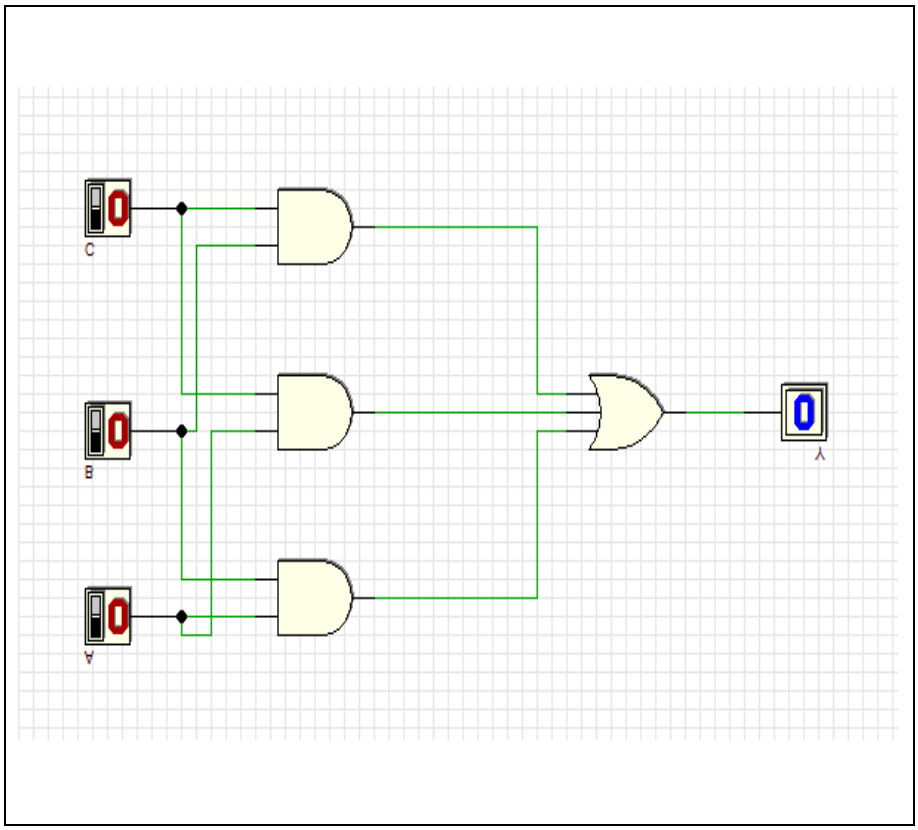
Y = AB + BC + AC
Term 1 = AB (C + C')
= ABC + ABC'
Term 2 = BC (A + A')
= BCA + BCA'
Term 3 = AC (B + B')
= ACB + ACB'
Therfore: ABC + ABC' + BCA + BCA' + ACB + ACB'
= ABC + A'BC + AB'C + ABC' , (rule 5).

2. Based on standard form expression, complete the following truth table.

INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

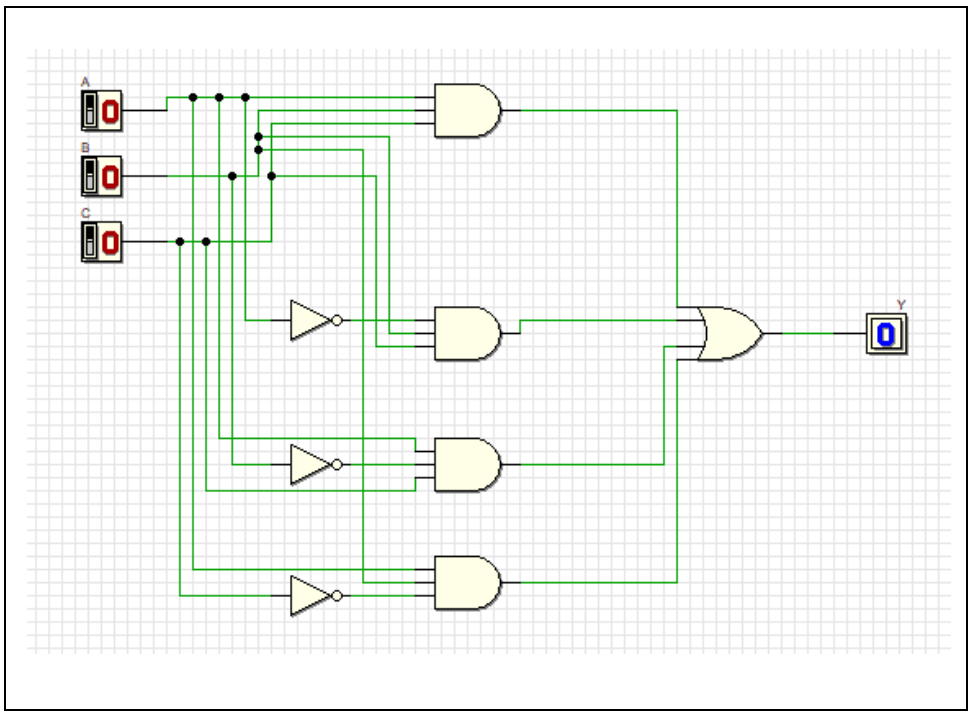
3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Circuit (i)

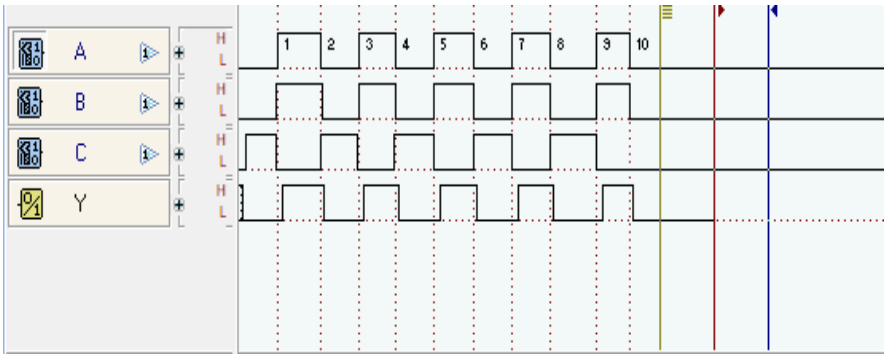
Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Circuit (ii)

Conclusion:

Circuit (i) is non-standard form while circuit (ii) is standard form.
There are no difference for the output in truth table as it is actually the same input and same process, only the expression is the difference.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



Part 2

Combinational circuit design process and simulate with Deeds Simulator.

Design Process

i) Determine Parameter Input / Output and their relations.
ii) Construct Truth Table.
iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.
iv) Draw the circuit and use duality symbol; convert AND-OR circuit to NAND gates ONLY.
v) Simulate the design using Deeds Simulator. Check the results according to Truth Table and Timing Diagram Operation.

Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.

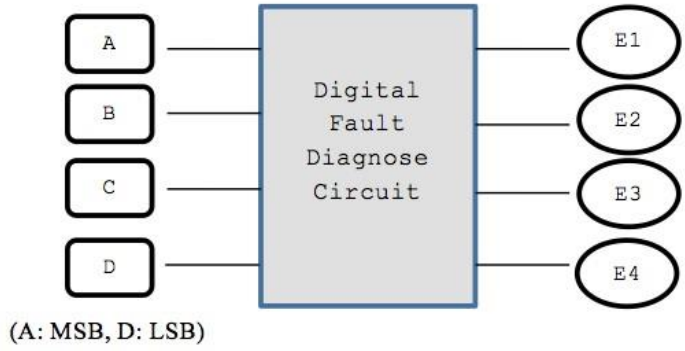


Figure 5

The following rules are used to activate the error's signal type:

RULE 1: E1 is activated if the input number is positive ODD and the majority of the bits is '0'.

RULE 2: E2 is activated if the input number is positive EVEN and the majority of the bits is '0'.

RULE 3: E3 is activated if the input number is negative ODD and the majority of the bits is '1'.

RULE 4: E4 is activated if the input number is negative EVEN and the majority of the bits is '1'.

RULE 5: The output of error signal is invalid if the input has equal bit '0' and bit '1'.

(**NOTE:** Positive ODD is positive numbers that are odd and negative EVEN is negative numbers that are even).

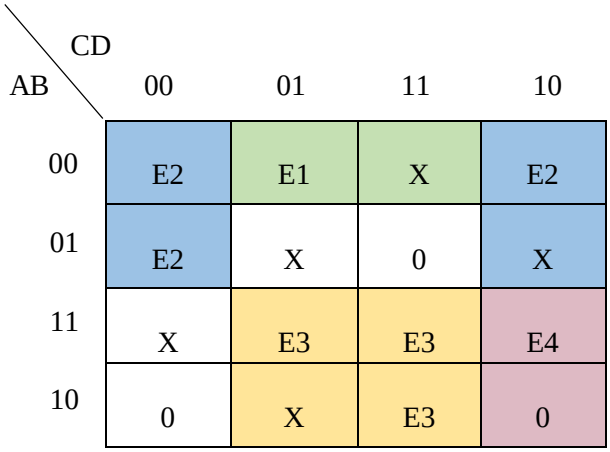
Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 1

INPUTS				**OUTPUTS**			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.



AB \ CD	00	01	11	10
00	E2	E1	X	E2
01	E2	X	0	X
11	X	E3	E3	E4
10	0	X	E3	0

E1:

0 0 0 1
0 0 1 1
A'B'D

E2:

0 0 0 0
0 1 0 0
0 0 1 0
0 1 1 0
A' D'

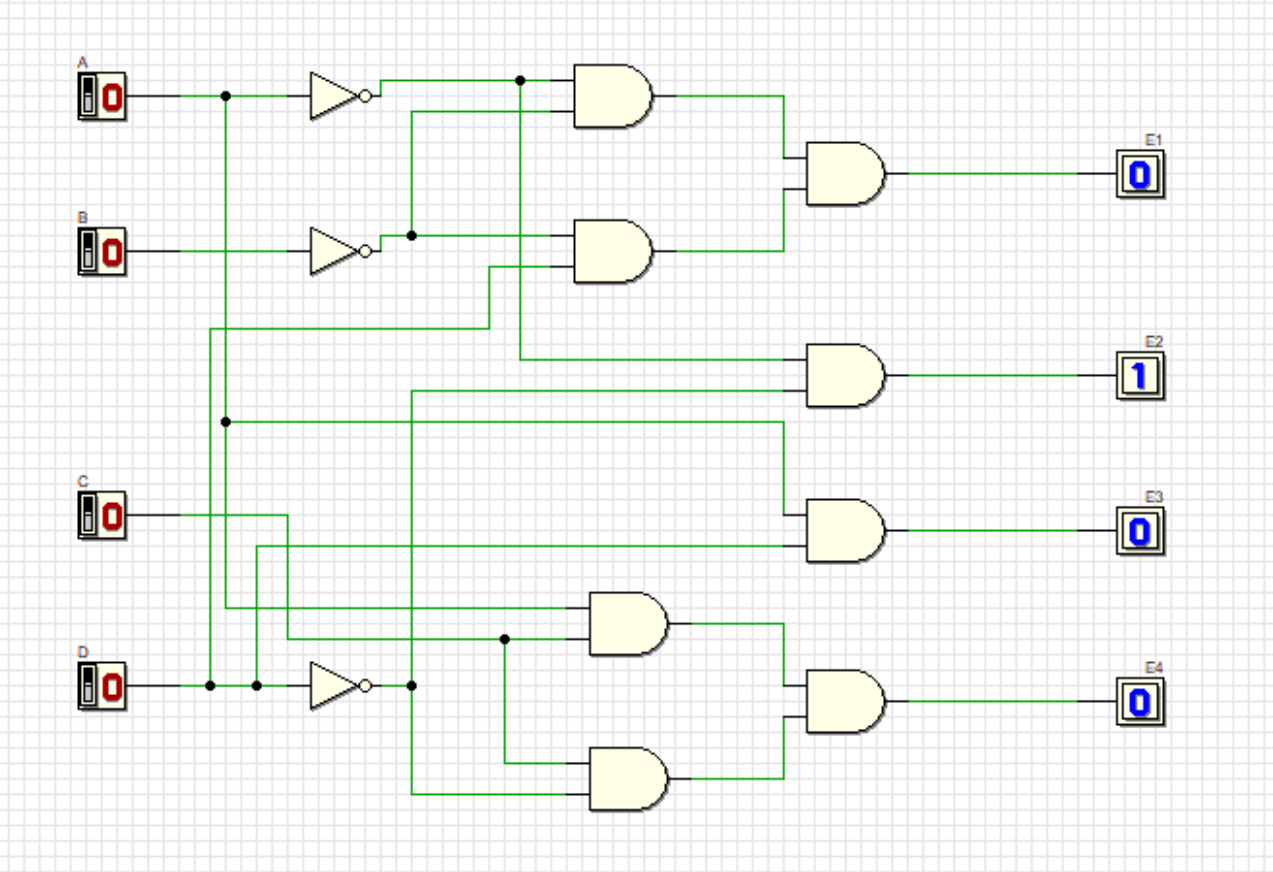
E3:

1 1 0 1
1 0 0 1
1 1 1 1
1 0 1 1
A D

E4:

1 1 1 0
1 0 1 0
A CD'

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

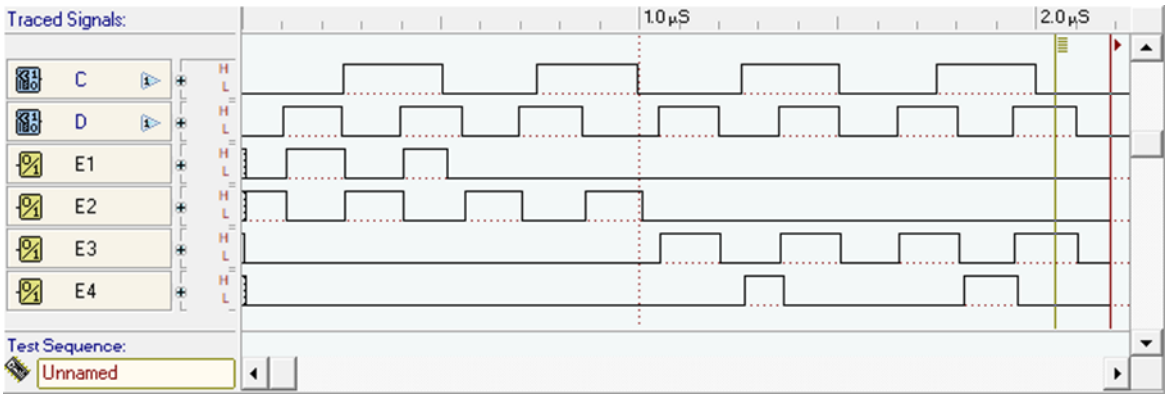
Truth Table 2

INPUTS				**OUTPUTS**			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

The output are same either before or after minimize SOP boolean expression. The process also use X as dont care method to get the output. Therefore, truth table 1 and 2 are same as the process anf the input also same.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

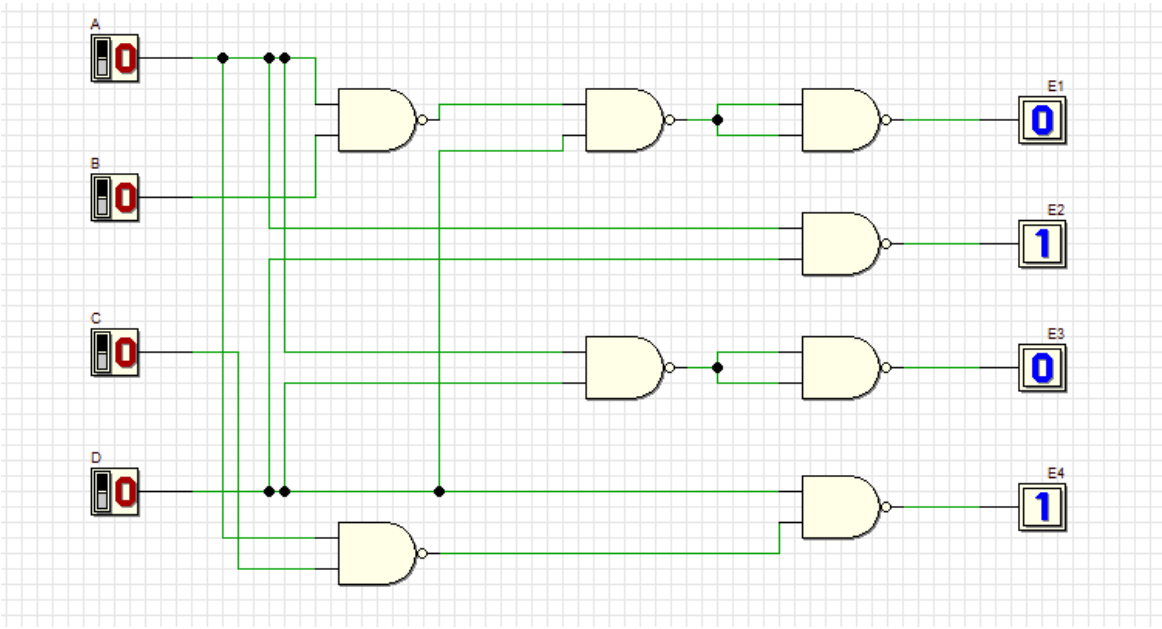
E1: The output will be high only when the input ABCD is 0001 and 0011. Other than that, the output is low.

E2: The output is high when the input ABCD is 0000, 0010, 0100, 0110, otherwise it is low.

E3: The output will be high when the input ABCD is 1001, 1011, 1101 and 1111. Other than that, the output is low.

E4: The output is high when the input ABCD is 0110 and 1110, otherwise it is low.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

Truth Table 3

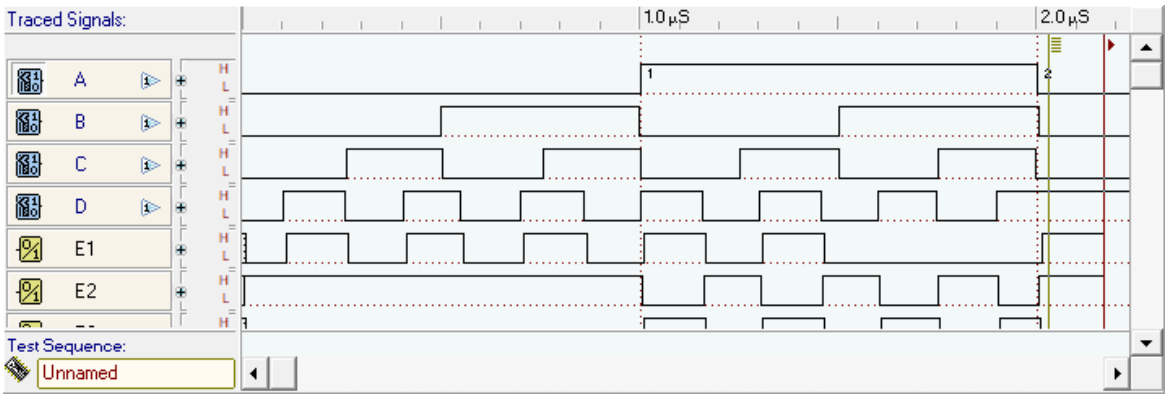
INPUTS				**OUTPUTS**			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

Conclusion:

NAND gate is a universal gate, so the output are still the same.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

The output is still the same, E1 produce high output only when the input is 0001 and 0011. For E2, it only produce high output for 0000, 0010, 0100 and 0110. Same goes to E3 when the input is 1001, 1011, 1101, and 1111. Last for E4, the output is high for 0110 and 1110. So the ttiming diagram is same as before we change to universal gate.

Fully ☐ Partially Completed ☐

Completed Checked by: _____