School of Computing
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SUBJECT : SECR1013 DIGITAL LOGIC

SESSION/SEM : 20202021/1

LAB 3 : SYNCHRONOUS DIGITAL COUNTER

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Lab #3

A. Preliminary Works

1) Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	J	K	CLK	Q
Set initial value Q = 1	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	⇓	1
Output Q become 0, no change in asynchronous input	1	1	0	1	⇓	0
Output Q is not the previous Q	1	1	1	1	⇓	1
RESET Q	1	1	0	1	⇓	0
SET Q	1	1	1	0	⇓	1

2) Answer all questions.

a) Which state that JK flip-flop has, but not on SR flip-flop.

When both the input J & K are 1,Jk flip-flop has a toggle state which Sr flip-flop does not have.

b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

It is a negative edge triggered flip-flop.

B. Lab Activities

1) You are given a counter circuit as shown in Figure 4.

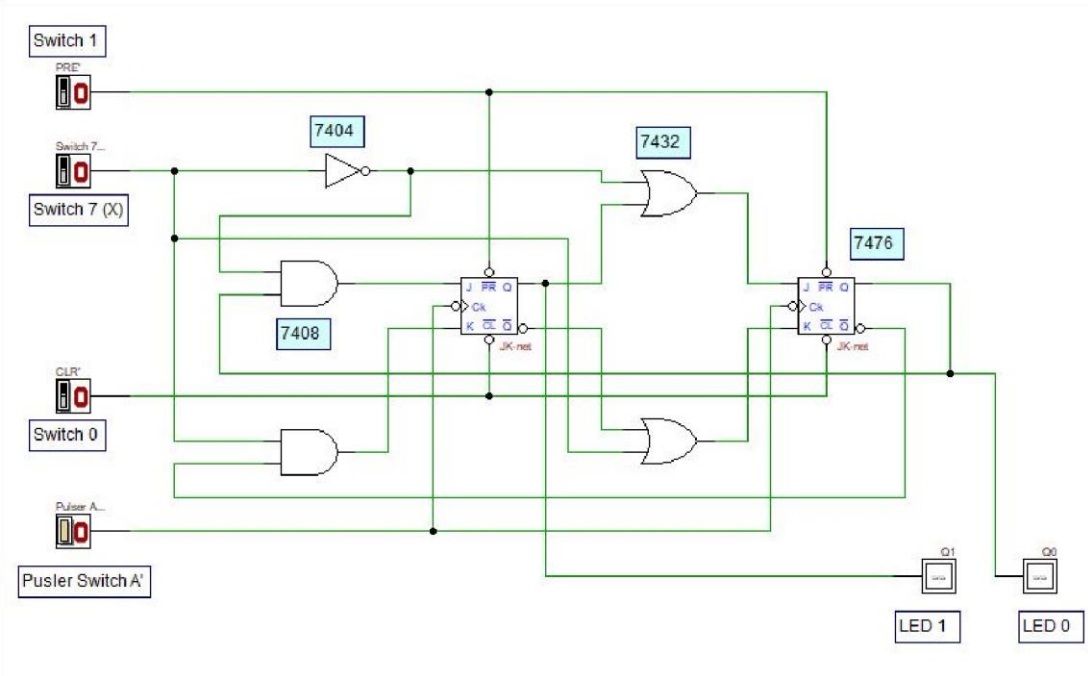
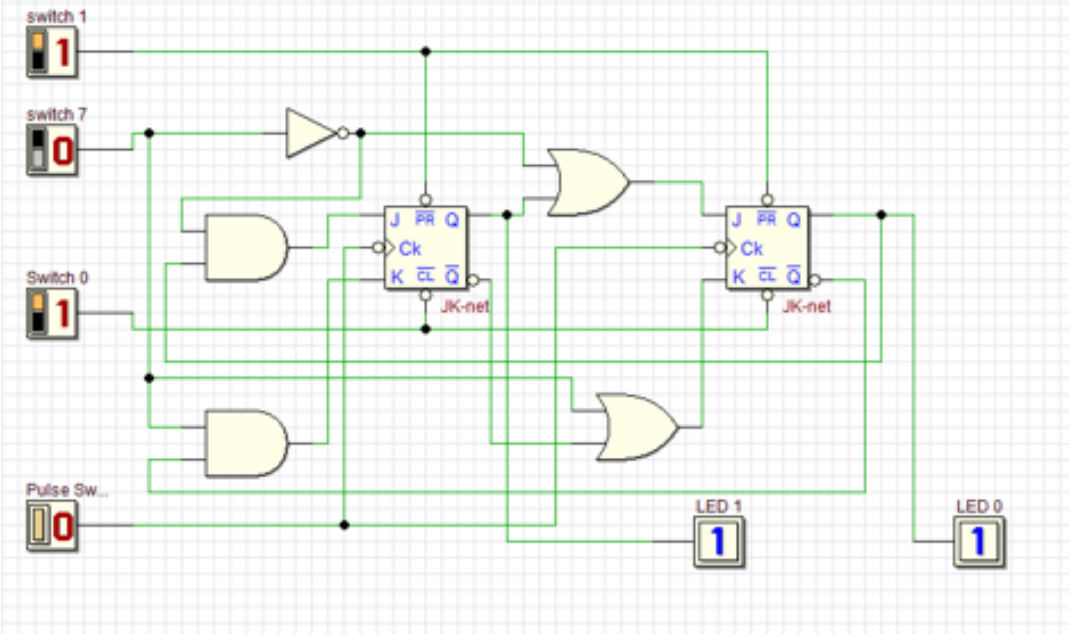


Figure 4: A Synchronous Counter Circuit

2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).

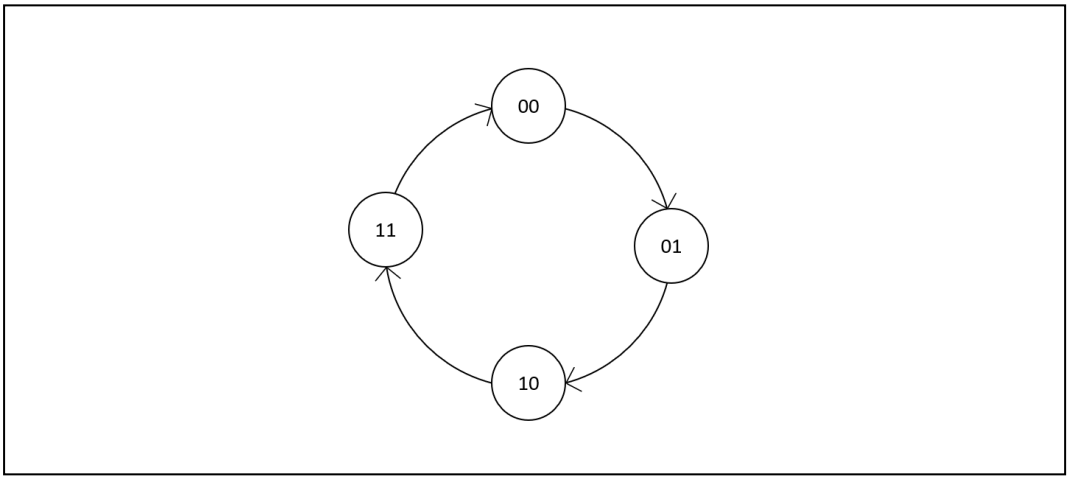


3) Investigate the behavior of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the *NextState* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state.
(0=LOW, 1=HIGH)

Table 2

Switch 7	**Present State**		**Next State**	
X	**Q1 LED 1**	**Q0 LED 0**	**Q1 LED 1**	**Q0 LED 0**
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?

It uses clock inputs to synchronize the circuit operation and all clock are from the same source.

b) How many states are available for the counter and what are they?

4 states : 00, 01, 11, 01

c) What is the function of Switch 7 (X) in the circuit?

As clock input

d) What is the function of Switch 0 and Switch 1 in the circuit?

As positive or negative edge (CLK)

e) Is the counter a saturated counter or recycle counter?

Saturated counter

6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3

Table 3

Input X	**Present State**		**Next State**		**D FF Transition**	
	Q1	**Q0**	**Q1+**	**Q0+**	**D1**	**D0**
0	0	0	0	1	0	1
1	0	0	0	0	0	0
0	0	1	1	0	1	0
1	0	1	0	0	0	0
0	1	0	1	1	1	1
1	1	0	0	1	0	1
0	1	1	1	1	1	1
1	1	1	1	0	1	0

b) Get the optimized Boolean expression.

D1:

Q1 \ Q0X	00	01	11	10
0				1
1	1		1	1

D1= $Q1Q0 + Q1\bar{X} + Q0\bar{X}$

D1= $Q1(Q0 + \bar{X}) + Q0\bar{X}$

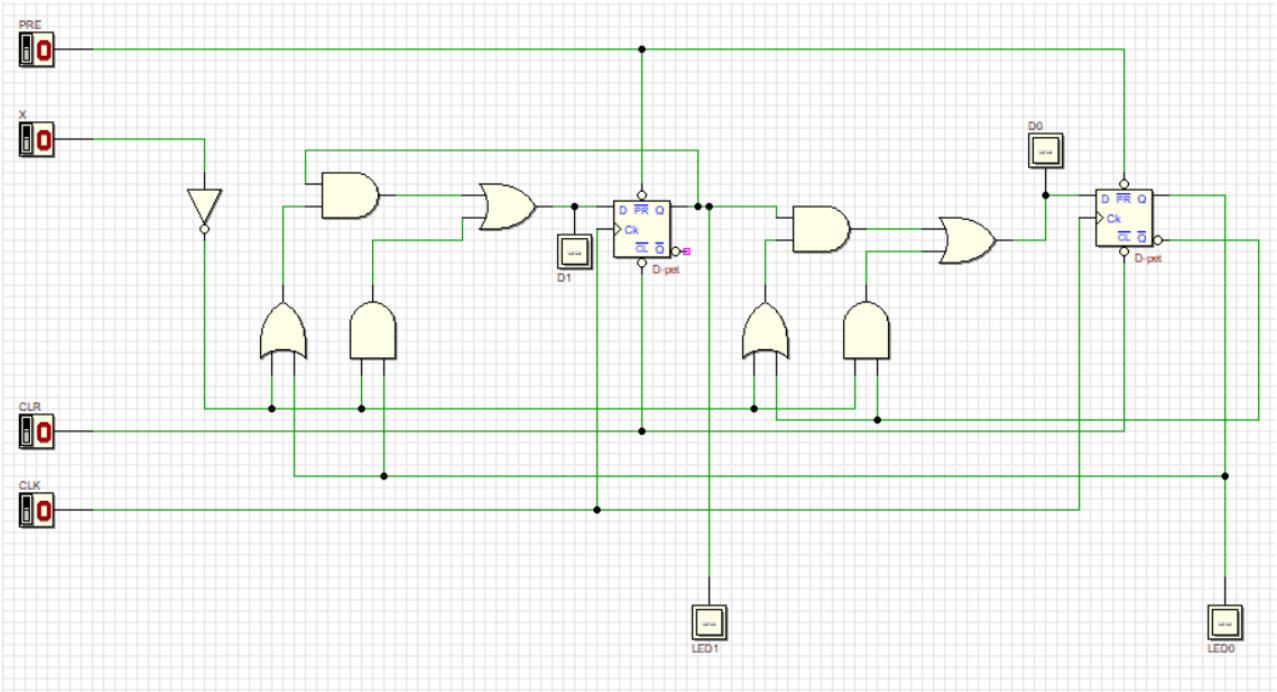
D0:

Q1 \ Q0X	00	01	11	10
0	1			
1	1	1		1

D0= $Q1\overline{Q0} + \overline{Q1}\bar{X} + \overline{Q0}\bar{X}$

D0= $Q1(\overline{Q0} + \bar{X}) + \overline{Q0}\bar{X}$

c) Draw the complete final circuit design in Deeds.
d) Simulate the circuit to prove that your Table 3 is correct.



7) Repeat steps in Q(6) using T flip-flop.

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
1	0	0	0	0	0	0
0	0	1	1	0	1	1
1	0	1	0	0	0	1
0	1	0	1	1	0	1
1	1	0	0	1	1	1
0	1	1	1	1	0	0
1	1	1	1	0	0	1

T1:

Q1 \ Q0X	00	01	11	10
0	**0**	**0**	**0**	**1**
1	**0**	**1**	**0**	**0**

T1= $\overline{Q0}XQ1 + Q0\overline{X}\overline{Q1}$

T0:

Q1 \ Q0X	00	01	11	10
0	**1**	**0**	**1**	**1**
1	**1**	**1**	**1**	**0**

T0= $\overline{Q1}\bar{X} + Q1\overline{Q0} + Q0X$