UTM
UNIVERSITI TEKNOLOGI MALAYSIA

SCHOOL OF COMPUTING
Faculty of Engineering

UNIVERSITI TEKNOLOGI MALAYSIA

SEMESTER 1, 2020/2021

LAB 2: COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION

SUBJECT	: SECR1013 DIGITAL LOGIC
SECTION	: 02
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SCHOOL	: SCHOOL OF COMPUTING
FACULTY	: FACULTY OF ENGINEERING
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Lab Activities

Part 1

1. $Y = AB + BC + CA$

$= AB(C + \bar{C}) + BC(A + \bar{A}) + CA(B + \bar{B})$

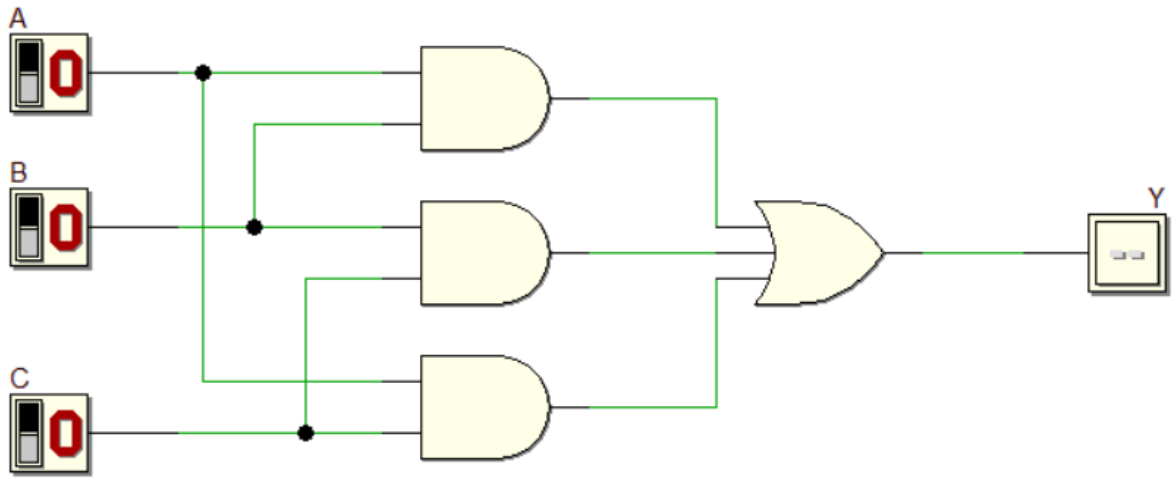
$= ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C$

$= ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$

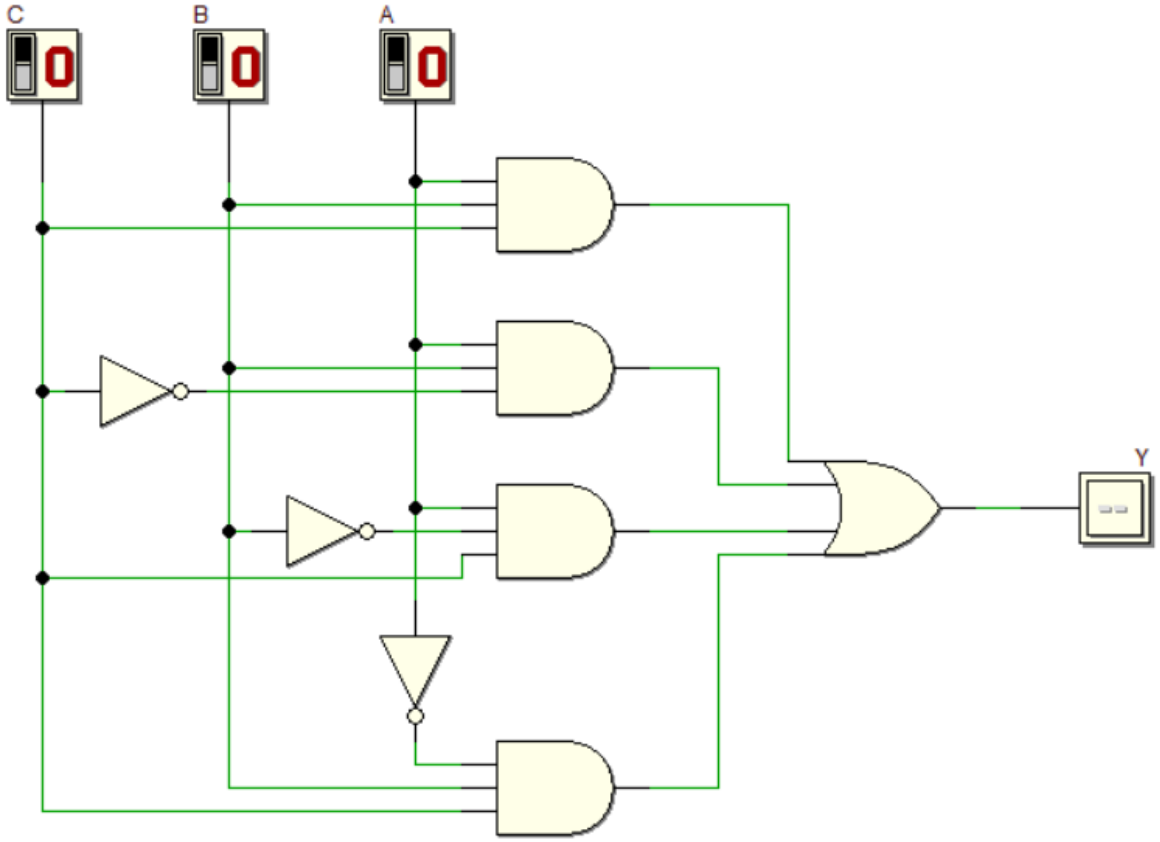
2.

Input			Output
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. a)



3. b)



4.

Circuit (i)

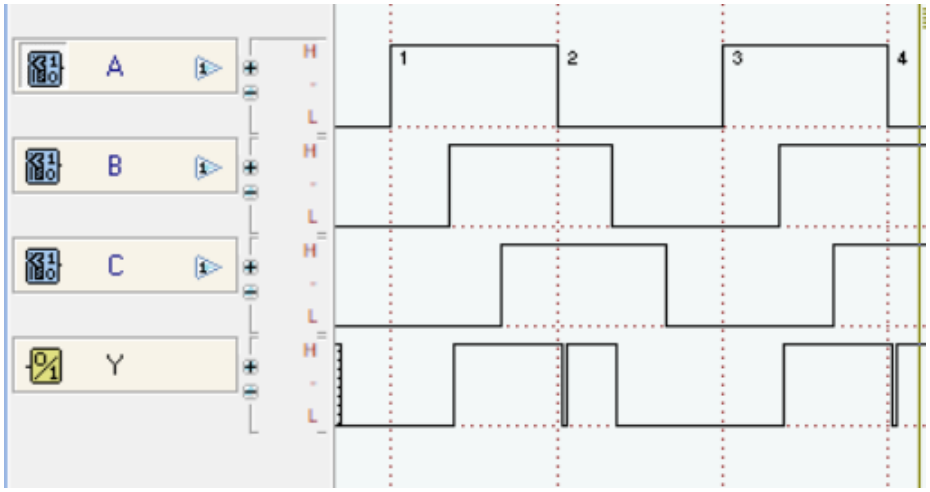
Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

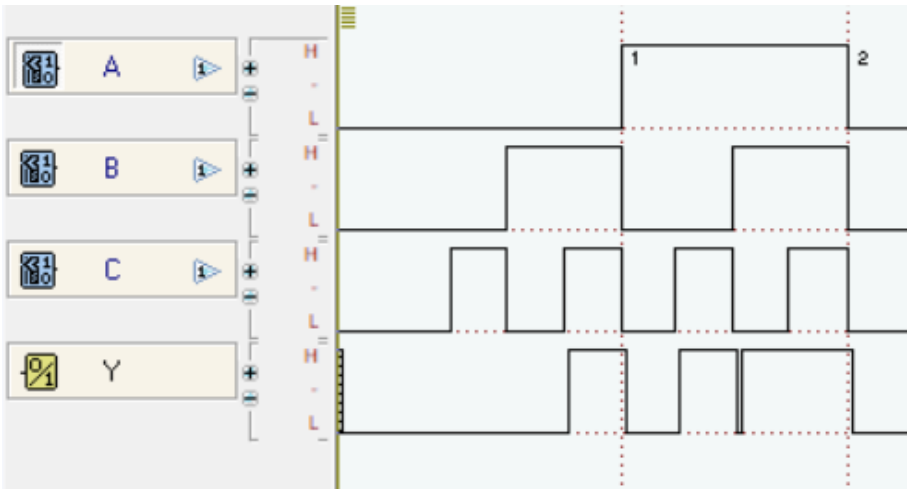
Circuit (ii)

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The results are the same. Circuit (i) is equivalent to Circuit (ii).

5.



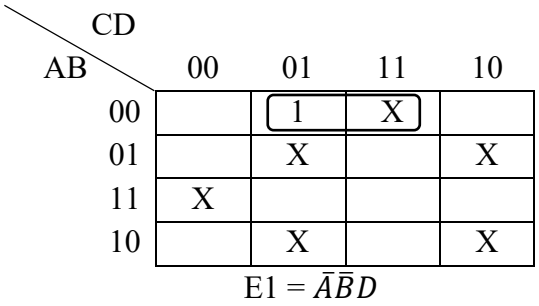


Part 2

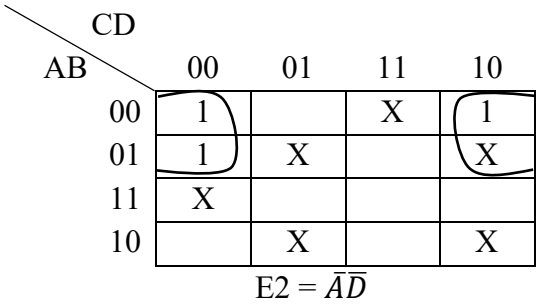
1. Truth Table 1

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

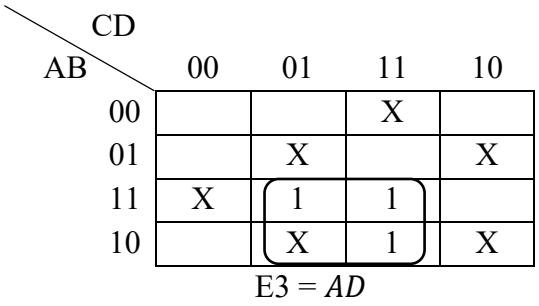
2.



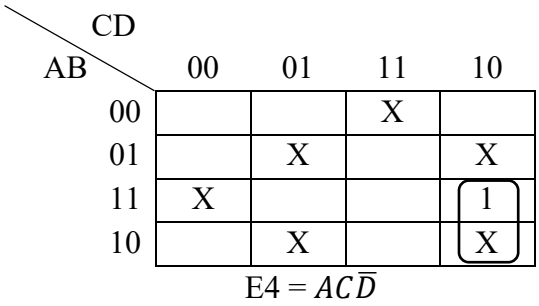
E1 = $\bar{A}\bar{B}D$



E2 = $\bar{A}\bar{D}$

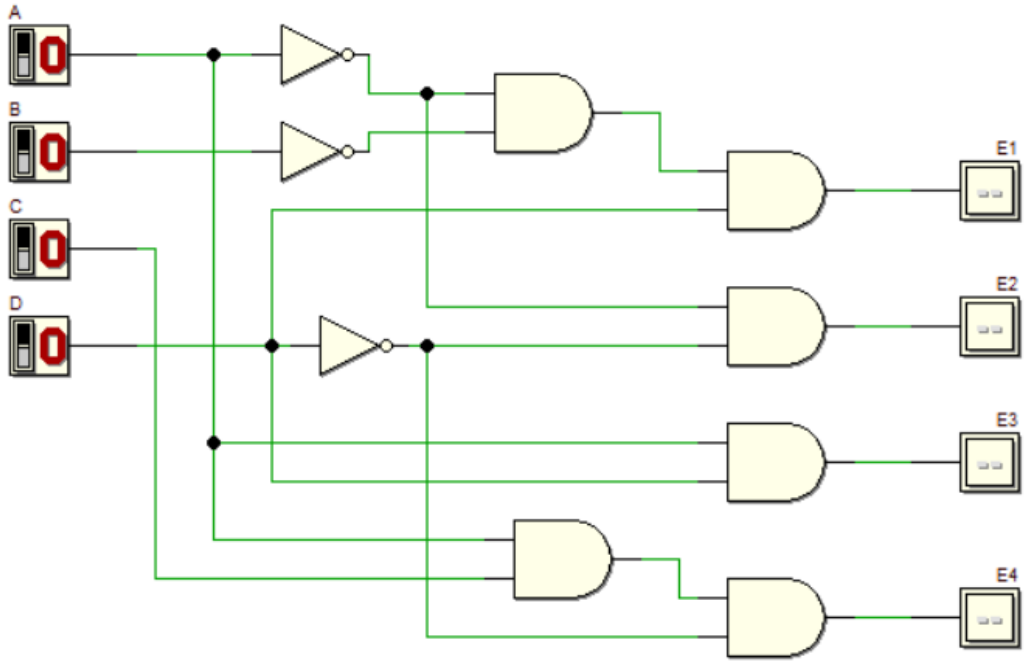


E3 = AD



E4 = $AC\bar{D}$

3.

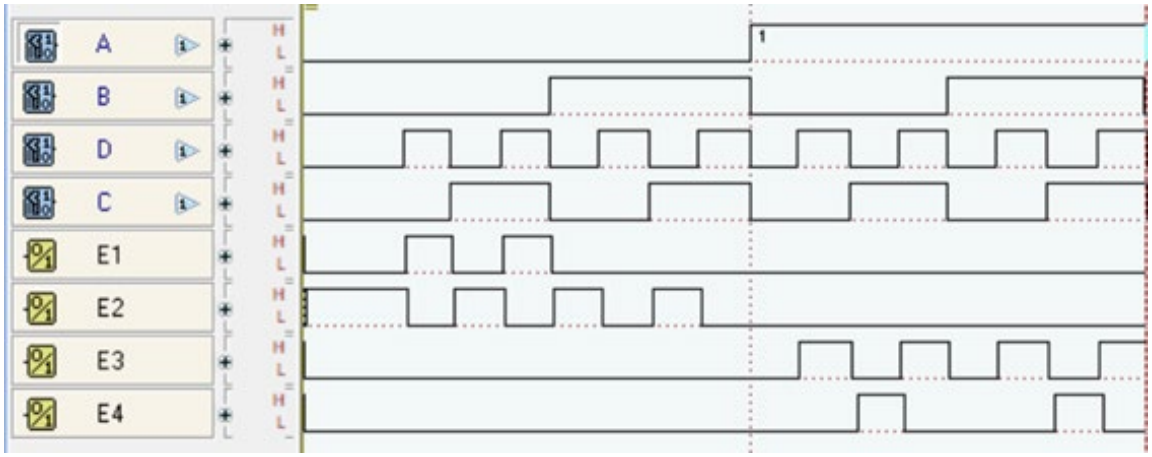


4. a) Truth Table 2

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

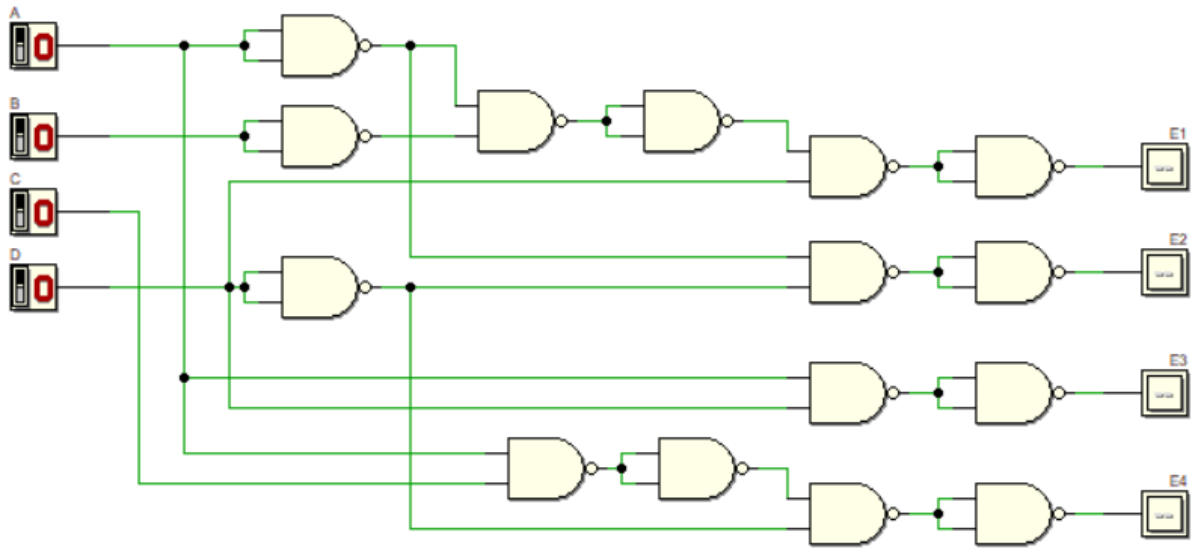
The output results are the same except for don’t cares. It can be used to represent the circuit.

4. b)



E1 and E2 are high only when A is high. E3 and E4 are high only when A is low.

5.

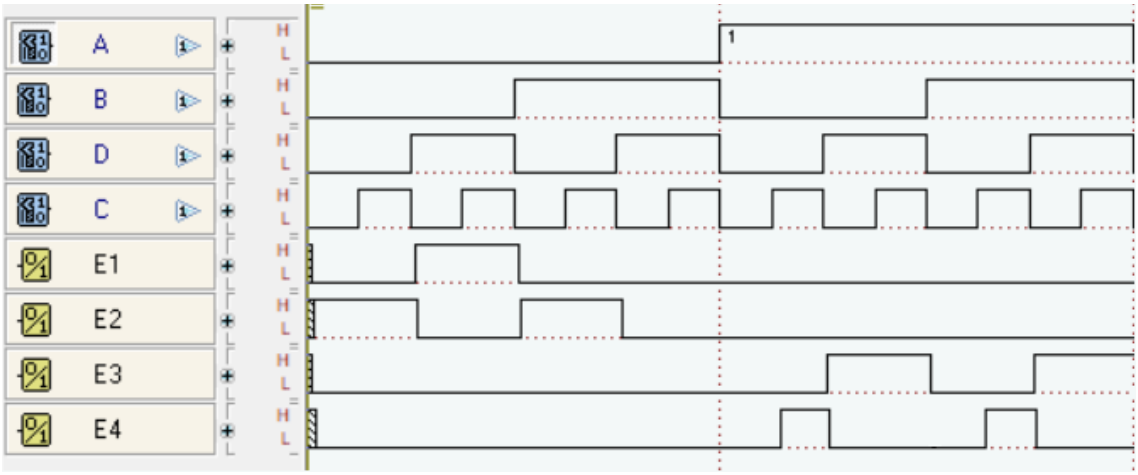


6. a) Truth Table 3

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

The output results are the same. NAND gate is a universal gate which can perform the function of basic gates and used to implement any logic circuits.

6. b)



When ABCD=0001, it is equivalent to 1, thus E1 is high because it is positive odd and the majority of the bits is ‘0’.
When ABCD=1110, it is equivalent to -1, thus E4 is high because it is negative even and the majority of the bits is ‘1’.