Preliminary Work

1.

AND

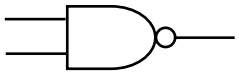
Symbol: 

IC Number: 7408

Truth Table 1

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND

Symbol: 

IC Number: 7400

Truth Table 2

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

2. *Truth Table 3*

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

3. $C = A\overline{B}$

$D = \overline{A}B$

$F = A\overline{B} + \overline{A}B$

4. *Truth Table 4*

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

Laboratory Work

Part 1

Truth Table 5

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table 5 matches the Truth Table 1 in the Preliminary Work.

Part 2

Truth Table 6

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

The output in Truth Table 6 and Truth Table 2 are the same. It can be concluded that Circuit 2 is equivalent to a single NAND gate.

Part 3

Truth Table 7

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

Circuit 3 can be represented by a single XOR gate.