UTM

UNIVERSITI TEKNOLOGI MALAYSIA

SEM 1 2020/2021: SECTION 01

Digital Logic

LAB 3

Students Information

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D. Preliminary Works

1) Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	**J**	**K**	**CLK**	**Q**
Set initial value Q = 1	0	0	X	X	--	1
Output Q stays the same	1	1	0	0	⇓	1
Output Q become 0, no change in asynchronous input	1	1	0	1	⇓	0
Output Q is not the previous Q	1	1	1	1	⇓	1
RESET Q	1	1	0	1	⇓	0
SET Q	1	1	1	0	⇓	1

2) Answer all questions.

a) Which state that JK flip-flop has, but not on SR flip-flop.
J=1, K=1

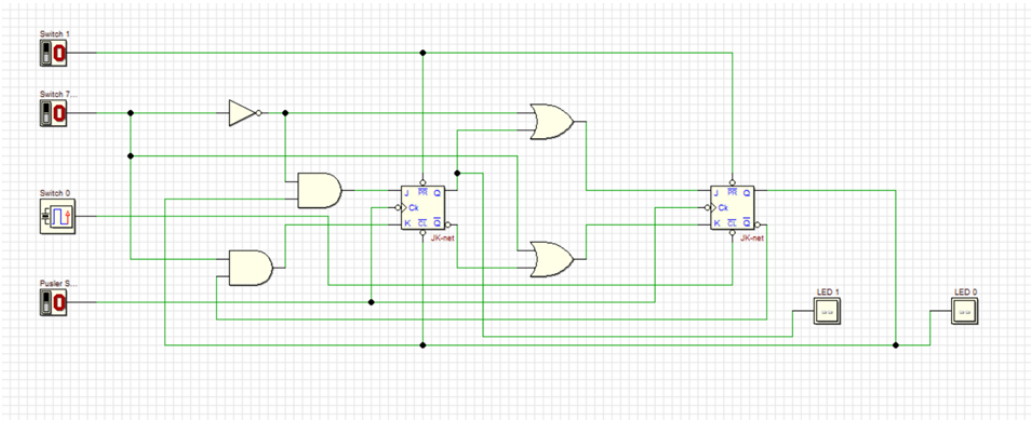
b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

Positive edge.

E. Lab Activities

1) You are given a counter circuit as shown in Figure 4.

2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).

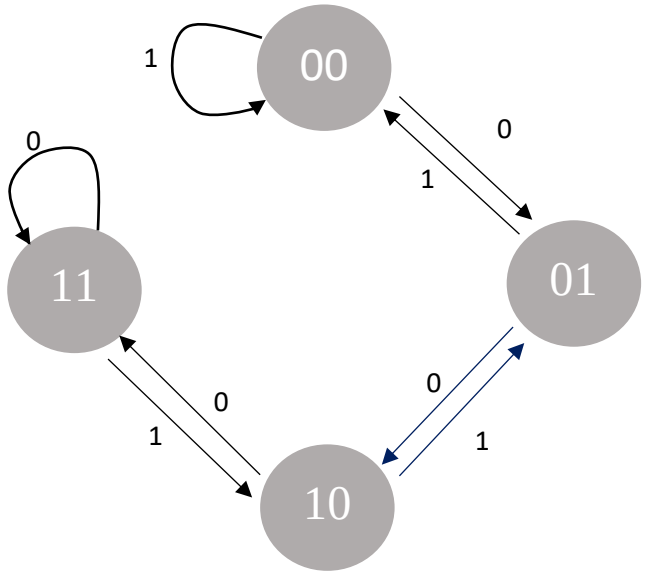


3) Investigate the behavior of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the Next State table of the counter in Table 2. Ensure the Switch 0 is in HIGH state. (0=LOW, 1=HIGH)

Table 2

Switch 7	Present State		Next State	
X	Q1 LED1	Q0 LED0	Q1 LED1	Q0 LED0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4) By referring to the Next-State in Table 2, sketch the state diagram of the counter.



5) By referring to the Next-State in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?
The clock input of the flip-flop. The J-K flip-flops are connected together at the same time by the same clock signal.

b) How many states are available for the counter and what are they?
There are 4 states that are available. 00, 01,10 and 11.

c) What is the function pf Switch 7 (X) in the circuit?
It acts an an up-down counter. The counter will count up or down.

d) What is the function of Switch 0 and Switch 1 in the circuit?
It acts as an asynchronous input. It has a control over the outputs. The inputs which are called preset (PRE) and clear (CLR) were put in a high state to allow a normal operation.

e) Is the counter a saturated counter or recycle counter?
The counter is a saturated counter. It is fixed when it reaches the limit.

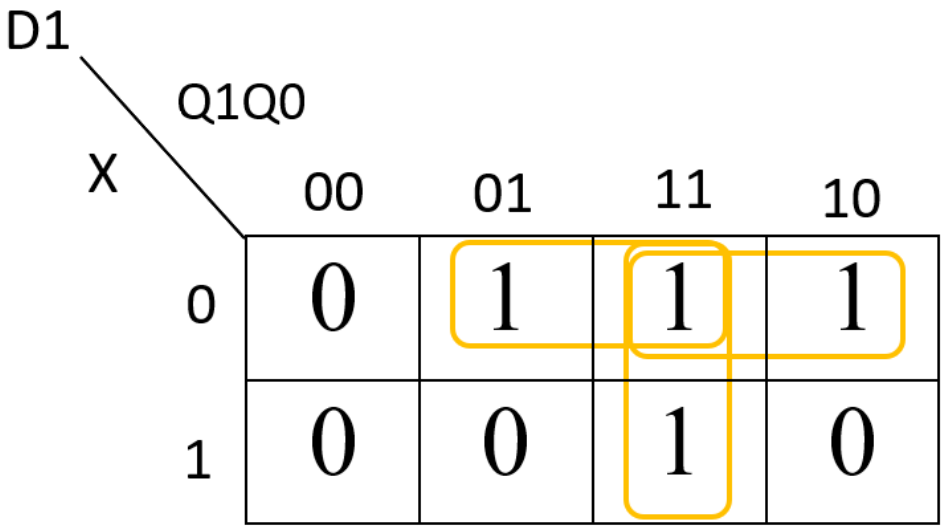
6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3.

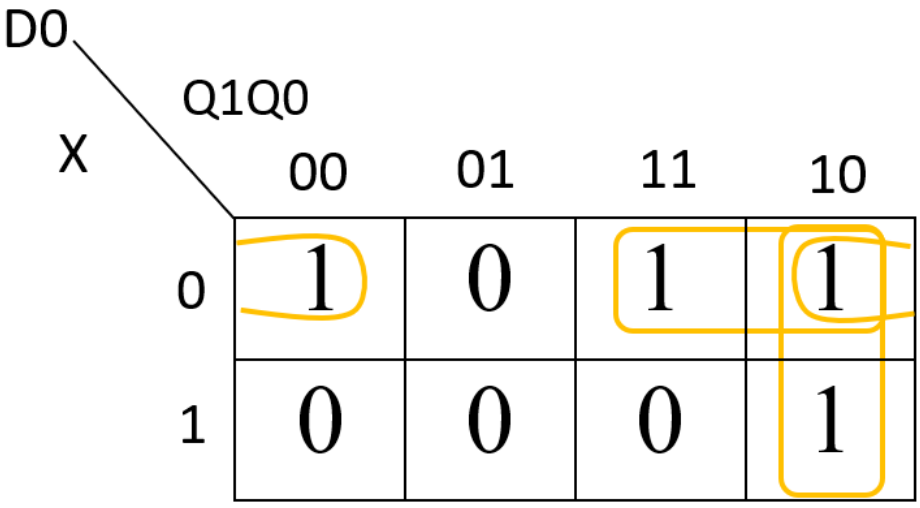
Table 3

Input X	Present State		Next State		D FF Transition	
	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

b) Get the optimized Boolean expression.

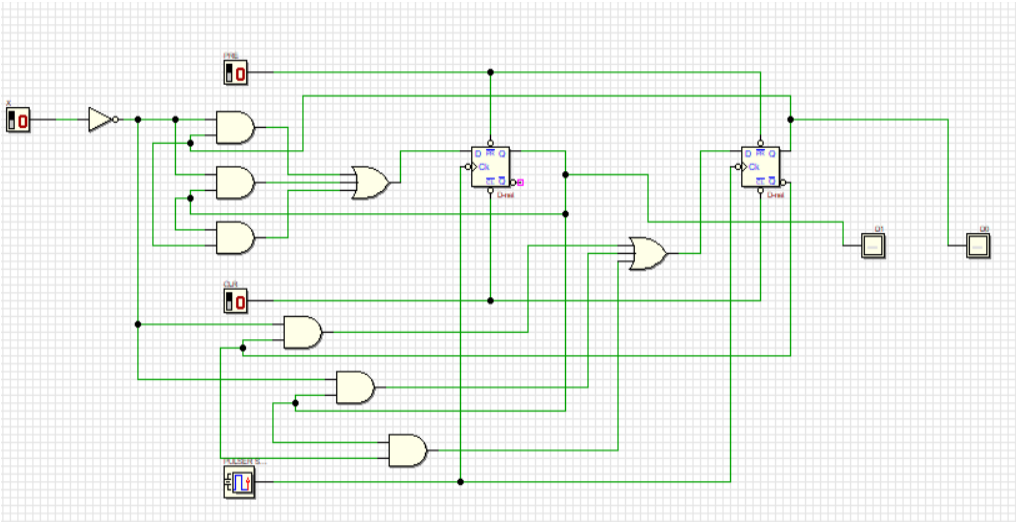


$$D1 = X'Q0 + X'Q1 + Q1Q0$$

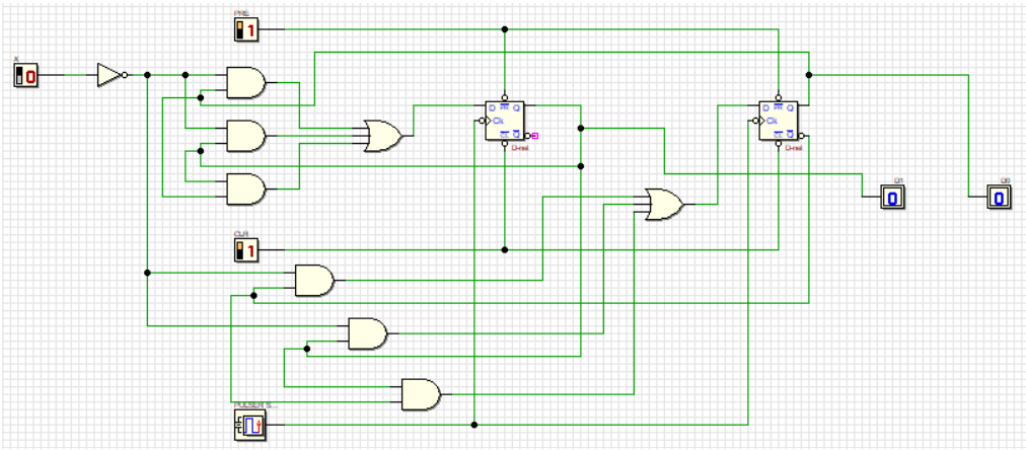


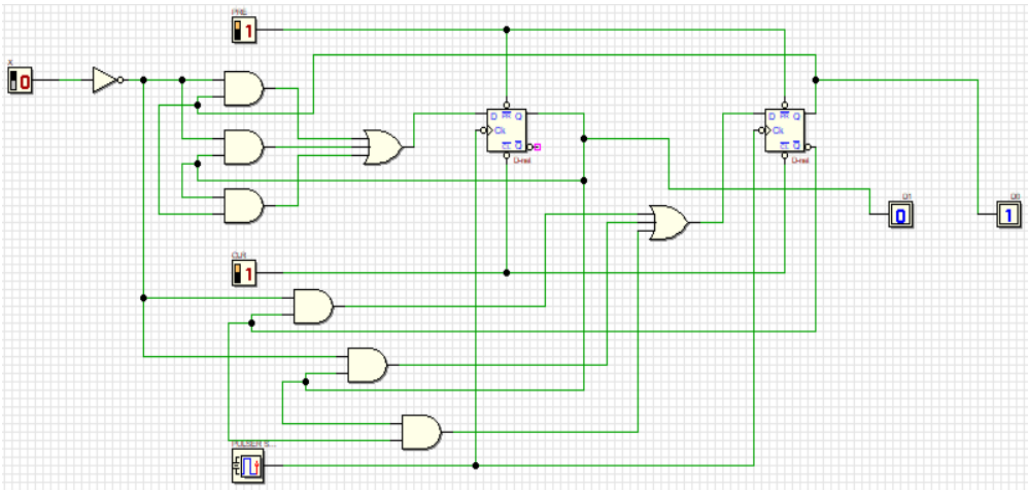
$$D0 = X'Q0' + X'Q1 + Q1Q0'$$

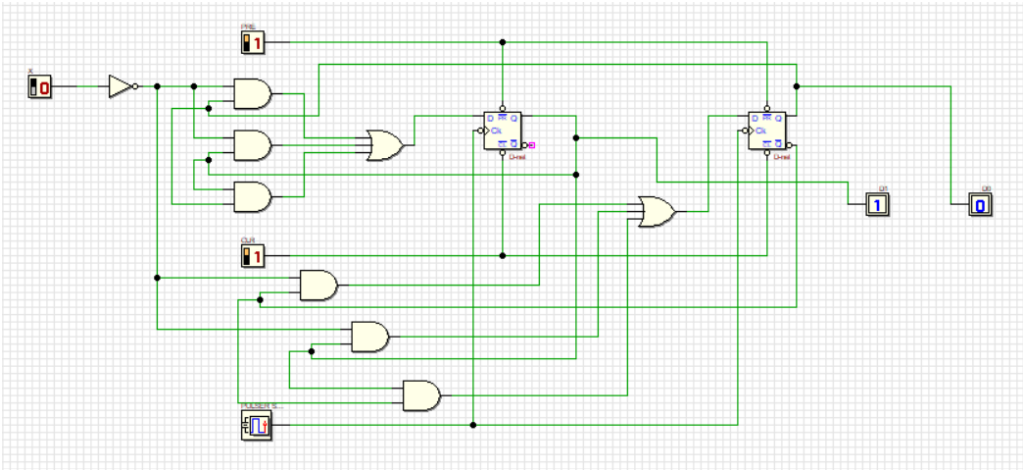
c) Draw the complete final circuit design in Deeds.

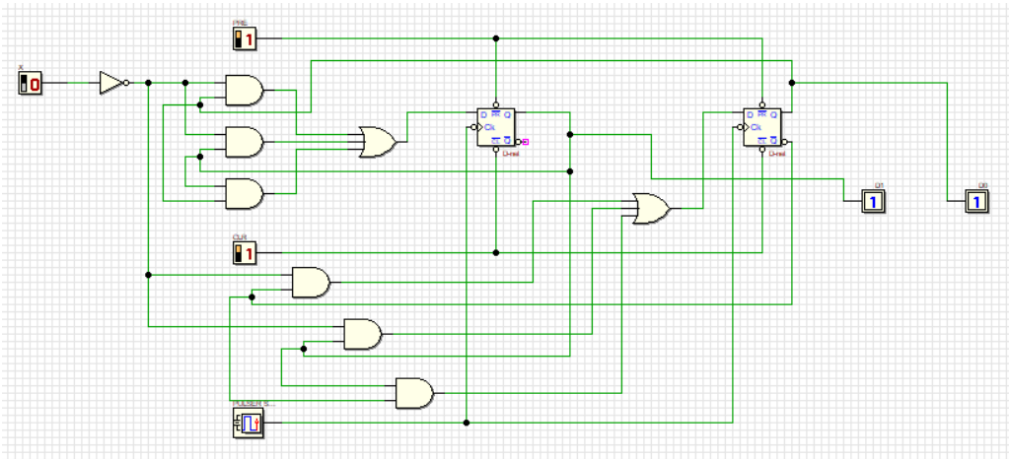


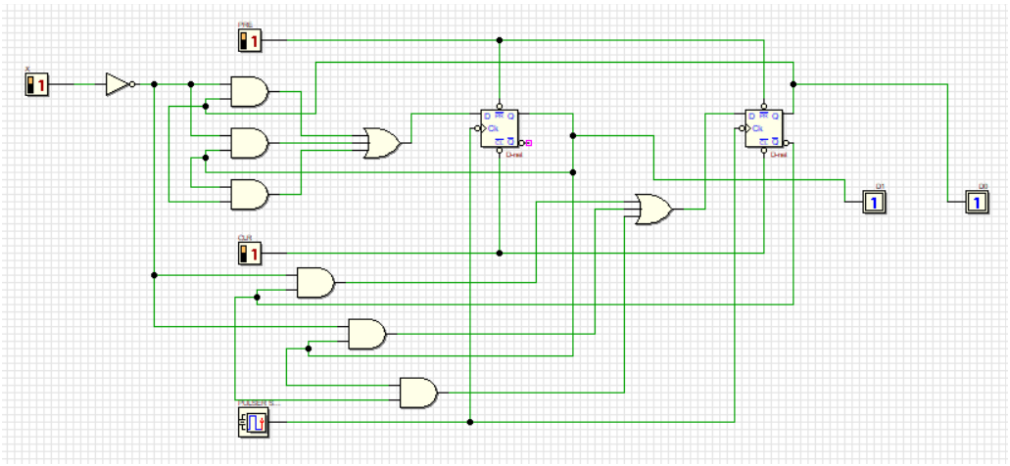
d) Simulate the circuit to prove your Table 3 is correct.

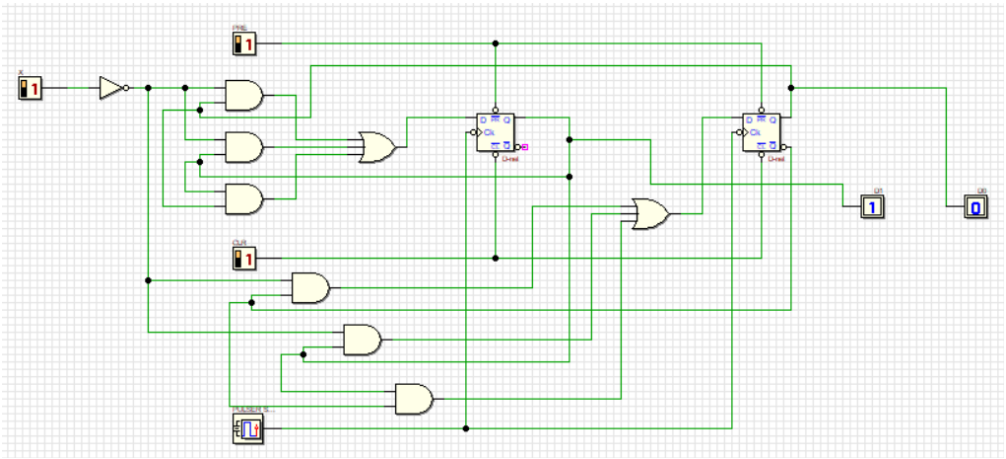


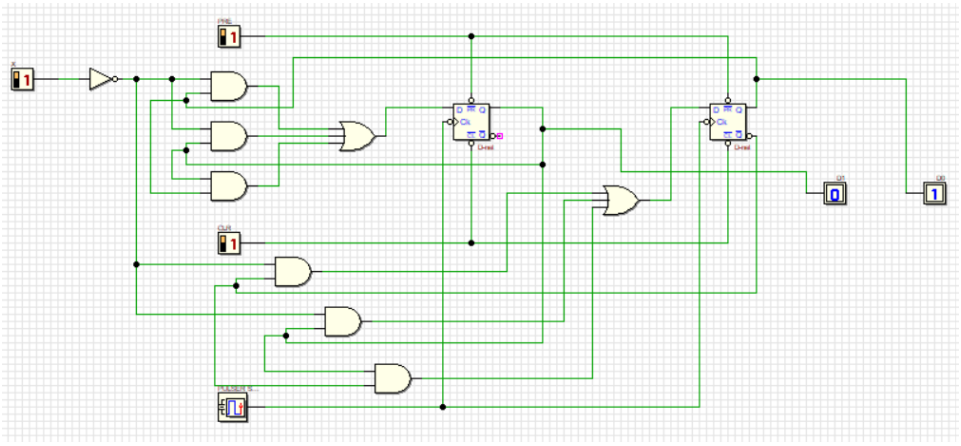

PRE
1
X
0
CLR
1
Q0
0
Q1
1

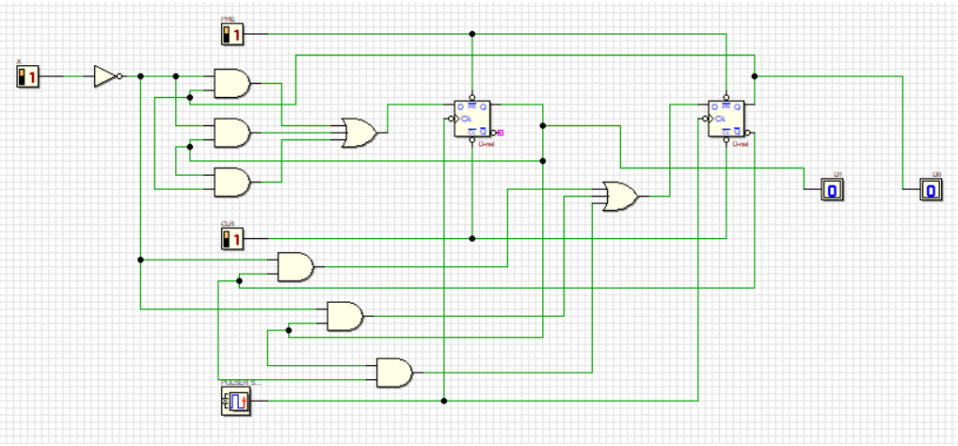

PRE
1
X
0
CLR
1
Q0
1
Q1
0


PRE
1
X
0
CLR
1
Q0
1
Q1
1









7) Repeat steps in Q(6) using T flip-flop.

a) Built the next state and transition table using the header in Table 3.

Table 4

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

b) Get the optimized Boolean expression.

T1

X \ Q1Q0	00	01	11	10
0	0	1	0	0
1	0	0	0	1

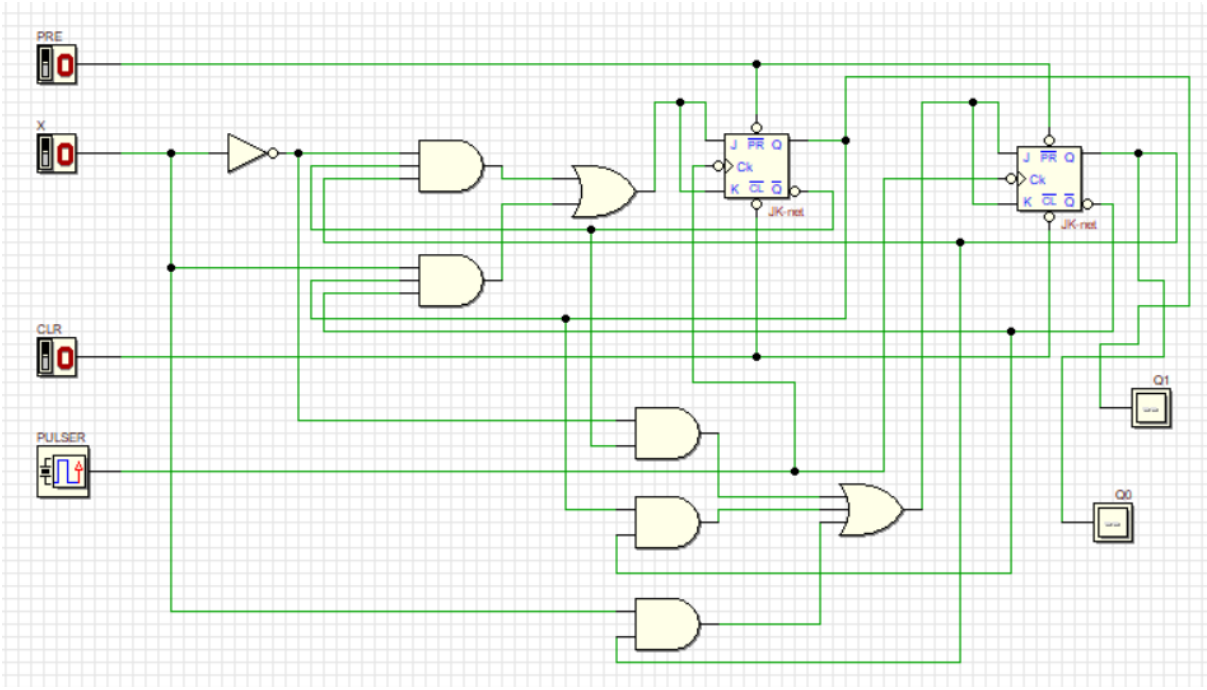
$$T1 = \overline{XQ1}Q0 + XQ1\overline{Q0}$$

T0

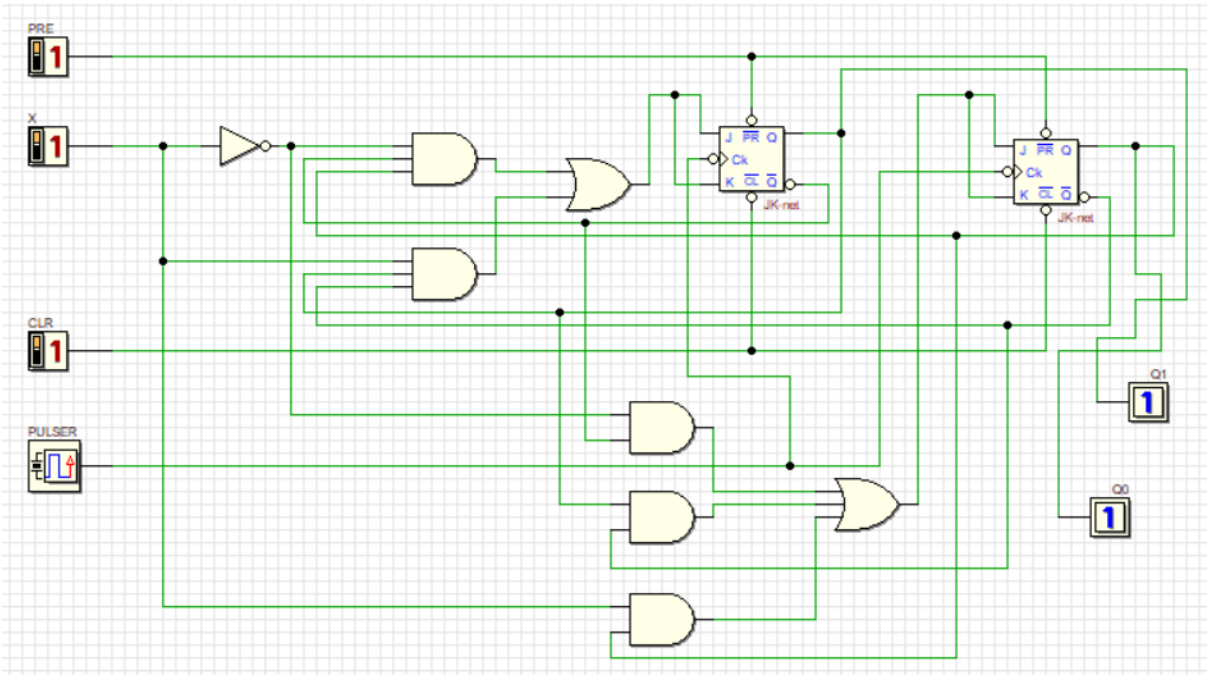
X \ Q1Q0	00	01	11	10
0	1	1	0	1
1	0	1	1	1

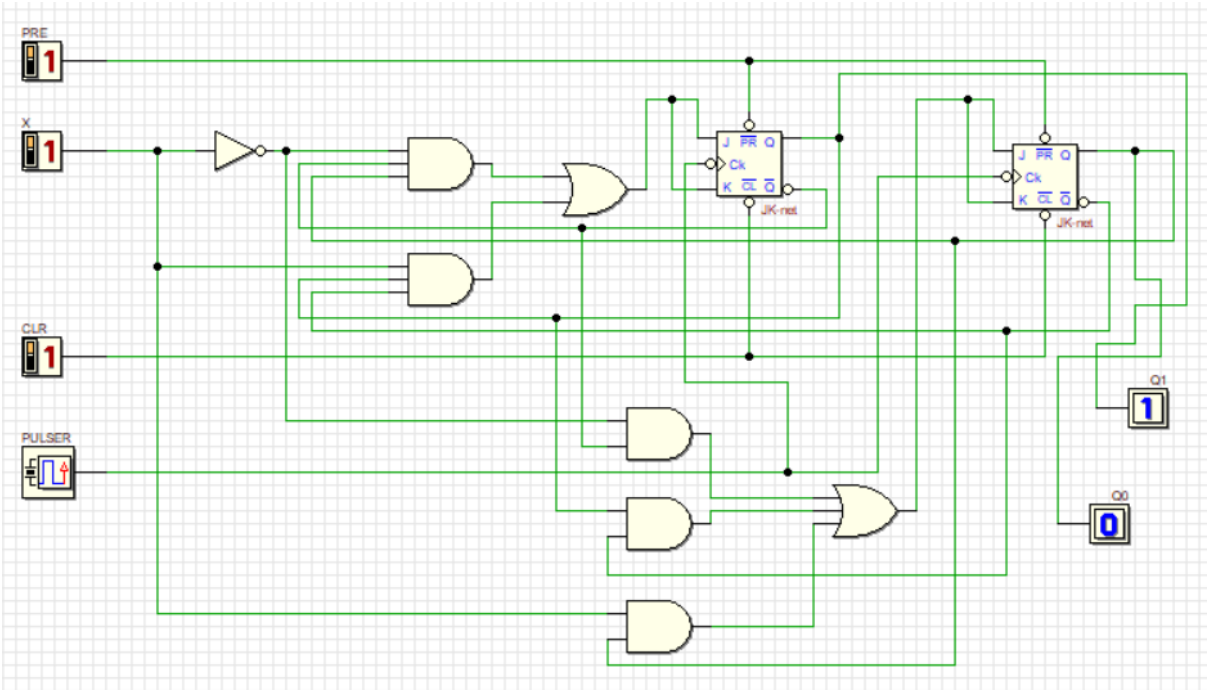
$$T0 = \overline{XQ1} + XQ0 + Q1\overline{Q0}$$

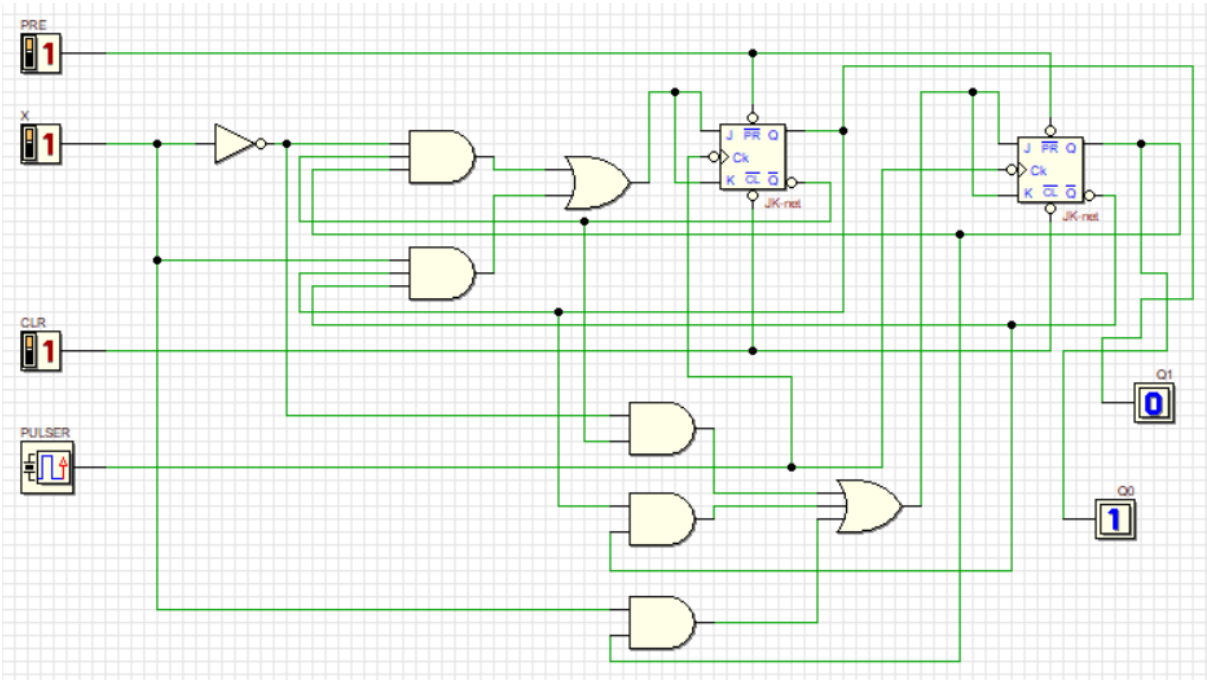
c) Draw the complete final circuit design in Deeds.

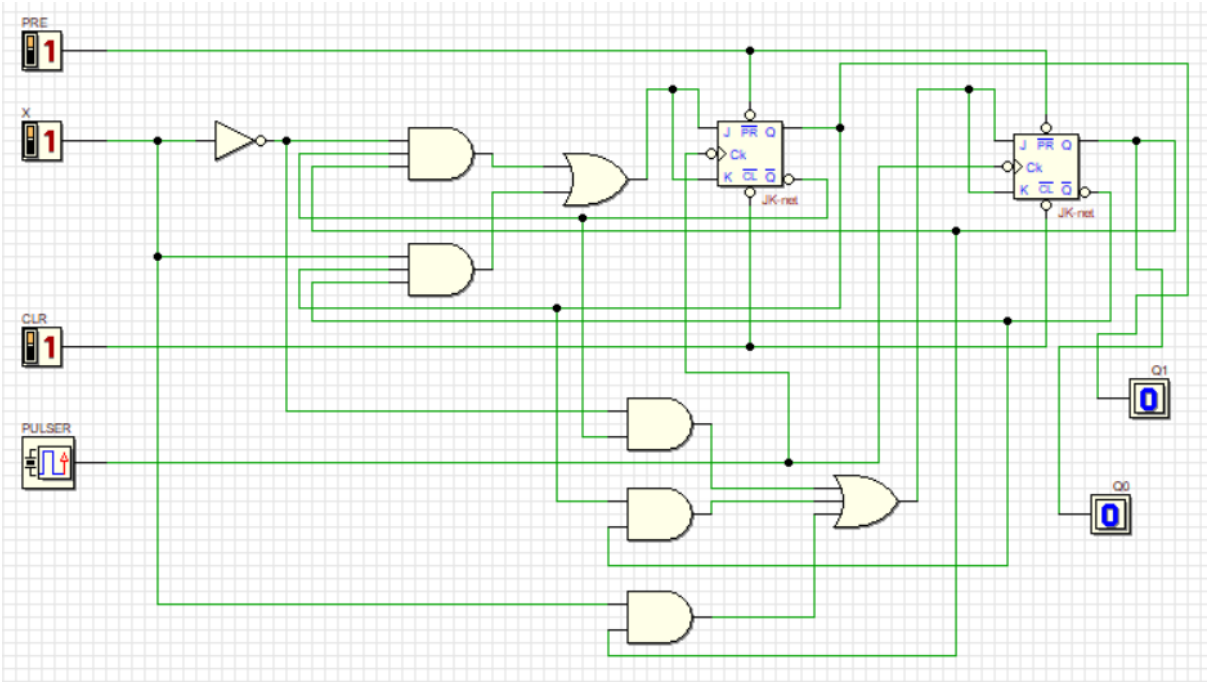


d) Simulate the circuit to prove your Table 3 is correct.




PRE
1
X
1
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-net
J PR Q
Ck
K CL Q
JK-net
Q1
1
Q0
0


PRE
1
X
1
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-net
J PR Q
Ck
K CL Q
JK-net
Q1
0
Q0
1


PRE
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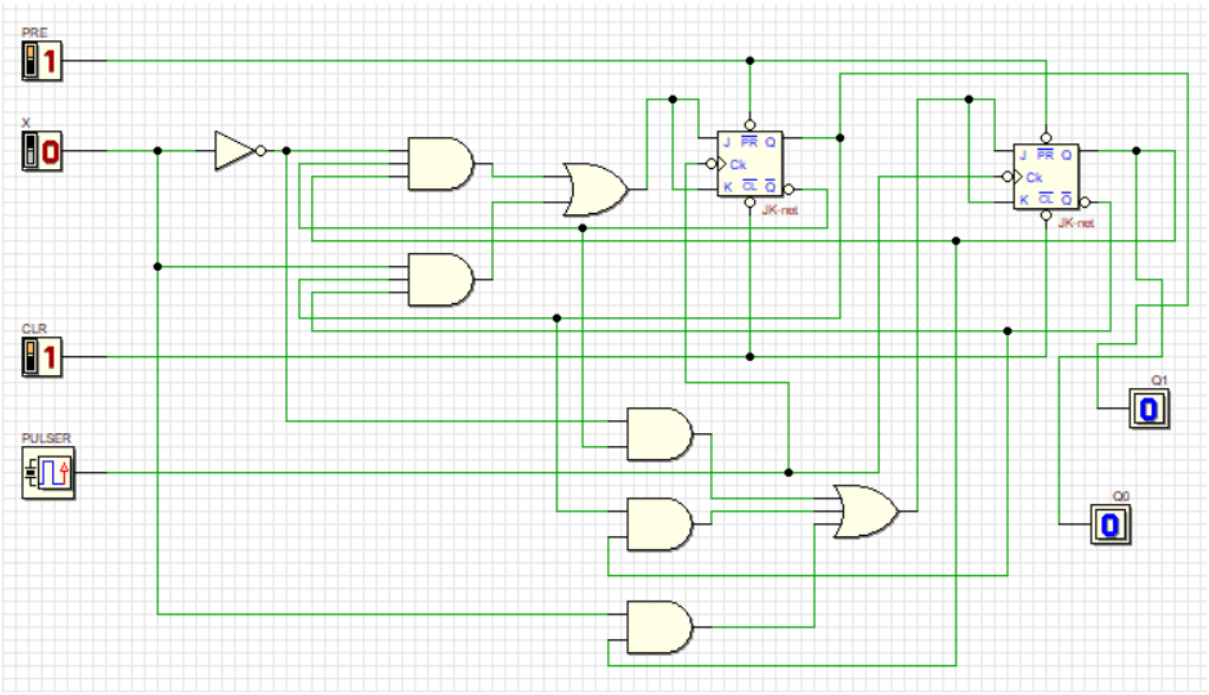
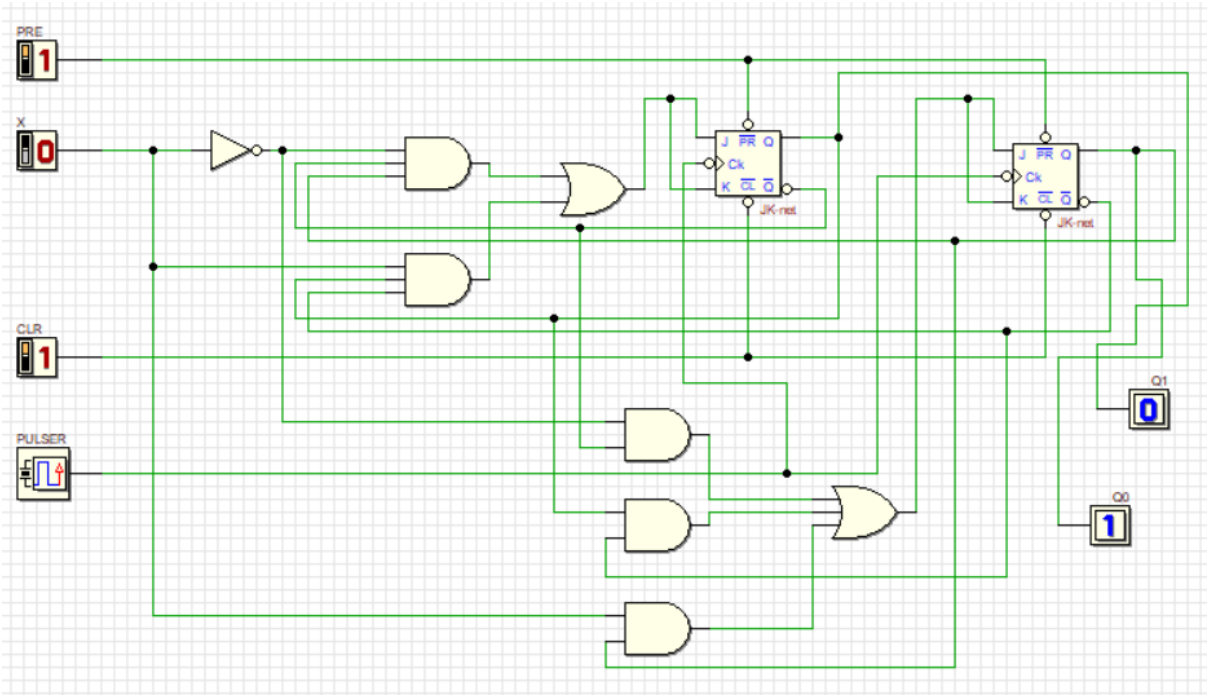
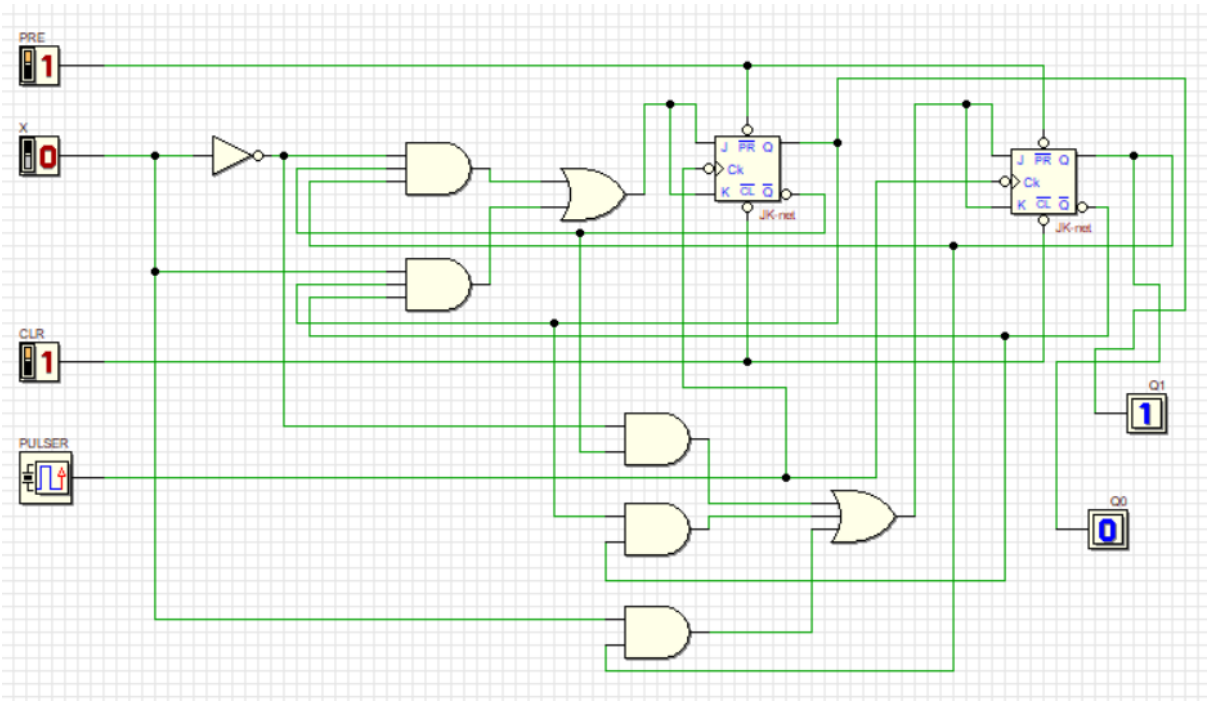
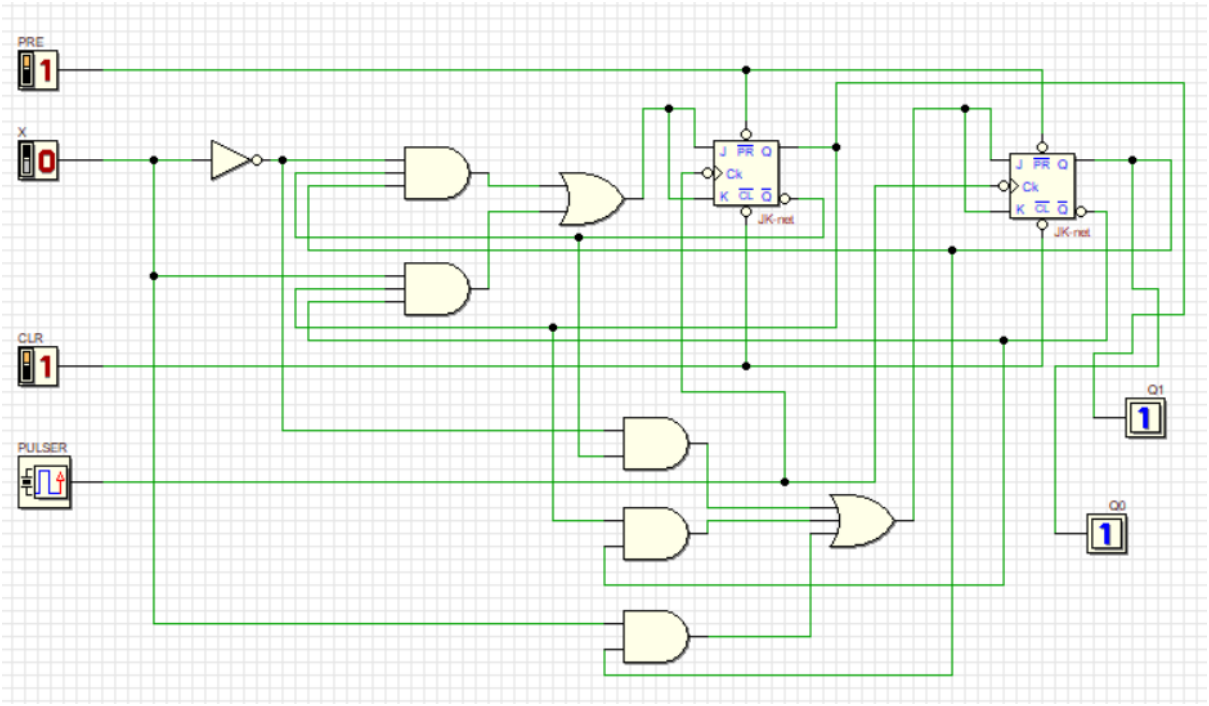
X
1
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-net
J PR Q
Ck
K CL Q
JK-net
Q1
0
Q0
0


PRE
1
X
0
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-net
J PR Q
Ck
K CL Q
JK-net
Q1
0
Q0
0


PRE
1
X
0
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-nst
J PR Q
Ck
K CL Q
JK-nst
Q1
0
Q0
1


PRE
1
X
0
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-nst
J PR Q
Ck
K CL Q
JK-nst
Q1
1
Q0
0


PRE
1
X
0
CLR
1
PULSER
J PR Q
Ck
K CL Q
JK-nst
J PR Q
Ck
K CL Q
JK-nst
Q1
1
Q0
1