UTM
UNIVERSITI TEKNOLOGI MALAYSIA

SEM 1 2020/2021: SECTION 01

Digital Logic

LAB 2

Students Information

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D. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

$Y = AB + BC + BC$

$Y = AB\,(C+C') + BC\,(A+A') + AC\,(B+B')$

$Y = (ABC + ABC') + (ABC + A'BC) + (ABC + AB'C)$

$Y = [ABC + (ABC + ABC)] + ABC' + A'BC + AB'C$

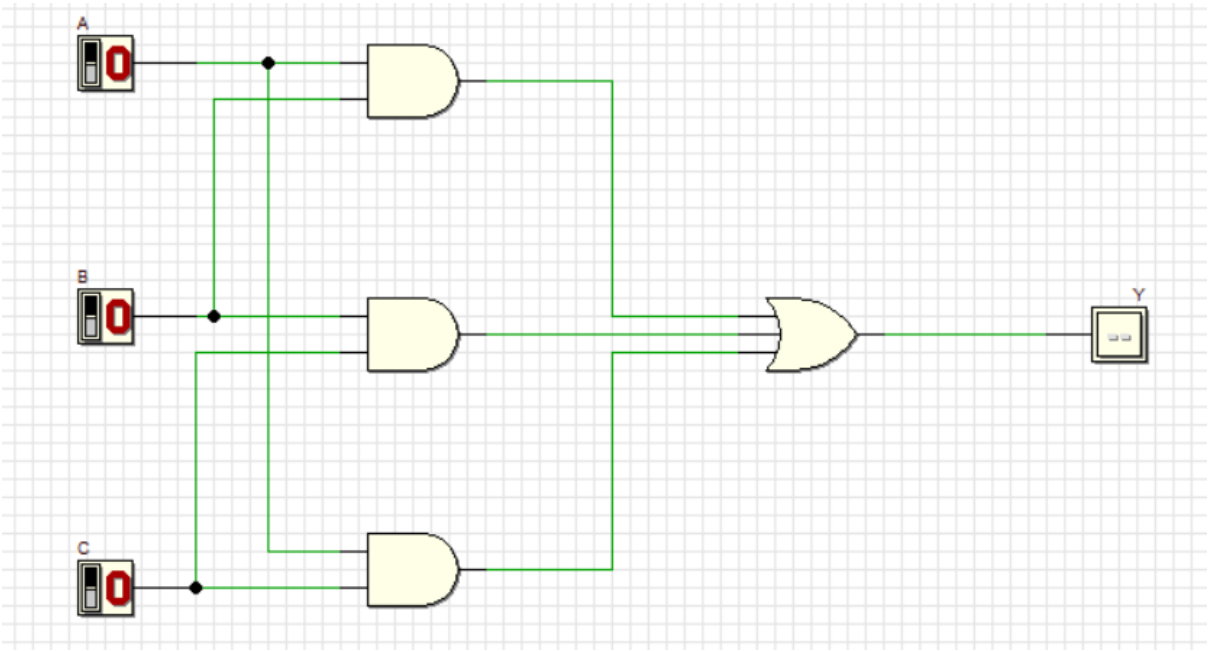
$Y = ABC + A'BC + AB'C + ABC'$

2. Based on standard form expression, complete the following truth table.

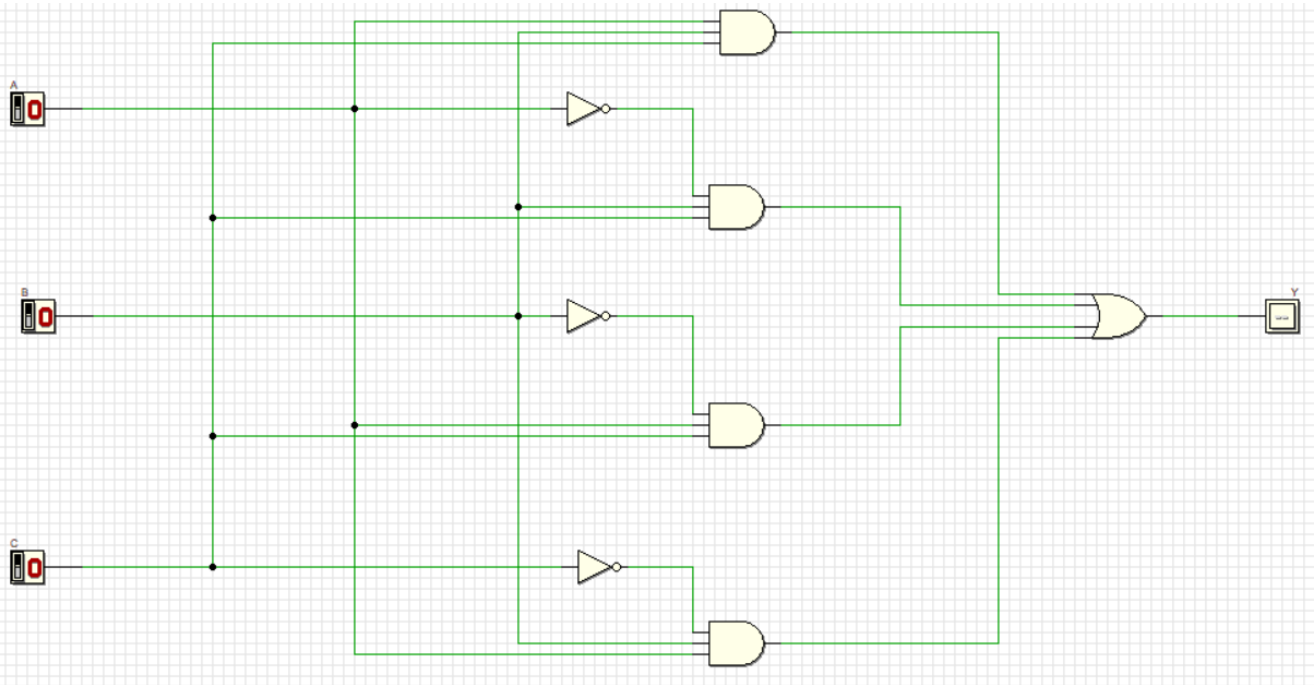
INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



b) Circuit (ii) for standard form (from your answer in question (1)).



4. Simulate these two circuits in step (3) and complete the truth table.
   Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Circuit (ii)

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

From the truth table above, it shows that both circuit (i) and circuit (ii) produce the same output. This is because the minimization Boolean expression is only to simplify the Boolean expression thus reduce the circuitry as it uses less number of gates to produce same output.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and outputs.