UTM

UNIVERSITI TEKNOLOGI MALAYSIA

Semester 2020/2021

Subject : Digital logic

Section : 06

Task : Lab 3

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D. Preliminary Works

1.

Table 1

Desired result	PRE'	CLR'	J	K	CLK	Q
Set initial value Q = 1	**0**	**1**	**X**	**X**	--	**1**
Output Q stays the same	**1**	**1**	**0**	**0**	⇓	**1**
Output Q become 0, no change in asynchronous input	**1**	**1**	**1**	**1**	⇓	**0**
Output Q is not the previous Q	**1**	**1**	**1**	**1**	⇓	**1**
RESET Q	**1**	**1**	**0**	**1**	⇓	**0**
SET Q	**1**	**1**	**1**	**0**	⇓	**1**

2. **a)** JK toggles when J is active (HIGH) and K is also active (HIGH)
b) Negative edge triggered

E. Lab Activities

1.

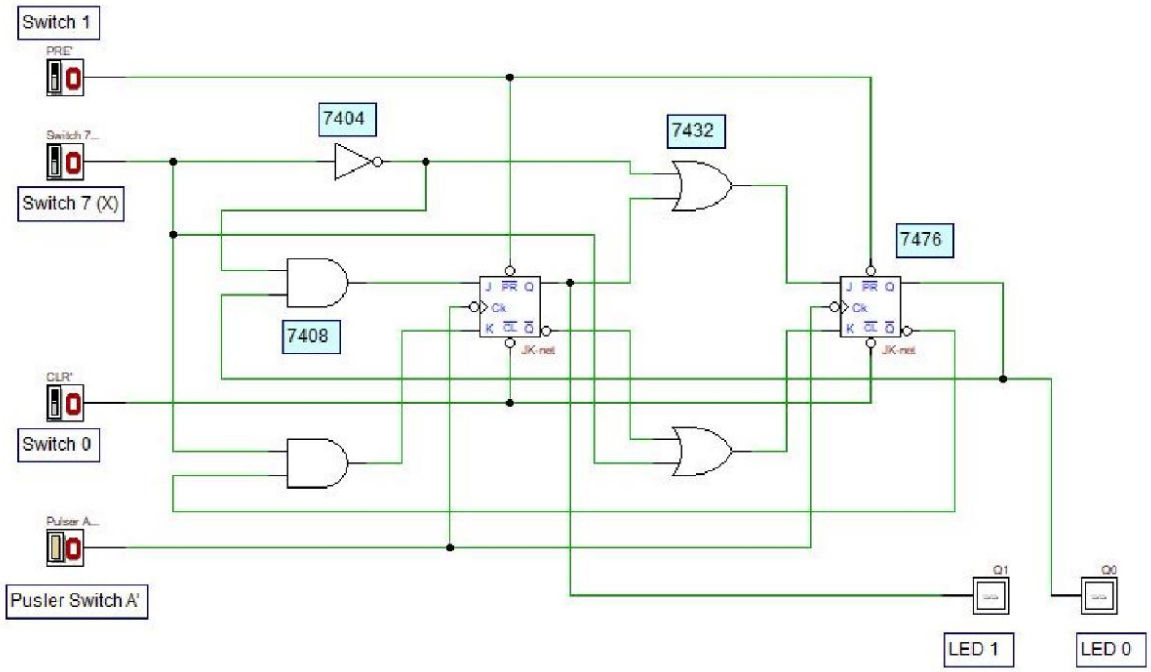


Figure 4: A Synchronous Counter Circuit

2.

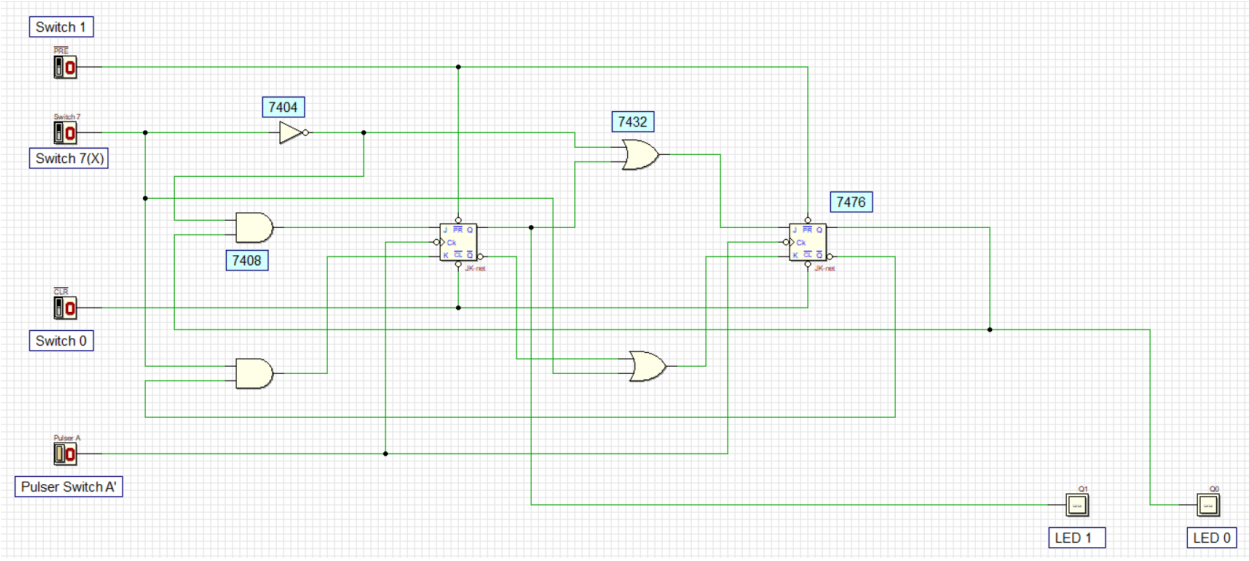


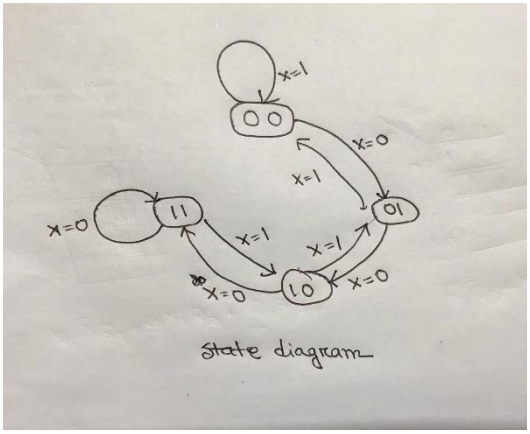
Figure 5: A Synchronous Counter Circuit

3.

Table 2

Switch 7	Present State		Next State	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4. **State diagram**



5. **a)** Both flip-flop are triggered with same clock simultaneously
b) There are 4 states: 00,01,10,11
c) Switch 7 is count direction, it will determine if counter will go up or down. X=1(count down) and X=0 (count up)

d) There are asynchronous inputs, if both set to 1, JK can work synchronously. Switch 1 is active (HIGH), it presets output to 1 and when switch 0 is active, it clears the output to 0

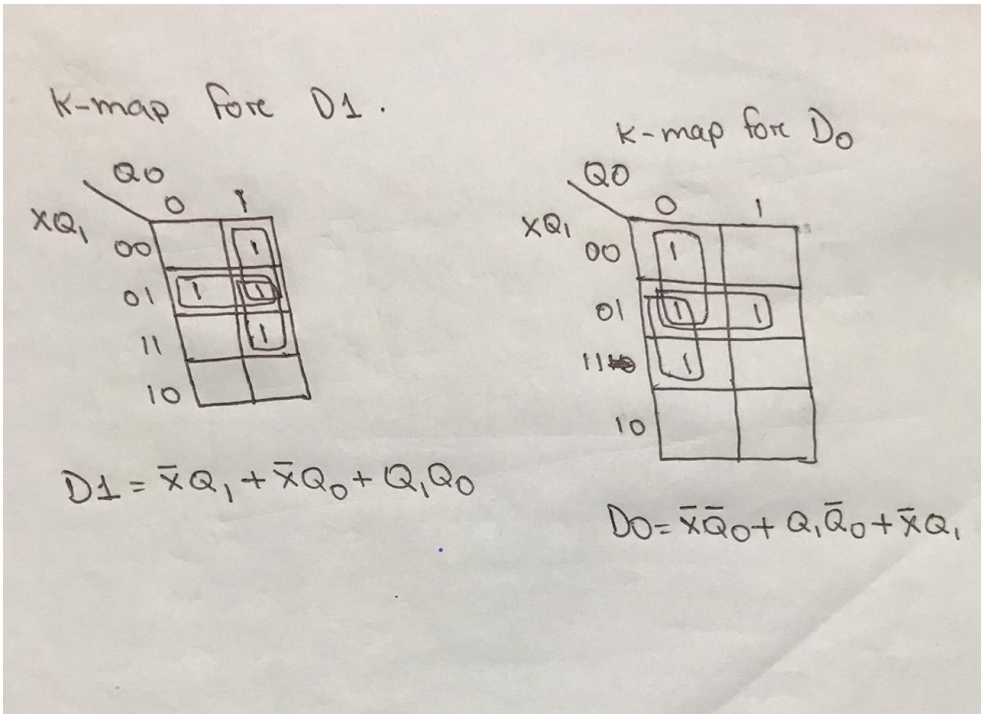
e) Yes, it is saturated counter.

6. **a)**

Table 3

Switch 7	Present State		Next State		D FF Transition	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

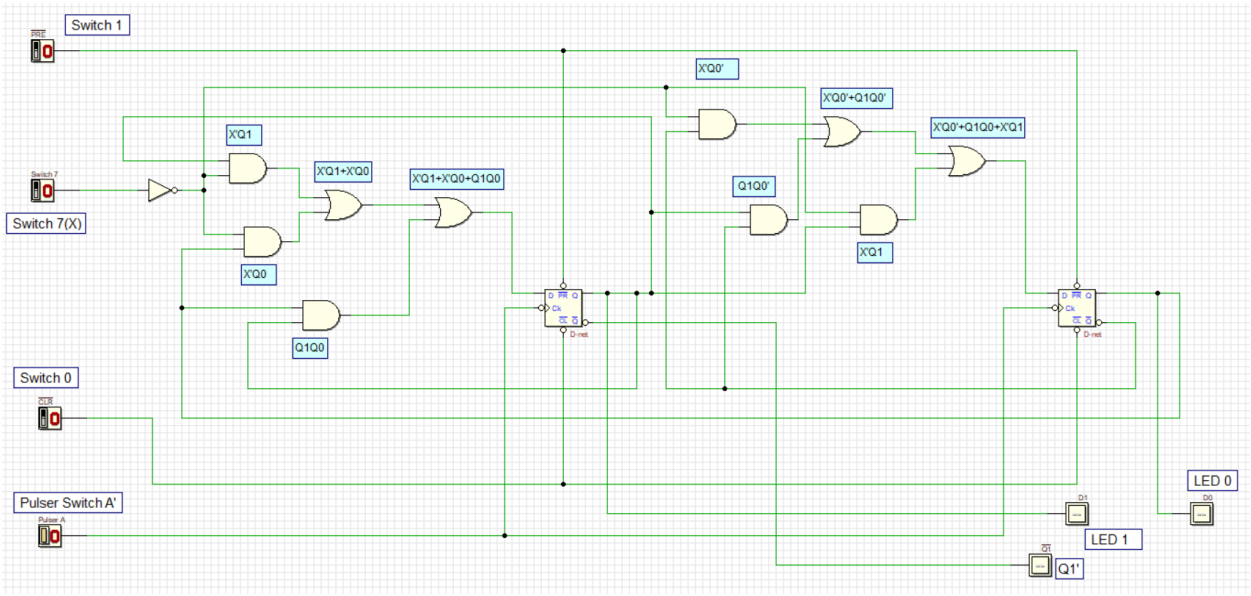
b)



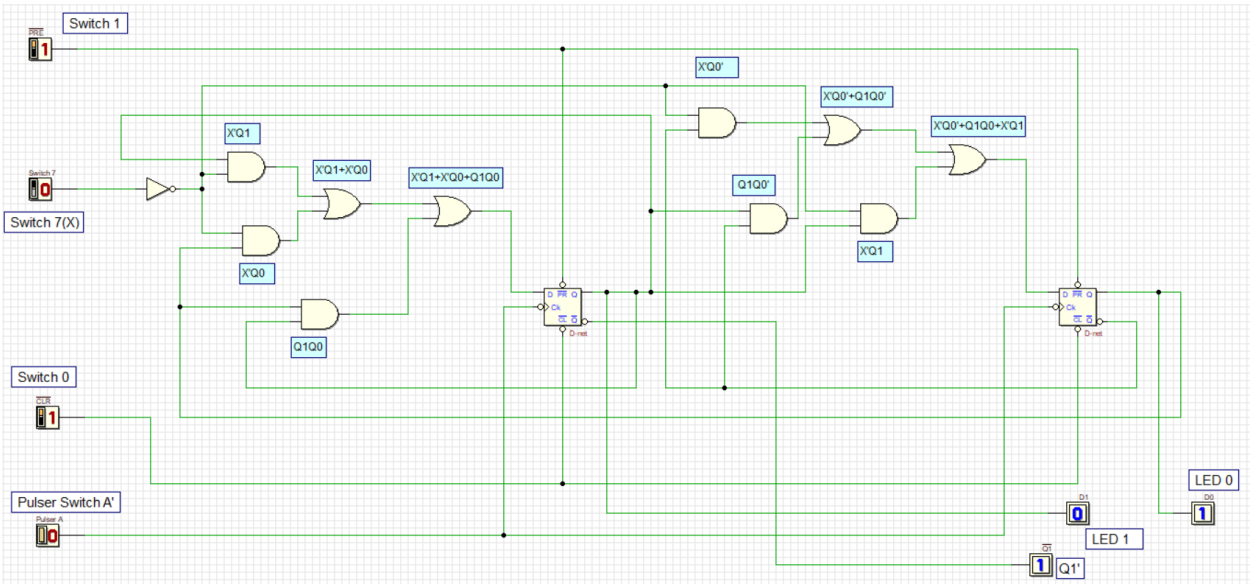
Boolean expression:

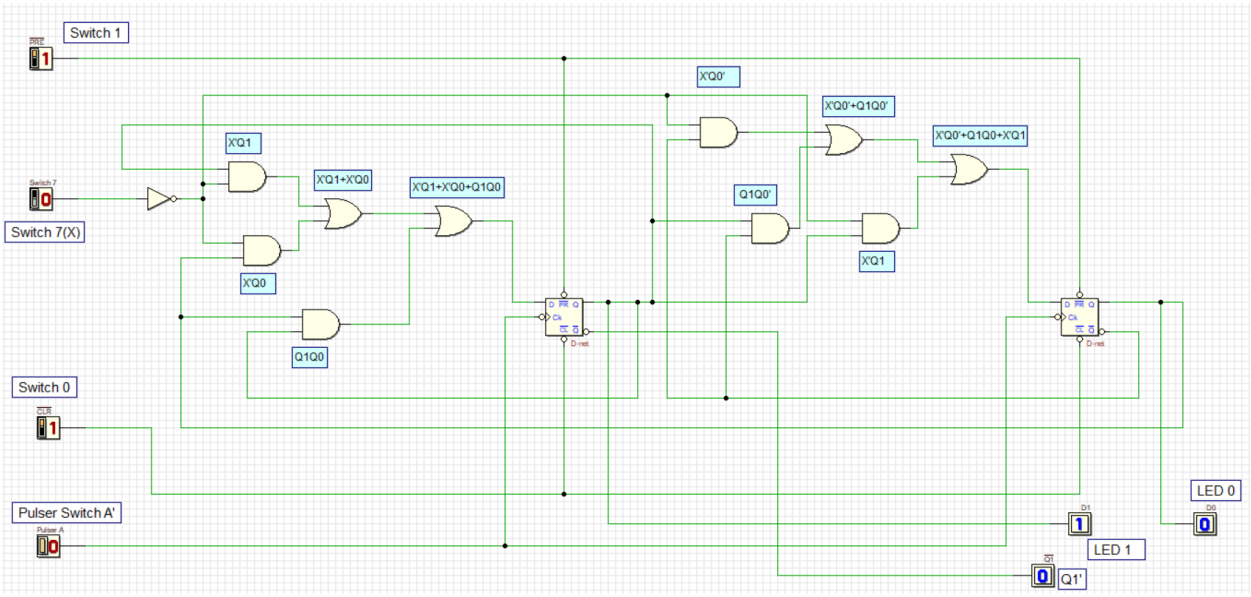
D1 = X'Q1+ X'Q0+ Q1Q0 D0 = X'Q0' + Q1Q0' + X'Q1

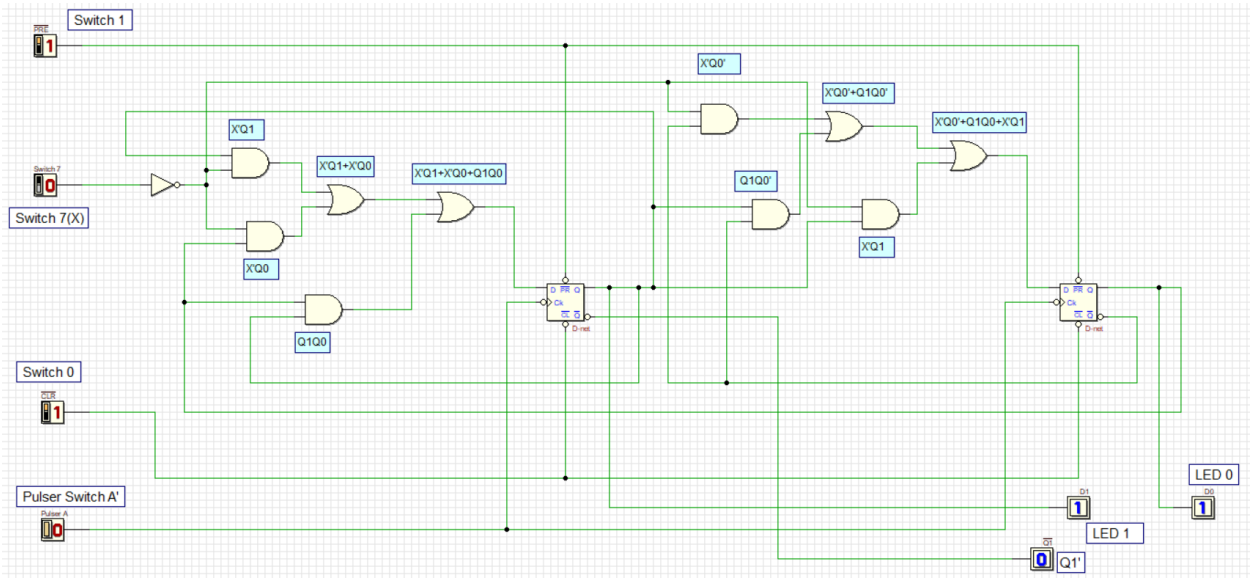
Circuit design for D FF

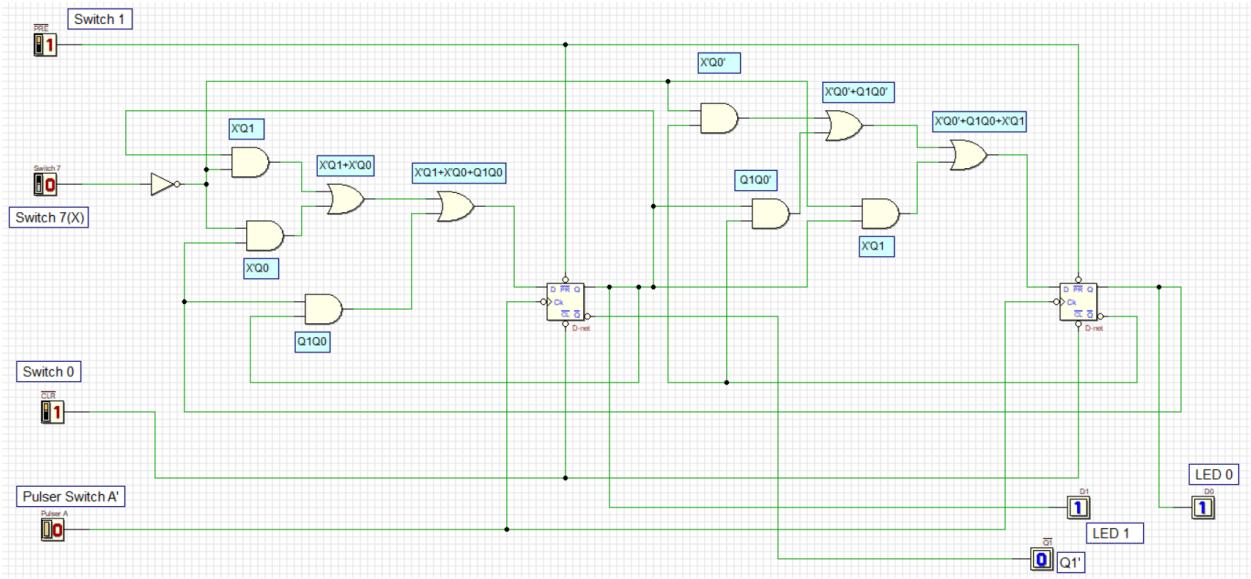


c) Count up

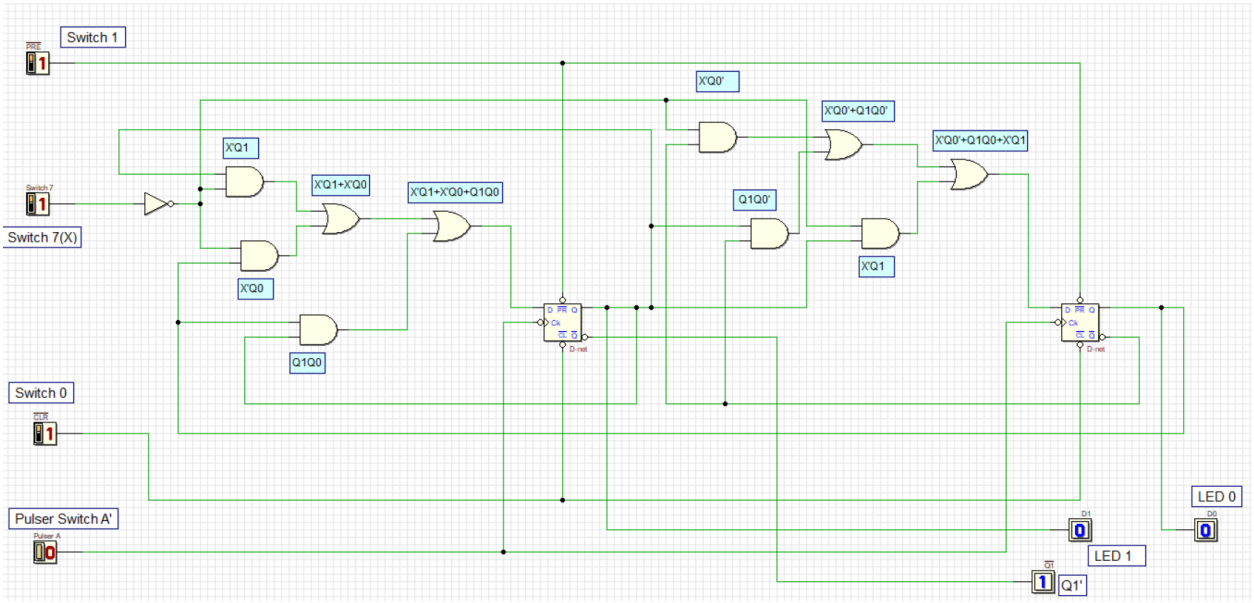


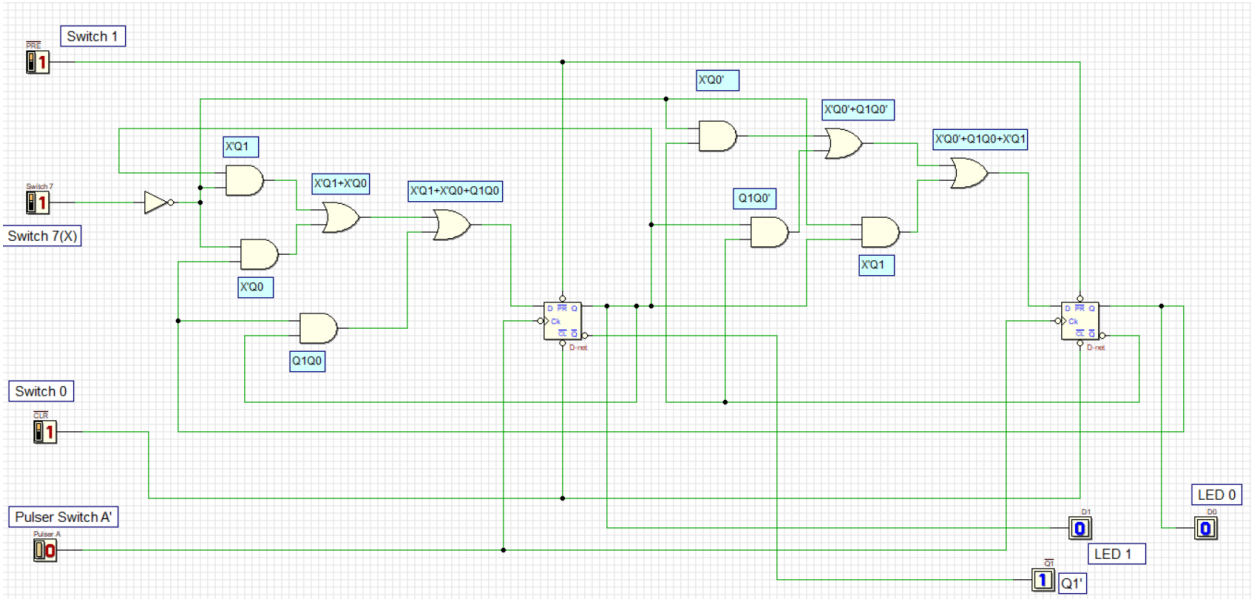

Switch 1
X'Q0'
X'Q0'+Q1Q0'
X'Q0'+Q1Q0+X'Q1
X'Q1
X'Q1+X'Q0
X'Q1+X'Q0+Q1Q0
Switch 7
Switch 7(X)
Q1Q0'
X'Q1
X'Q0
Q1Q0
Switch 0
Pulser Switch A'
LED 0
LED 1
Q1'

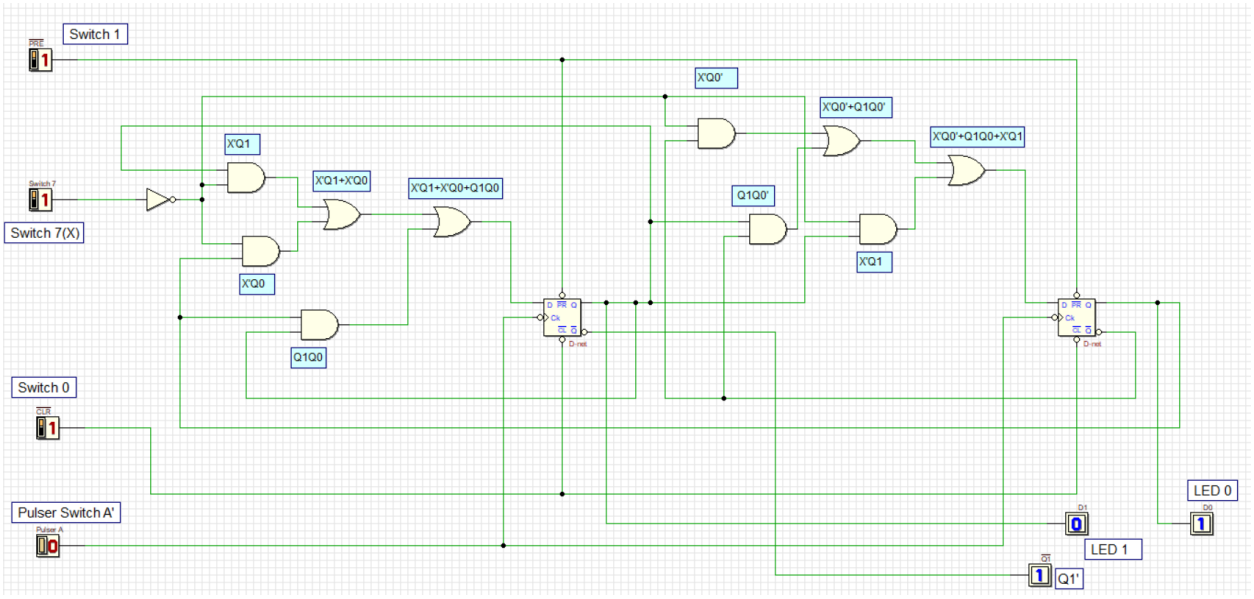

Switch 1
X'Q0'
X'Q0'+Q1Q0'
X'Q0'+Q1Q0+X'Q1
X'Q1
X'Q1+X'Q0
X'Q1+X'Q0+Q1Q0
Switch 7
Switch 7(X)
Q1Q0'
X'Q1
X'Q0
Q1Q0
Switch 0
Pulser Switch A'
LED 0
LED 1
Q1'

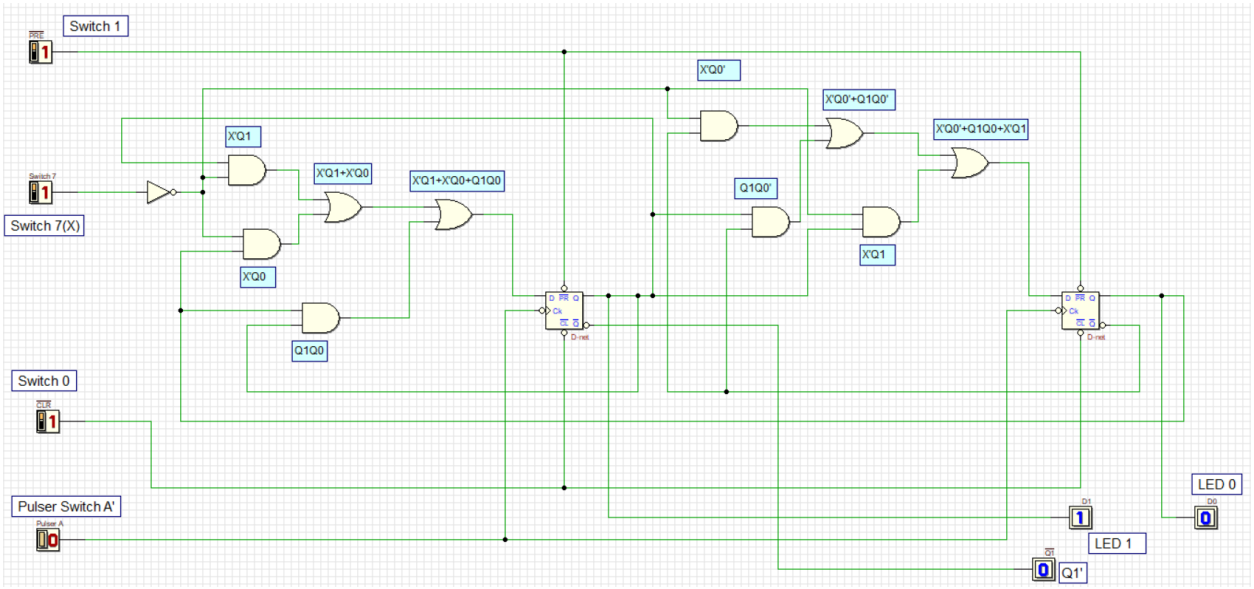

Switch 1
X'Q0'
X'Q0'+Q1Q0'
X'Q0'+Q1Q0+X'Q1
X'Q1
X'Q1+X'Q0
X'Q1+X'Q0+Q1Q0
Switch 7
Switch 7(X)
Q1Q0'
X'Q1
X'Q0
Q1Q0
Switch 0
Pulser Switch A'
LED 0
LED 1
Q1'

Count down


Switch 1
X'Q1
X'Q1+X'Q0
X'Q1+X'Q0+Q1Q0
X'Q0'
X'Q0'+Q1Q0'
X'Q0'+Q1Q0+X'Q1
Q1Q0'
X'Q1
Switch 7
Switch 7(X)
X'Q0
Q1Q0
Switch 0
Pulser Switch A'
LED 0
LED 1
Q1'


Switch 1
X'Q1
X'Q1+X'Q0
X'Q1+X'Q0+Q1Q0
X'Q0'
X'Q0'+Q1Q0'
X'Q0'+Q1Q0+X'Q1
Q1Q0'
X'Q1
Switch 7
Switch 7(X)
X'Q0
Q1Q0
Switch 0
Pulser Switch A'
LED 0
LED 1
Q1'



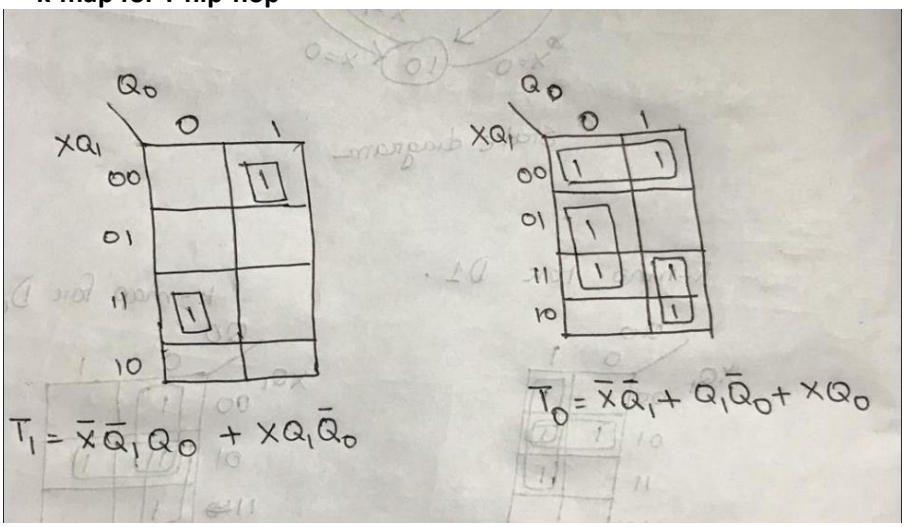


7. a)

Table 4

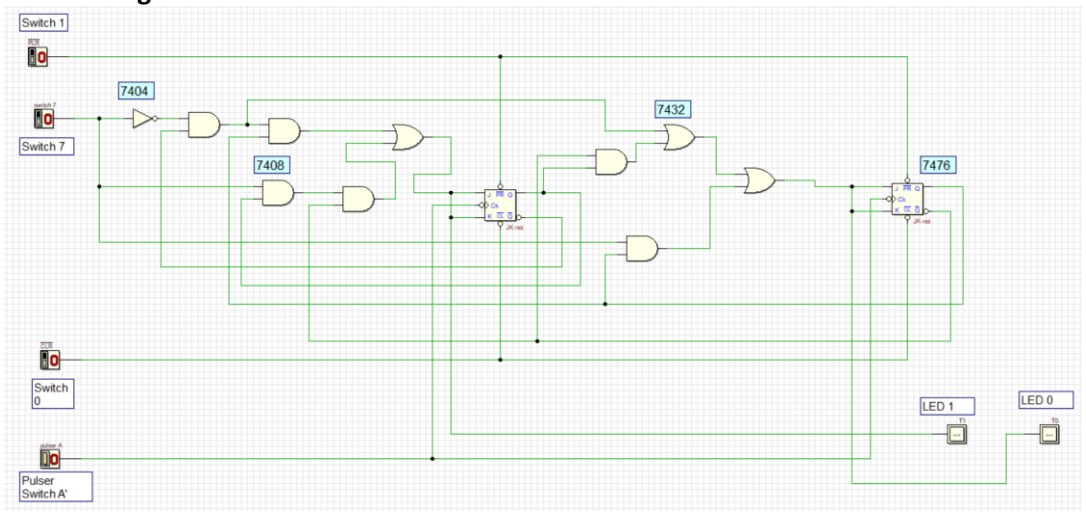
Switch 7	Present State		Next State		D FF Transition	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

k-map for T flip-flop



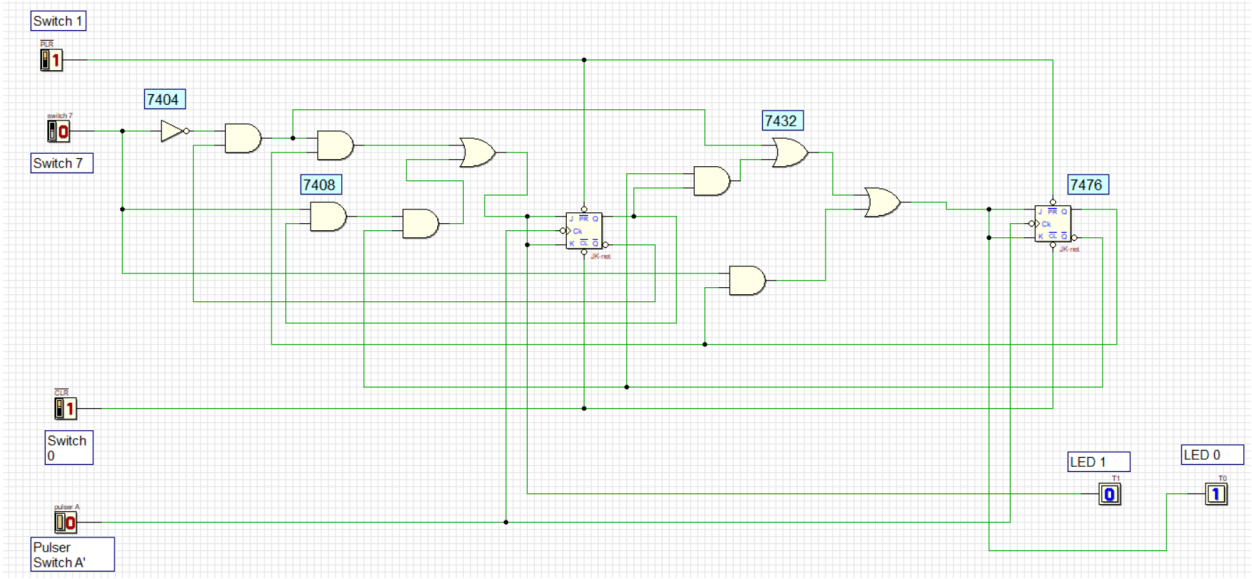
Boolean expression: T1=X'Q1'Q0 + XQ1Q0' T0=X'Q1' + Q1Q0' + XQ0

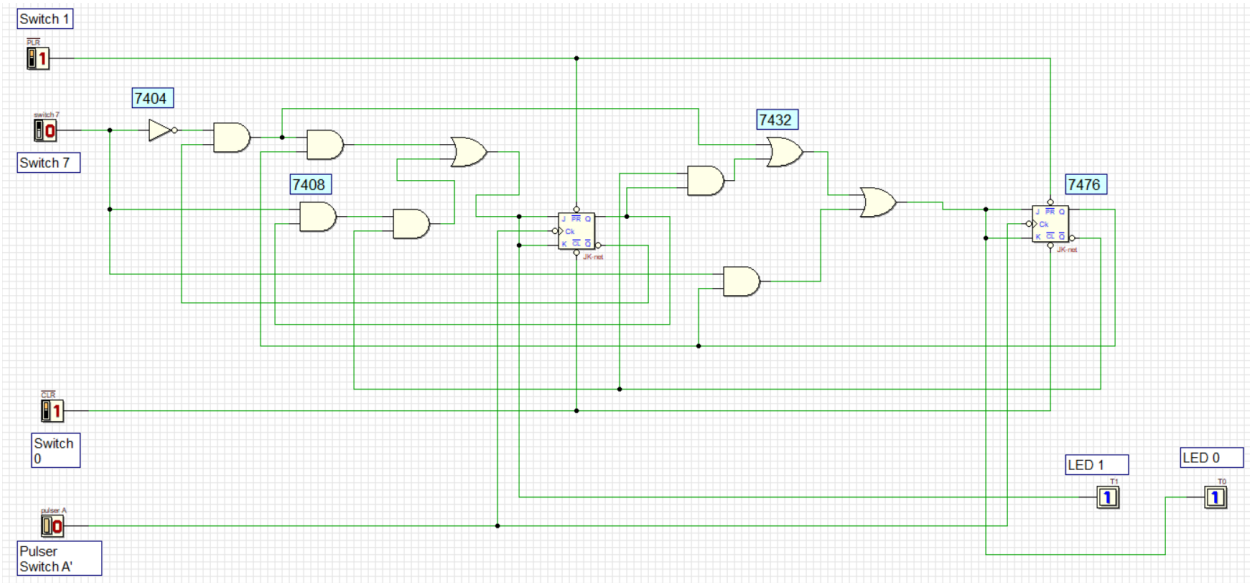
Circuit design for T FF

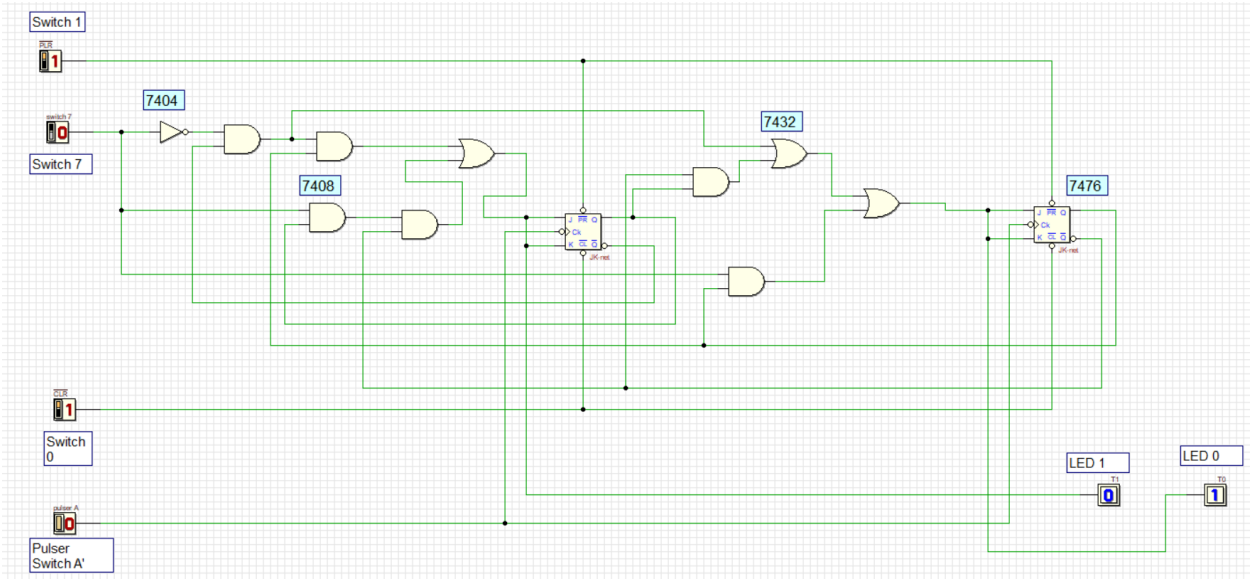


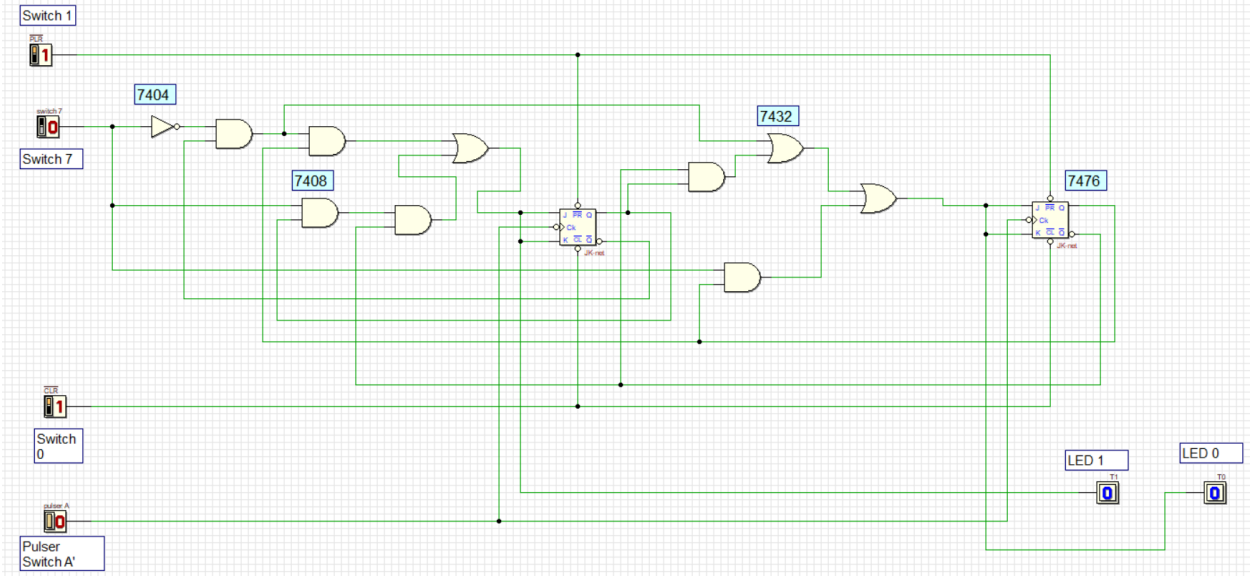
Simulation

Count up

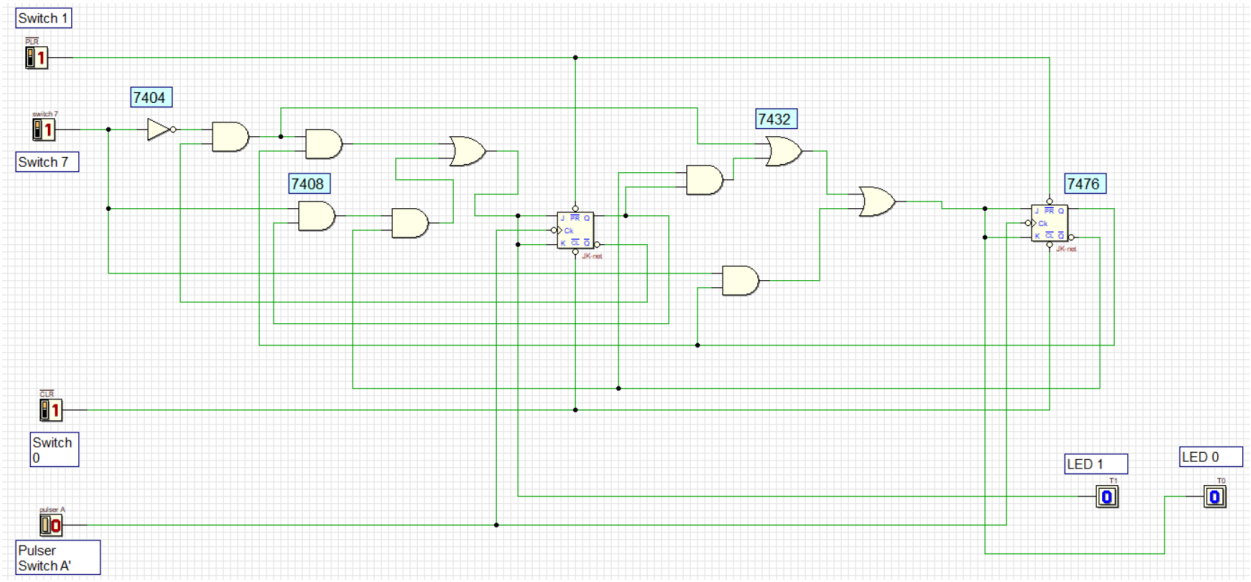


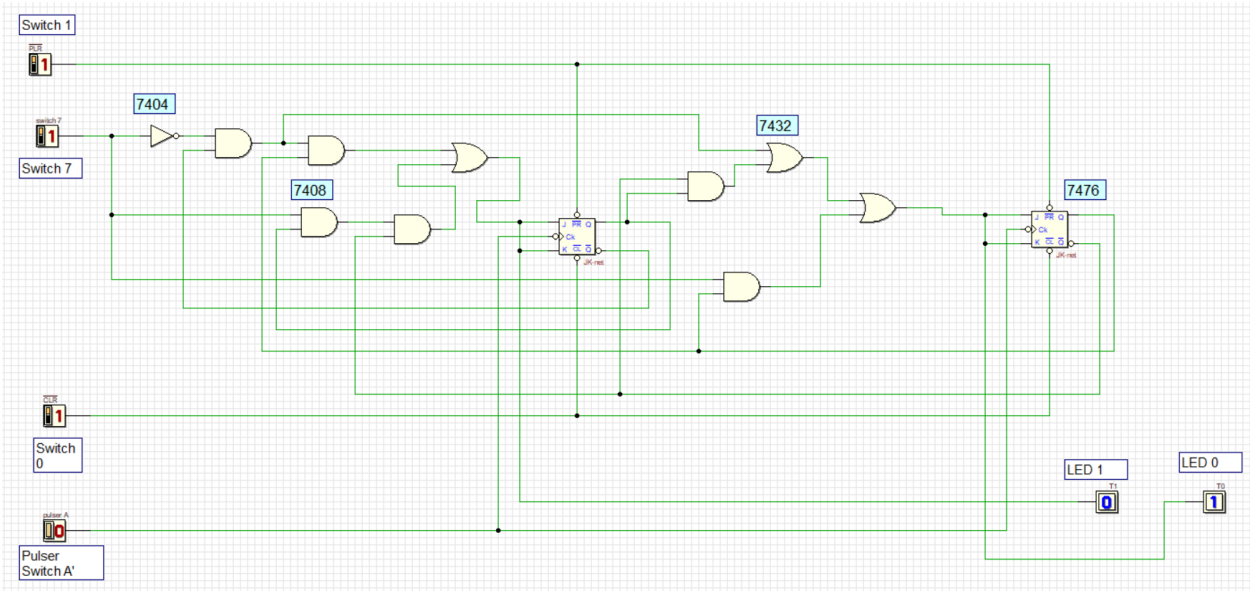

Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
Pulser
Switch A'
LED 1
LED 0

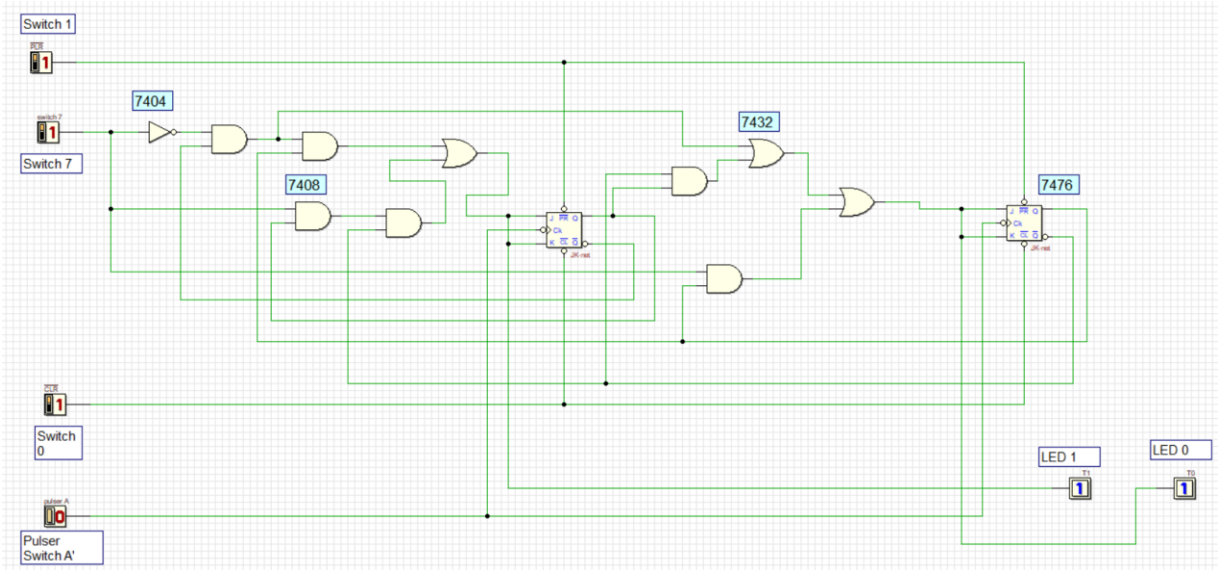

Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
Pulser
Switch A'
LED 1
LED 0

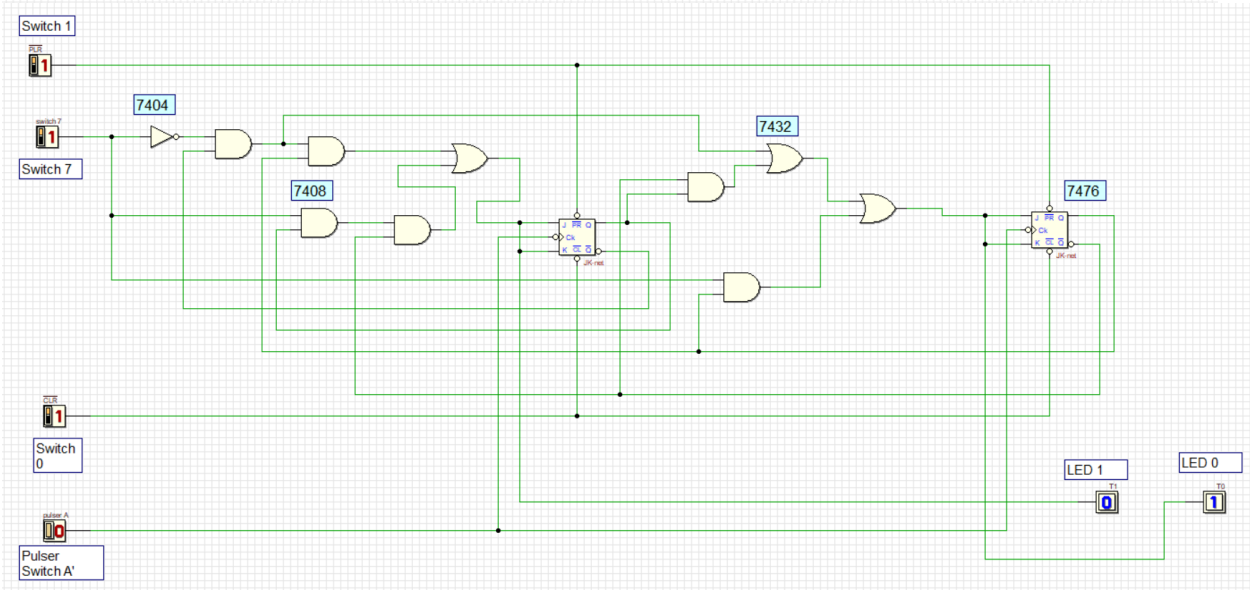

Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
Pulser
Switch A'
LED 1
LED 0

Count down


Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
LED 1
LED 0
Pulser
Switch A'


Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
LED 1
LED 0
Pulser
Switch A'


Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
Pulser
Switch A'
LED 1
LED 0


Switch 1
7404
Switch 7
7408
7432
7476
Switch
0
Pulser
Switch A'
LED 1
LED 0