

**SCHOOL OF COMPUTING**

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**GROUP: 09**

**Submission Date: 29/01/2021**

**D. Preliminary Works**

**1.**

**Table 1**

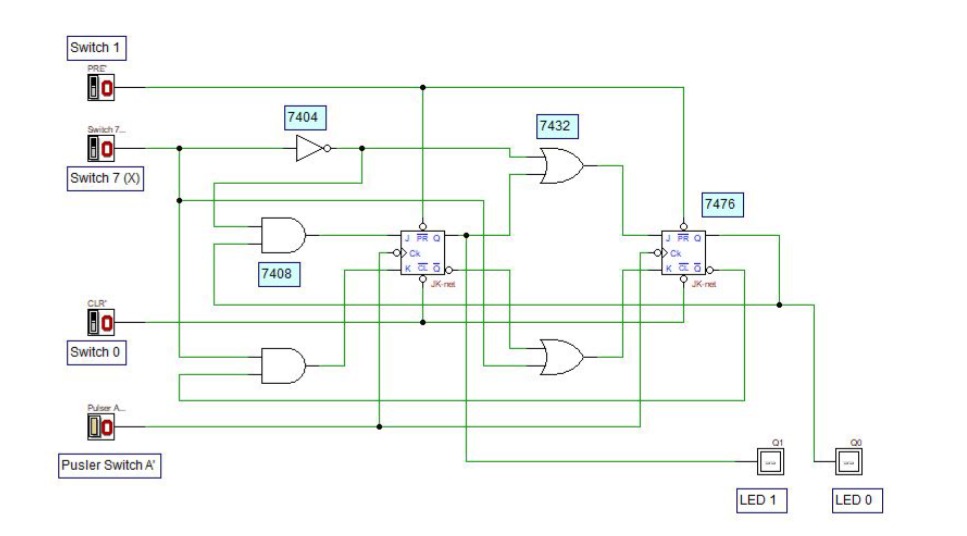
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Desired result | PRE’ | CLR’ | J | K | CLK | Q |
| Set initial value Q = 1 | **0** | **1** | **X** | **X** | **--** | **1** |
| Output Q stays the same | **1** | **1** | **0** | **0** | **⇓** | **1** |
| Output Q become 0, no change in asynchronous input | **1** | **1** | **1** | **1** | **⇓** | **0** |
| Output Q is not the previous Q | **1** | **1** | **1** | **1** | **⇓** | **1** |
| RESET Q | **1** | **1** | **0** | **1** | **⇓** | **0** |
| SET Q | **1** | **1** | **1** | **0** | **⇓** | **1** |
|  |  |  |  |  |  |  |

**2. (a) JK toggles when j is active (HIGH) and K is also active (HIGH).**

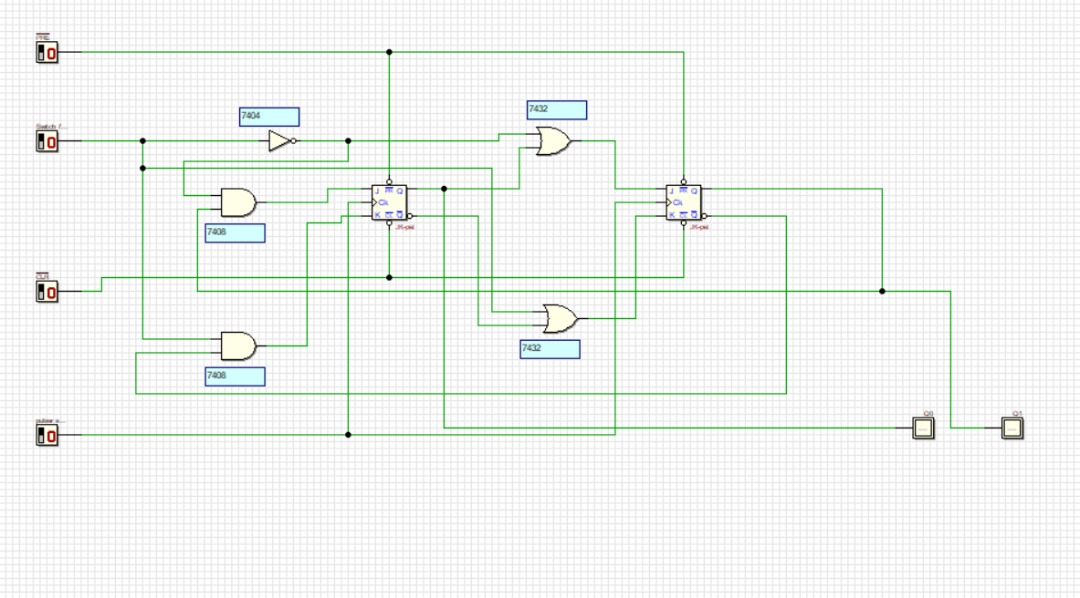
**(b) Negative edge triggered.**

**E. Lab Activities**

1.



2.

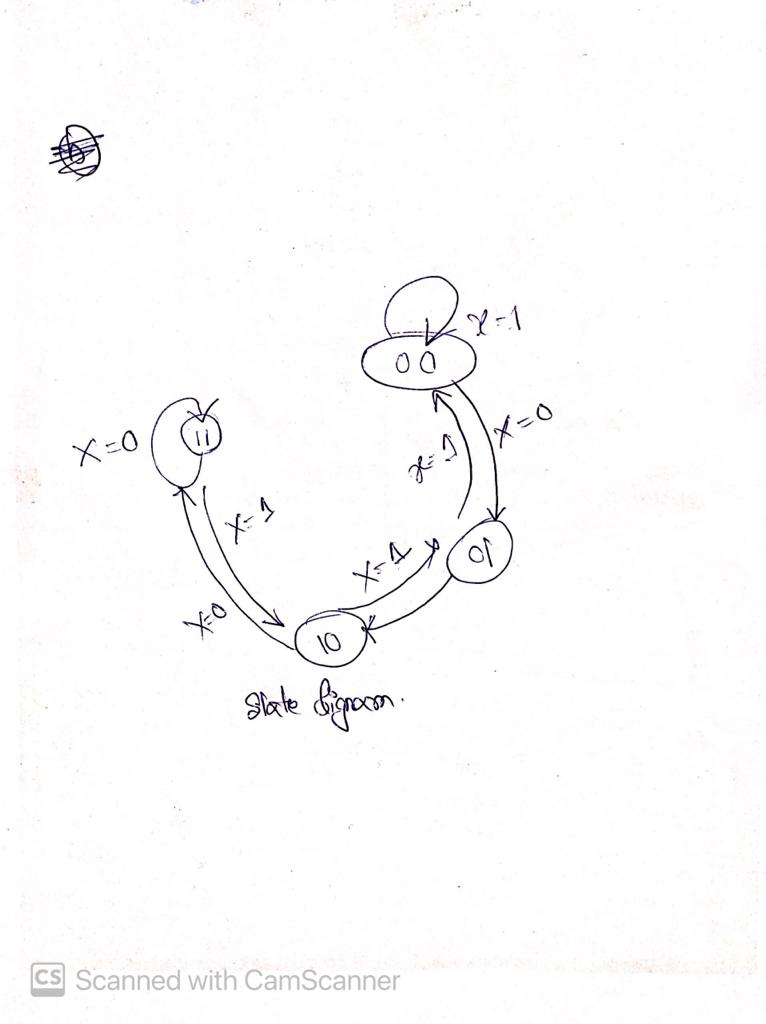
**figure 5: Asynchronous counter circuit**

3.

Table 2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Switch 7 | Present State | | Next State | |
| X | Q1  LED 1 | Q0  LED 0 | Q1  LED 1 | Q0  LED 0 |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 |

1. **State diagram**

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1. **(a) Both flip-flops are triggered with same clock simultaneously.**

**(b) There are 4 states – 00, 01, 10, 11.**

**(c) Switch 7 is count direction.**

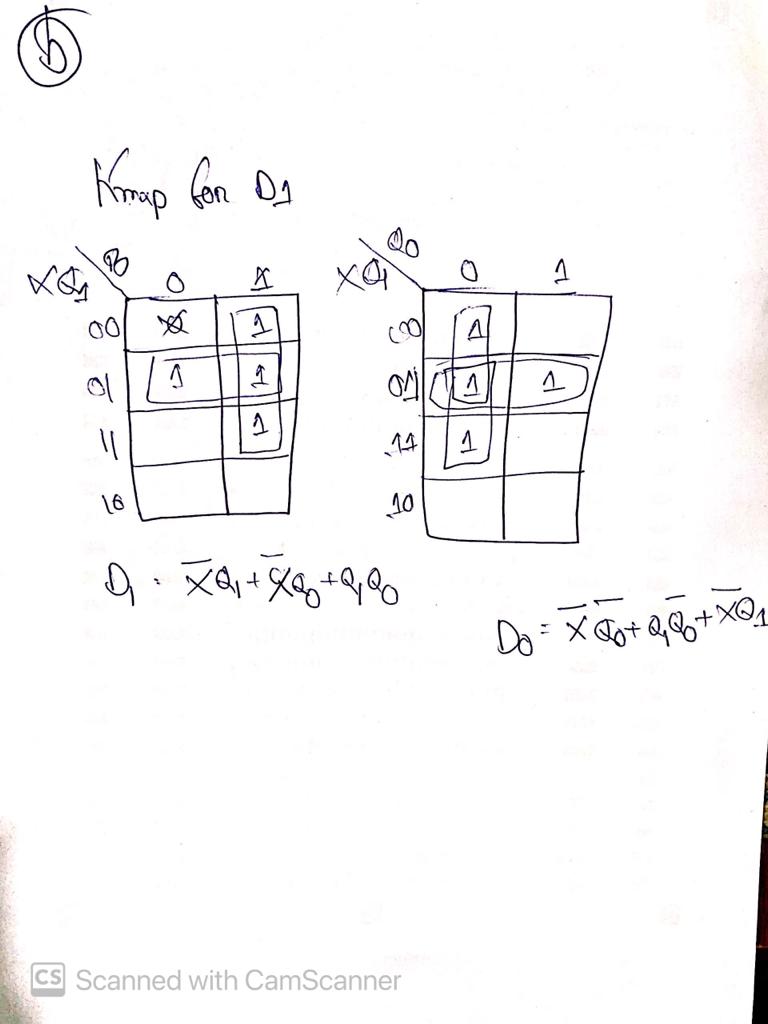
**(e) Yes, it is saturated counter.**

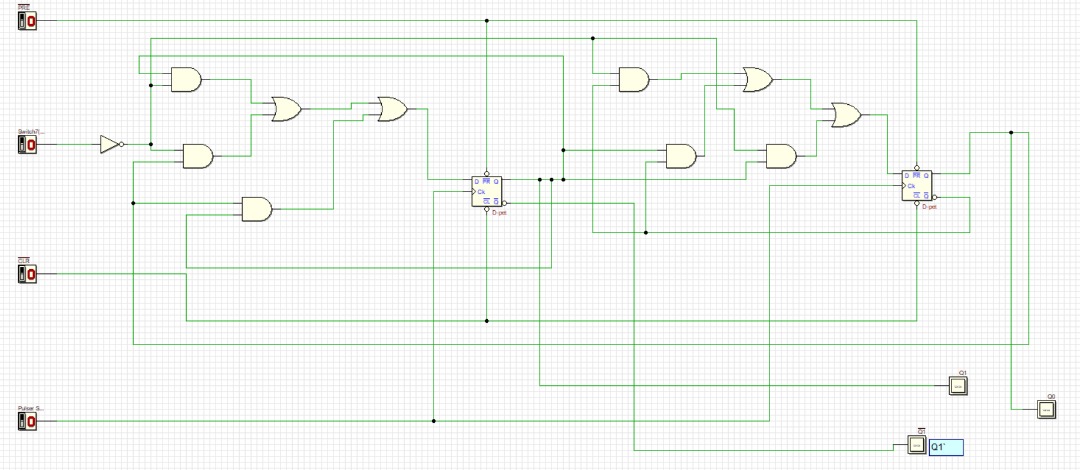
**6.**

**a)**

**Table 3**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Switch 7** | **Present State** | | **Next State** | | **D FF Transition** | |
| X | Q1  LED 1 | Q0  LED 0 | Q1  LED 1 | Q0  LED 0 | D1 | D0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

**b) **

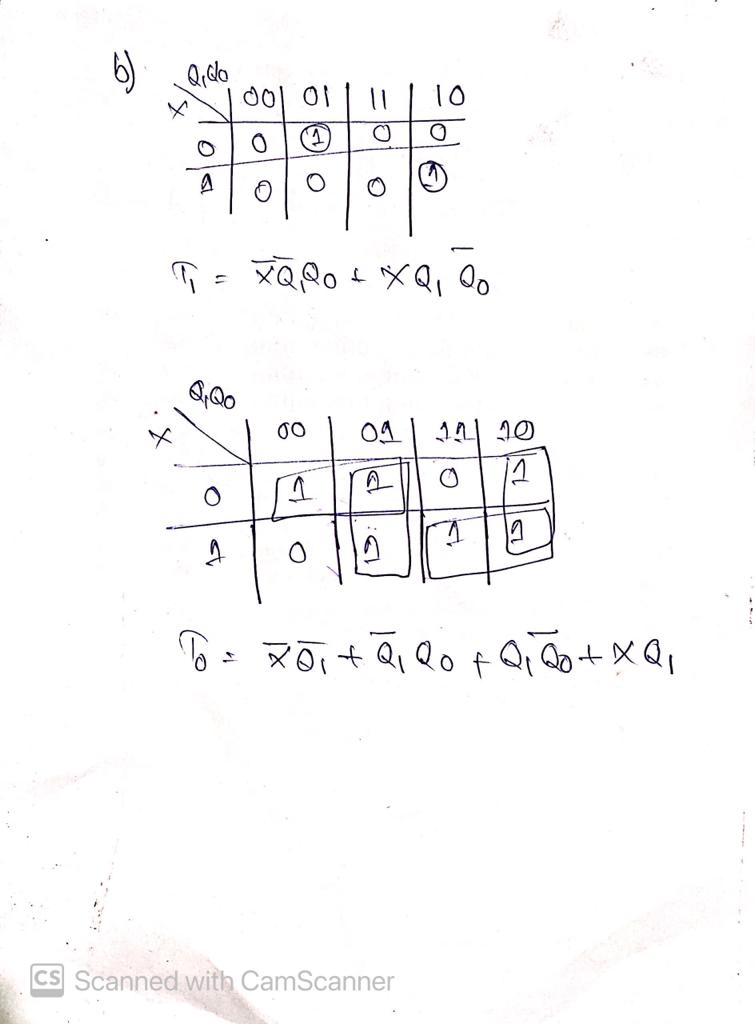
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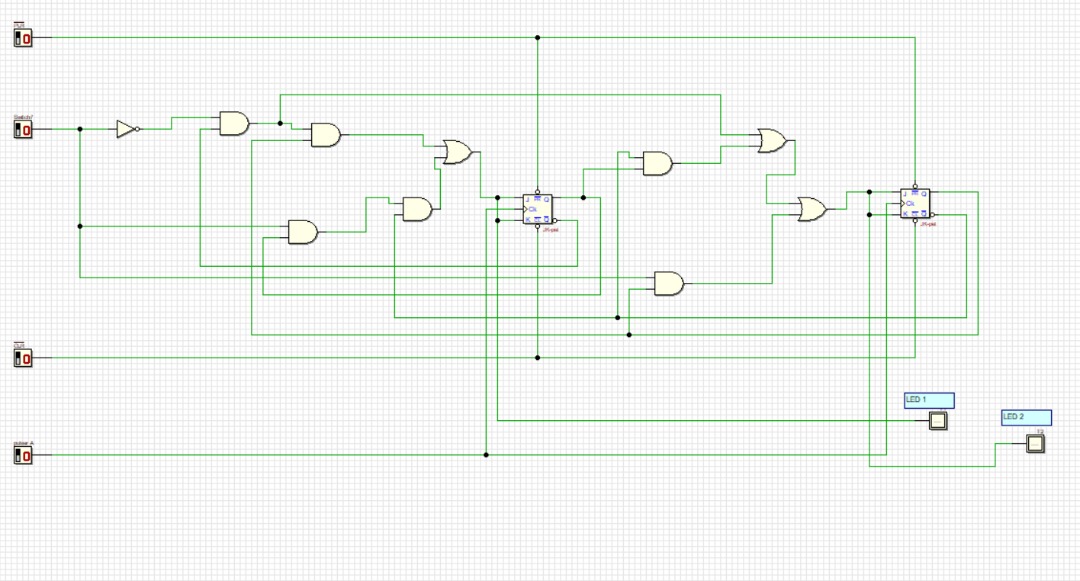
**7.**

**a)**

**Table 4**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Switch 7** | **Present State** | | **Next State** | | **D FF Transition** | |
| X | Q1  LED 1 | Q0  LED 0 | Q1  LED 1 | Q0  LED 0 | T1 | T0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 |

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