

SUBJECT: SECR1013 DIGITAL LOGIC

SESSION/SEM: 1/1

LAB 3: SYNCHRONOUS DIGITAL COUNTER

NAME 1: CHANG MIN XUAN (A20EC0024)

NAME 2: PHANG CHENG YI (A20EC0131)

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REMARKS:

MARKS:

Lab #3: Identifying the Properties of a Synchronous Counter D. Preliminary Works

1)

Table 1

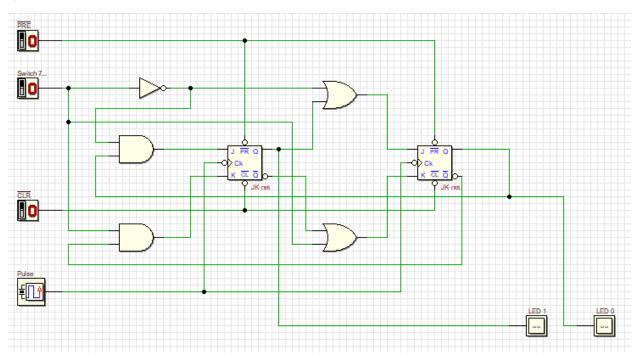
Desired Result	PRE'	CLR'	J	K	CLK	Q
Set initial value Q = 1			X	X		
Output Q stays the same	1	1	0	0	₩	1
Output Q become 0, no change in asynchronous input	1	0	X	X	₩	0
Output Q is not the previous Q	1	1	1	1	₩	1
RESET Q	1	1	0	1	₩	0
SET Q	1	1	1	0	₩	1

2)

- a) The J-K flip-flop has a toggle state of operation when both J and K inputs are HIGH while S-R flip flop don't have.
- b) The J-K flip flop in 7476 is a negative-edge triggered flip flop.

E. Lab Activities

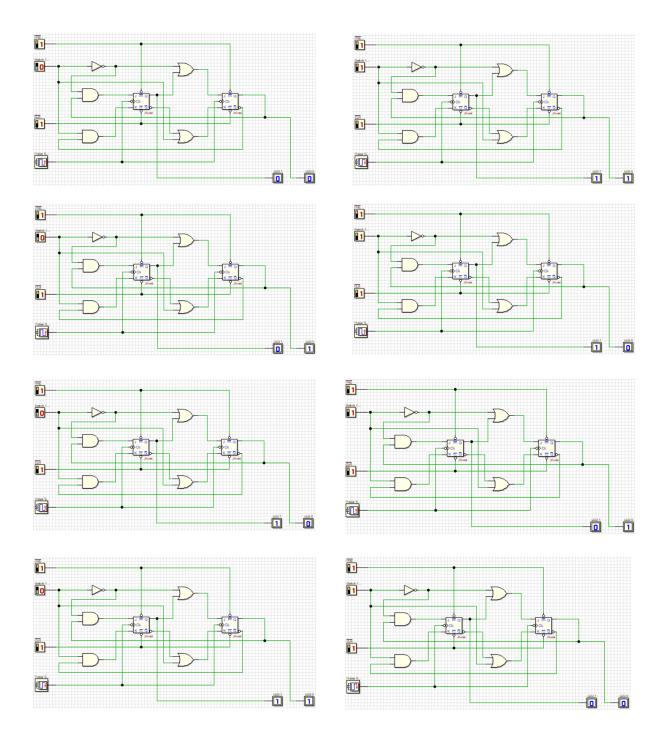
2)

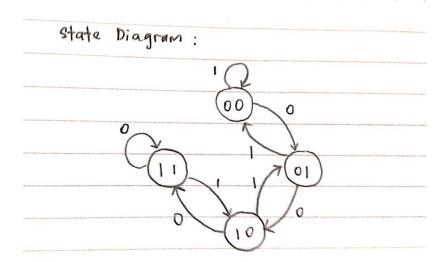


3)

Table 2

Switch 7	Present State		Next State		
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0	
0	0	0	0	1	
0	0	1	1	0	
0	1	0	1	1	
0	1	1	1	1	
1	0	0	0	0	
1	0	1	0	0	
1	1	0	0	1	
1	1	1	1	0	





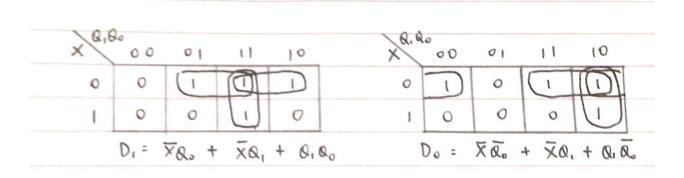
5)

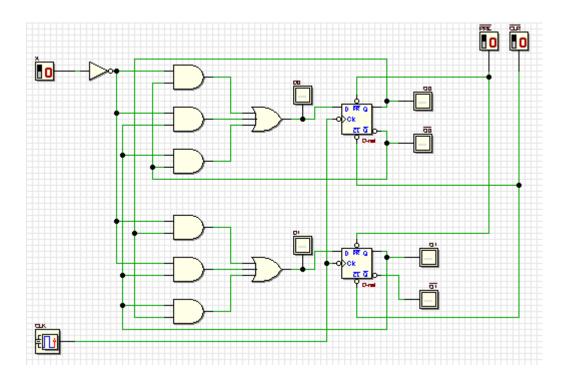
- a) The main indicator is counting sequence. The bits are changed synchronously with the same clock.
- b) There are 4 states available for the counter which includes 00, 01, 10 and 11.
- c) The function of Switch 7 (X) in the circuit is to determine the count sequence whether up or down.
- d) The function of Switch 0 and Switch 1 is act as asynchronous input. To allow the normal operation of the flip flop, both asynchronous inputs must be deactivated.
- e) The counter is saturated because the counter repeats the maximum count if count up or repeat the minimum count if count down.

Table 3

Input	Presen	Present State		Next State		D FF Transition	
X	Q1	Q0	Q1+	Q0+	D1	D0	
0	0	0	0	1	0	1	
0	0	1	1	0	1	0	
0	1	0	1	1	1	1	
0	1	1	1	1	1	1	
1	0	0	0	0	0	0	
1	0	1	0	0	0	0	
1	1	0	0	1	0	1	
1	1	1	1	0	1	0	

(b)





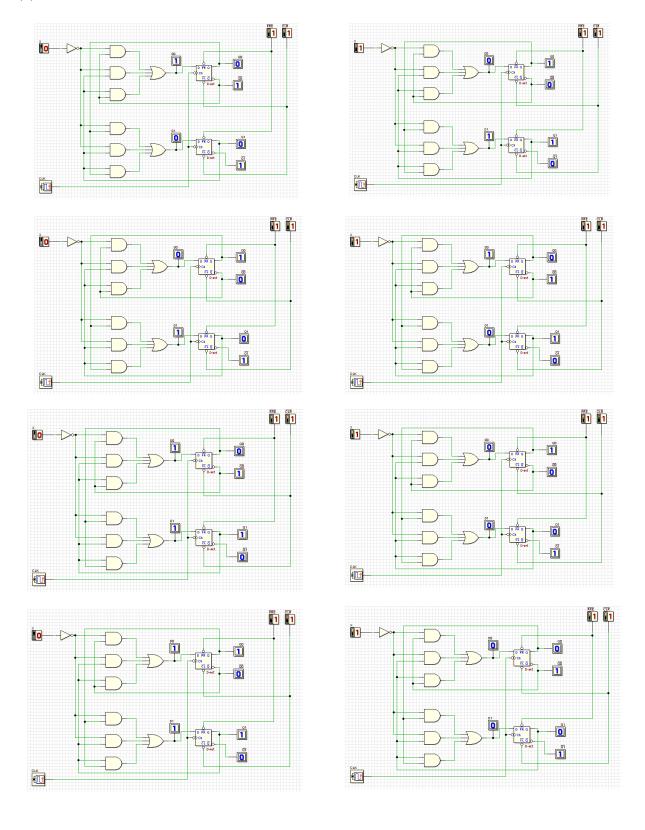
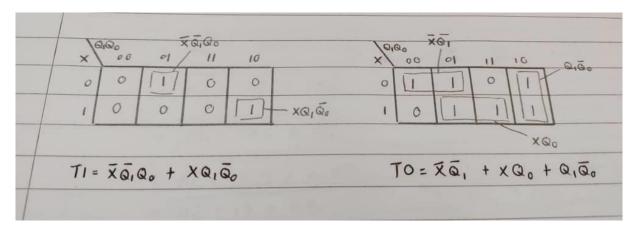


Table 4

Input X	Input X Present		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

(b)



(c)

