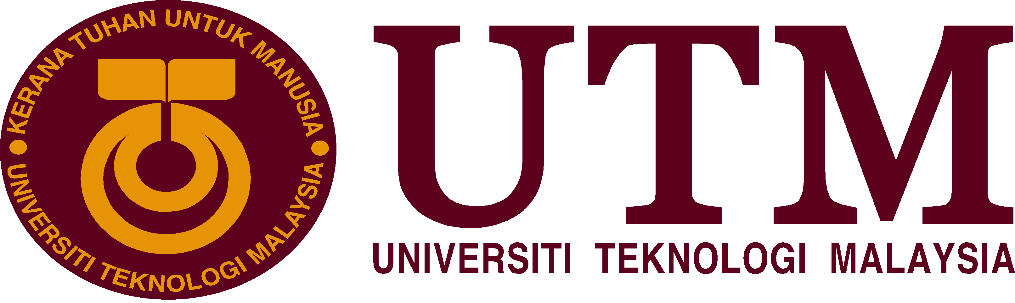
****

SUBJECT: SECR1013 DIGITAL LOGIC

SESSION/SEM: 1/1

LAB 1: COMBINATIONAL LOGIC

NAME 1: CHANG MIN XUAN (A20EC0024)

NAME 2: PHANG CHENG YI (A20EC0131)

DATE: 17/12/2020

REMARKS:

MARKS:

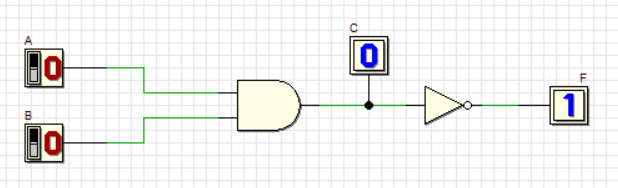
**Lab 1: Introduction to Logic Circuits**

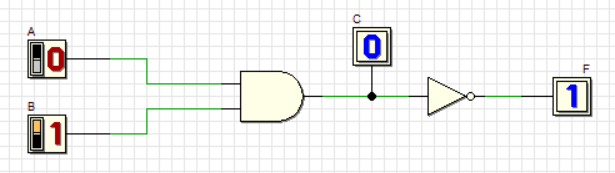
D: Preiminary Work

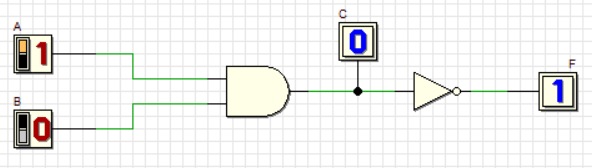
**Question 1**

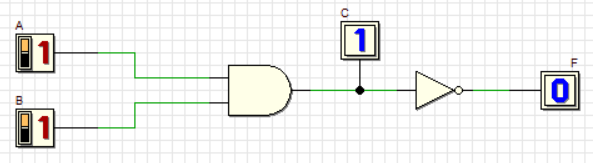
|  |  |
| --- | --- |
| Symbol: | |
| AND | NAND |
| IC Number: 7408 | IC Number: 7400 |
| Truth Table 1   |  |  |  | | --- | --- | --- | | Input | | Output | | A | B | F | | 0 | 0 | 0 | | 0 | 1 | 0 | | 1 | 0 | 0 | | 1 | 1 | 1 | | Truth Table 2   |  |  |  | | --- | --- | --- | | Input | | Output | | A | B | F | | 0 | 0 | 1 | | 0 | 1 | 1 | | 1 | 0 | 1 | | 1 | 1 | 0 | |

**Question 2**





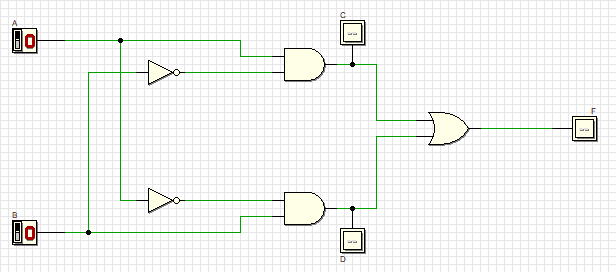




Truth Table 3:

|  |  |  |  |
| --- | --- | --- | --- |
| Input | | | Output |
| A | B | C | F |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

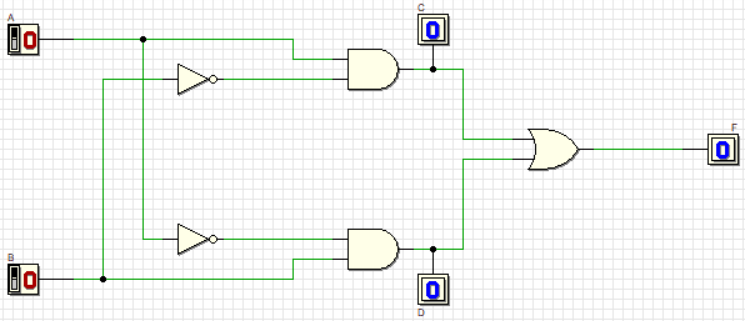
**Question 3**

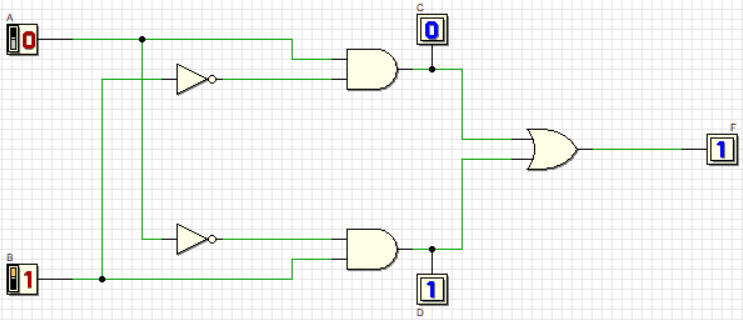


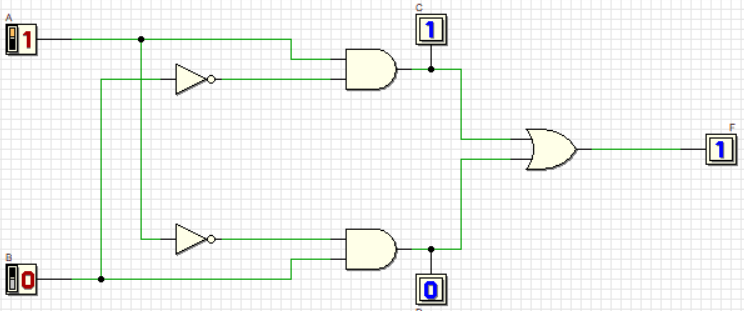
C: A.B̅

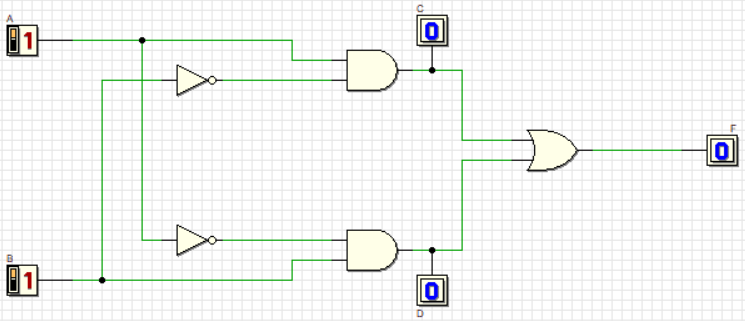
D: A̅.B

F: A.B̅ + A̅.B

**Question 4**







Truth Table 4:

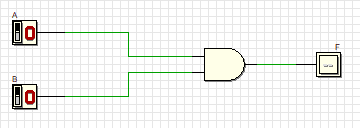
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | F |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |

E: Laboratory Work

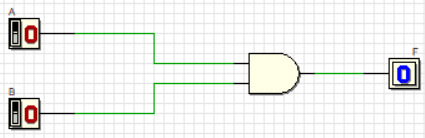
Part 1

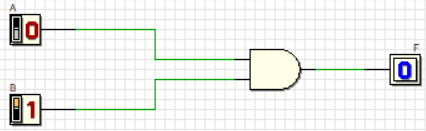
**Question 1**

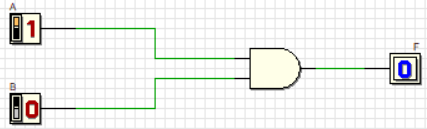
Circuit 1:

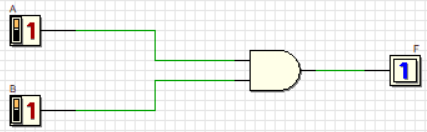


**Question 2**

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Truth Table 5:

|  |  |  |
| --- | --- | --- |
| Input | | Output |
| A | B | F |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

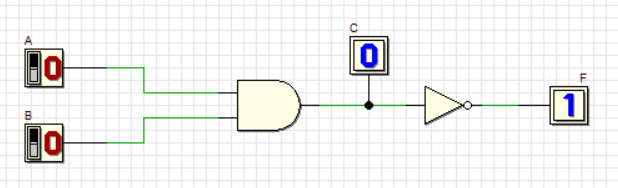
Part 2

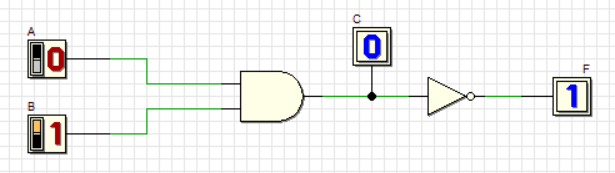
**Question 3**

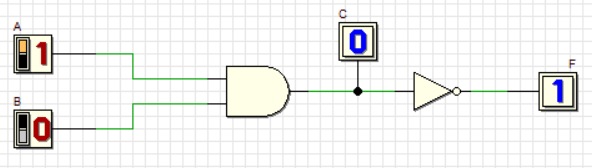
Circuit 2:

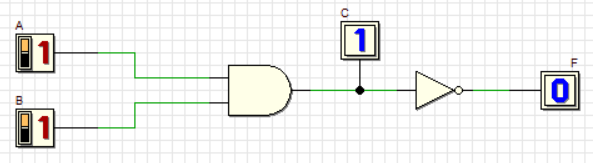


**Question 4**

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****

****



Truth Table 6:

|  |  |  |  |
| --- | --- | --- | --- |
| Input | | | Output |
| A | B | C | F |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

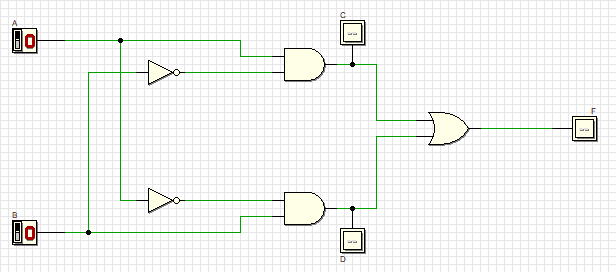
**Question 5**

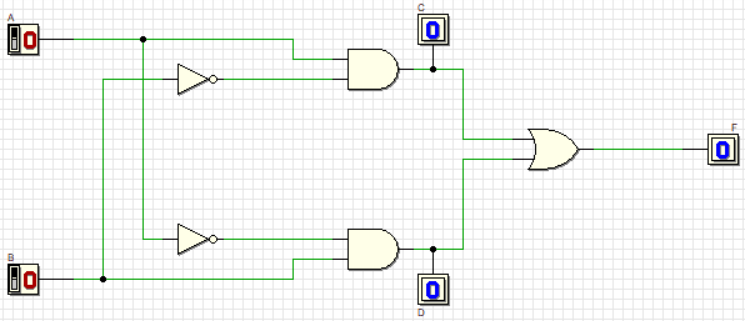
The output F of Truth Table 2 and Truth Table 6 are the same. For Truth Table 2, NAND gate is used while for Truth Table 6, the combination of AND gate and inverter which is NOT gate is used. Both types of gate show the same function.

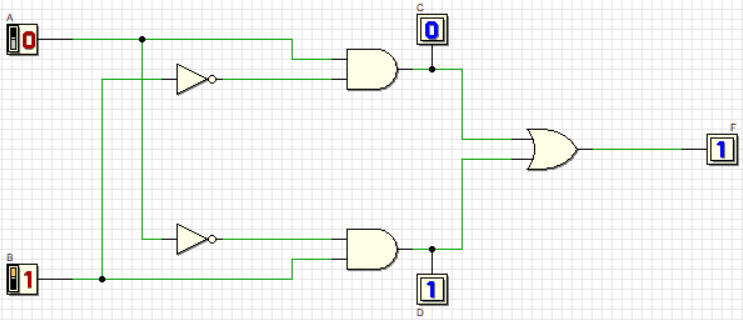
Part 3

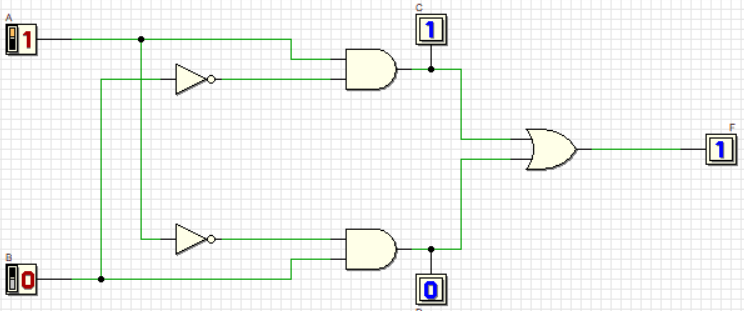
**Question 6**

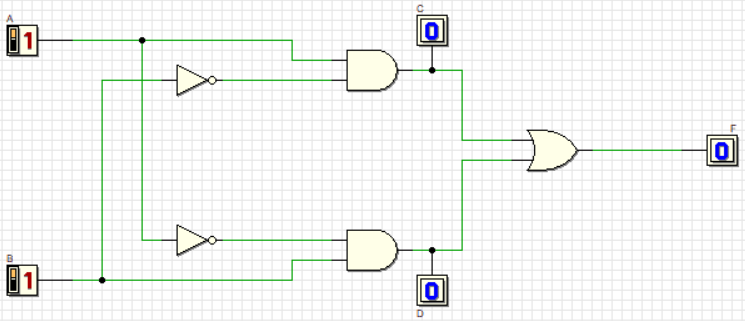
Circuit 3:



**Question 7**







Truth Table 7:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | D | F |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |

**Question 8**

The single gate represented in Circuit 3 is XOR gate which is the combination of 2 AND gates, 1 OR gate and 2 inverters. XOR gate has only two inputs and it used as a universal gate.