



**UTM**  
UNIVERSITI TEKNOLOGI MALAYSIA

**SCHOOL OF COMPUTING**  
Faculty of Engineering

# **SECR1013 DIGITAL LOGIC**

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## **Lab 3 Synchronous Digital Counter**

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Section 08

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### E. Preliminary Works

- 1) Using 7476 IC, connect the synchronous input (J, K) of a JK flip-flop to switches and its output (Q) to an LED. Connect the CLK input to a pulser switch, A. Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	J	K	CLK	Q
Set initial value Q = 1	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	↓	1
Output Q become 0, no change in asynchronous input	1	1	1	1	↓	0
Output Q is not the previous Q	1	1	1	1	↓	1
RESET Q	1	1	0	1	↓	0
SET Q	1	1	1	0	↓	1

- 2) Answer all questions.
  - a) Which state that JK flip-flop has, but not on SR flip-flop.  
Toggle
  - b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.  
Negative edge triggered flip flop.

## F. Lab Activities

- 1) You are given a counter circuit as shown in Figure 4.

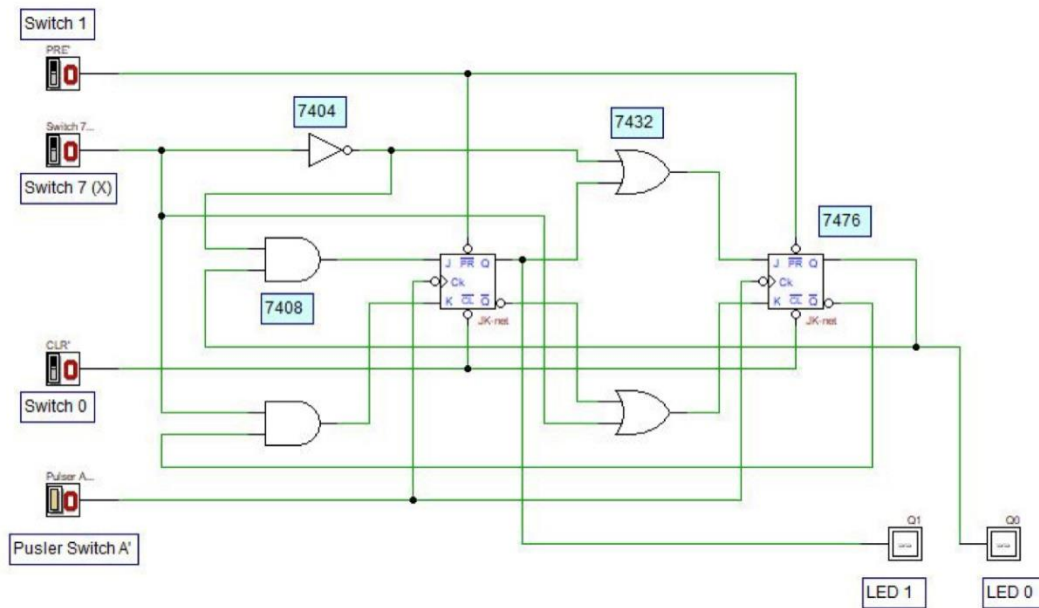


Figure 4: A Synchronous Counter Circuit

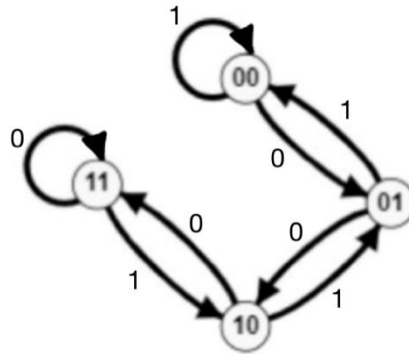
- 2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).
- 3) Investigate the behavior of the counter by observing the next state of the counter for all combination of Present State and X values. Complete the Next-State table of the counter in Table 2. Ensure the Switch 0 is in HIGH state. (0=LOW, 1=HIGH)

$$\begin{aligned} J_0 &= \bar{X} + Q_1 & J_1 &= \bar{X}Q_0 \\ K_0 &= X + \bar{Q}_1 & K_1 &= X\bar{Q}_0 \end{aligned}$$

Table 2

Switch 7	Present State		Next State	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4) By referring to the Next-State in Table 2, sketch the state diagram of the counter.



5) By referring to the Next-State in Table 2 and the state diagram in (4), answer all questions.

a) **What is the main indicator to decide that the counter is a synchronous counter?**  
Pulser Switch A.

b) **How many states are available for the counter and what are they?**  
4 states are available for the counter. They are 00, 01, 10 and 11.

c) **What is the function of Switch 7 (X) in the circuit?**  
Switch 7 (X) is the input mode selector.

d) **What is the function of Switch 0 and Switch 1 in the circuit?**  
Switch 0 is clear which is used to direct RESET the output of flip-flops.  
Switch 1 is preset which is used to direct SET the output of the flip-flops.

e) **Is the counter a saturated counter or recycle counter?**  
Recycle counter

6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3

Input X	Present State		Next State		D FF Transition	
	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

Table 3

b) Get the optimized Boolean expression.

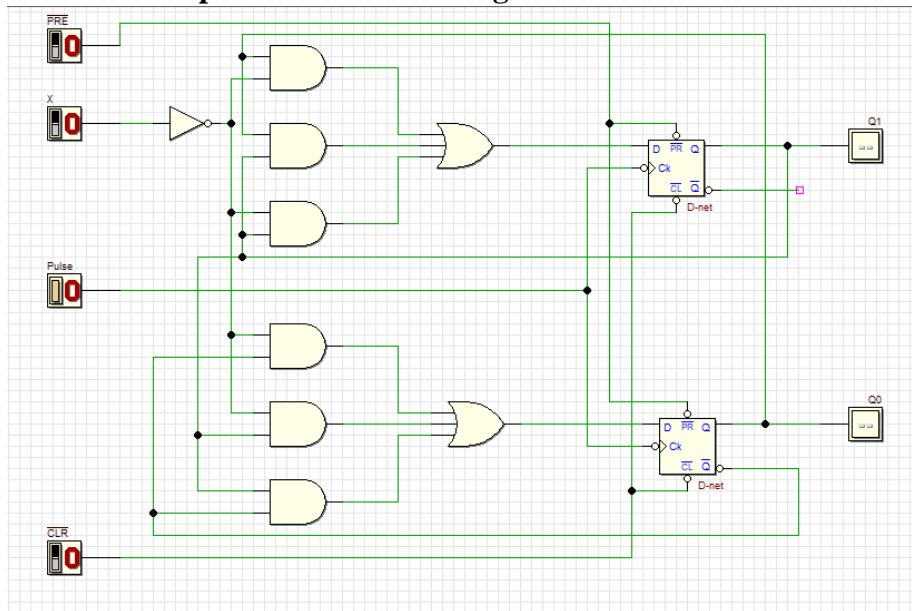
X \ Q1Q0	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$$D1 = Q1Q0 + \bar{X}Q0 + \bar{X}Q1$$

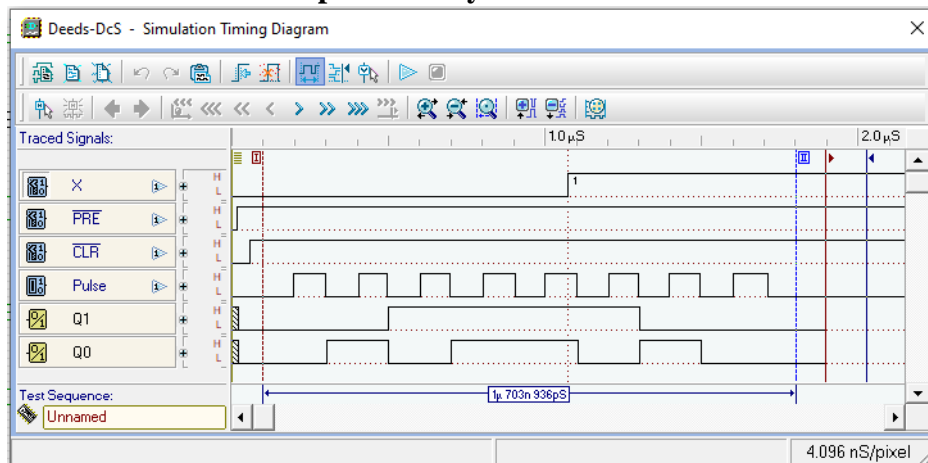
X \ Q1Q0	00	01	11	10
0	1	0	1	1
1	0	0	0	1

$$D0 = Q1\bar{Q0} + \bar{X}\bar{Q0} + \bar{X}Q1$$

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 3 is correct.



7) Repeat steps in Q(6) using T flip-flop.

a) Built the next state and transition table using the header in Table 4

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

Table 4

b) Get the optimized Boolean expression.

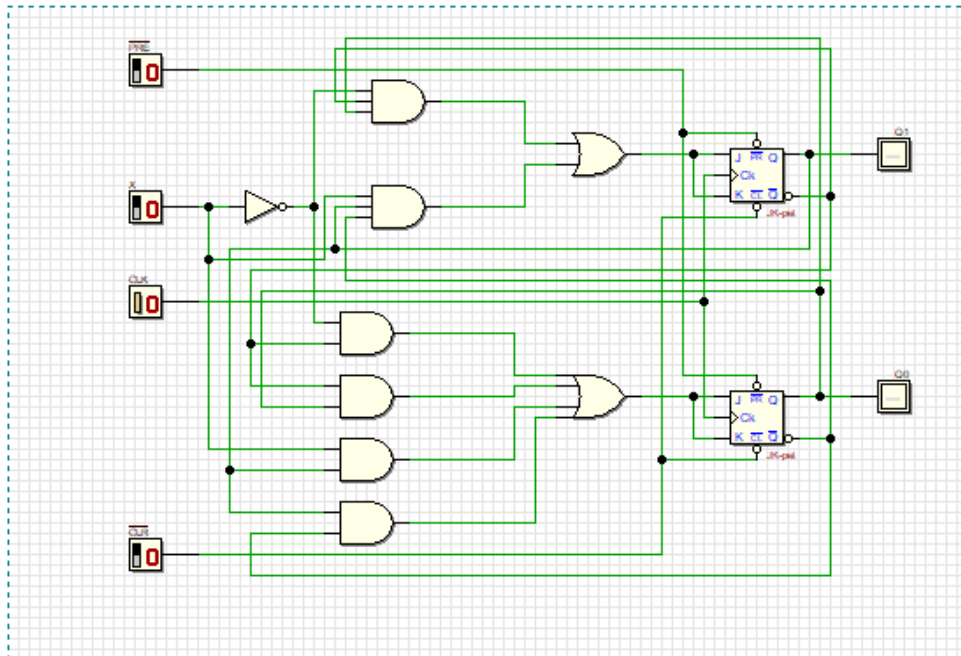
X \ Q1Q0	00	01	11	10
0	0	1	0	0
1	0	0	0	1

$$T1 = \bar{X} \bar{Q1} Q0 + X Q1 \bar{Q0}$$

X \ Q1Q0	00	01	11	10
0	1	1	0	1
1	0	1	1	1

$$T0 = \bar{X} \bar{Q1} + \bar{Q1} Q0 + X Q1 + Q1 \bar{Q0}$$

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 3 is correct.

