UTM UNIVERSITI TEKNOLOGI MALAYSIA

SCHOOL OF COMPUTING
Faculty of Engineering

SECR1013 DIGITAL LOGIC

Lab 2 Combinational Logic Circuit Design Stimulation

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Section 08

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Lab 2: COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION

D. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds. Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

Y = $AB + BC + AC$

= $AB(C + \overline{C}) + BC(A + \overline{A}) + AC(B + \overline{B})$

= $ABC + AB\overline{C} + ABC + \overline{A}BC + ABC + A\overline{B}C$

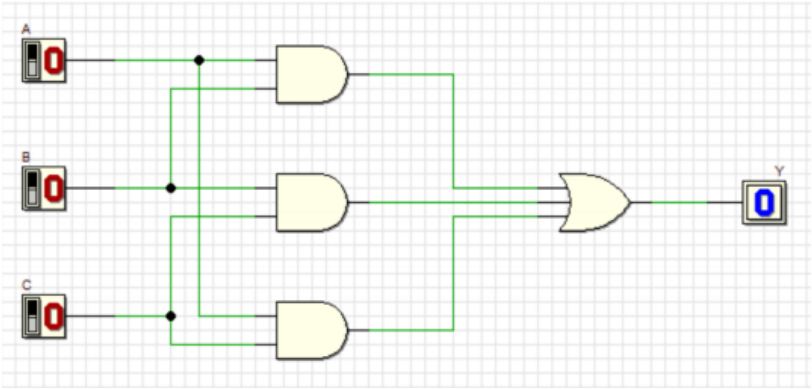
= $ABC + AB\overline{C} + \overline{A}BC + A\overline{B}C$

2. Based on standard form expression, complete the following truth table

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

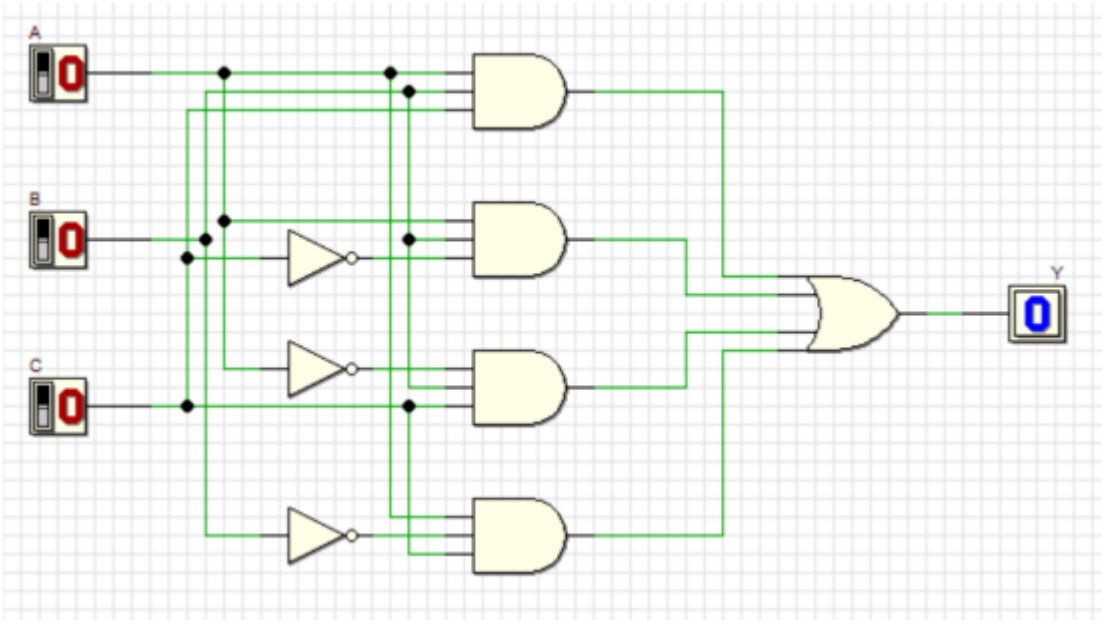
3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table. Compare the simulation result for these two truth tables. What is your conclusion?

Circuit(i)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

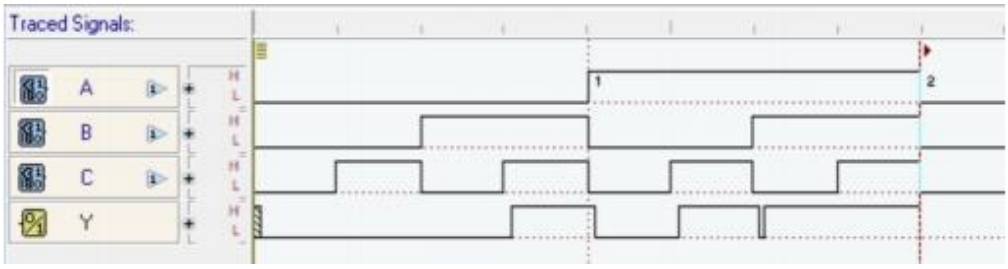
Circuit(ii)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

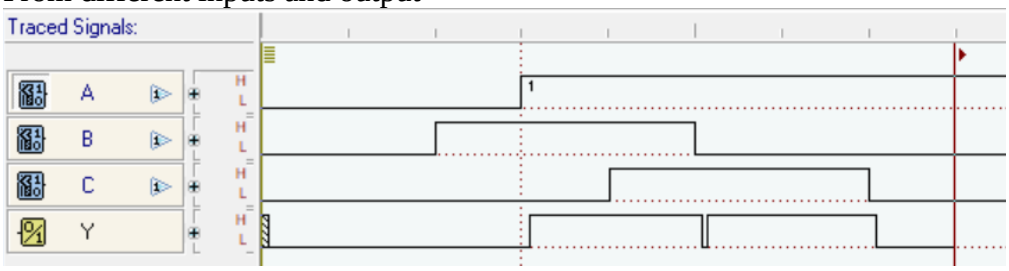
Conclusion:
Both truth table for the circuits have the same result. Circuit(i) is non-standard form while Circuit(ii) is a standard form. Standard form and non-standard form can produce the same output. Thus, non-standard form is the simple form of the standard form circuit.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.

From truth table



From different inputs and output



Part 2

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Truth Table 1

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits

AB \ CD	00	01	11	10
00	0	1	X	0
01	0	X	0	X
11	X	0	0	0
10	0	X	0	X

E1 = $\overline{A}\,\overline{B}\,D$

AB \ CD	00	01	11	10
00	1	0	X	1
01	1	X	0	X
11	X	0	0	0
10	0	X	0	X

E2 = $\overline{A}\,\overline{D}$

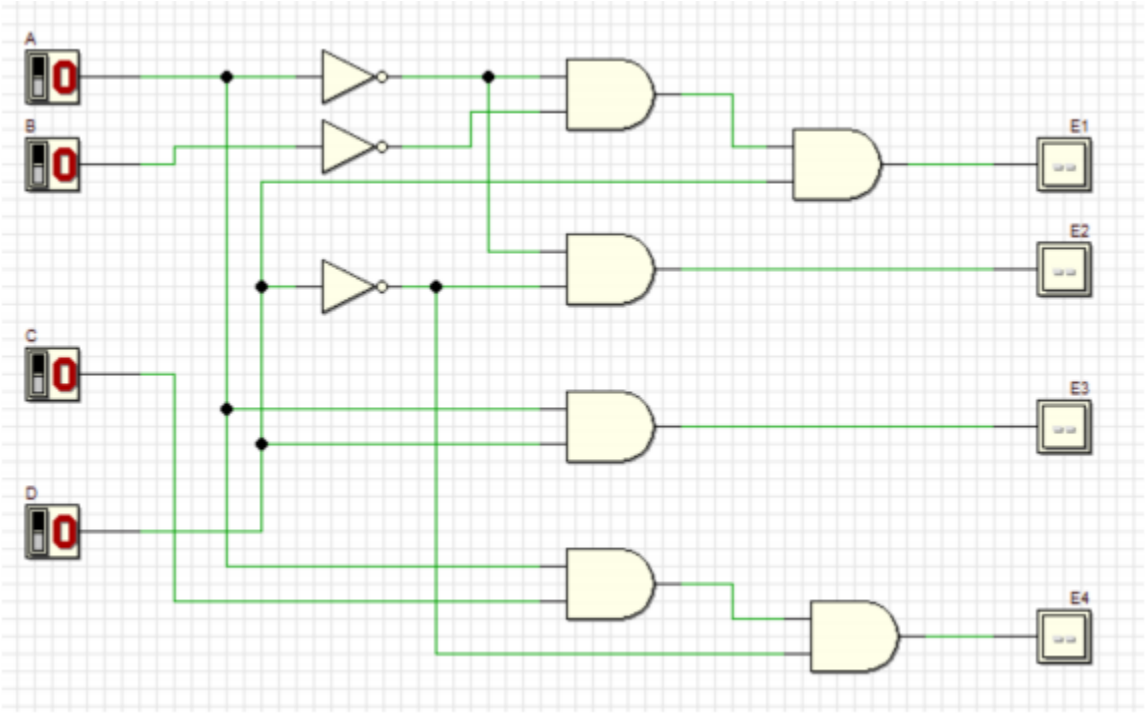
AB \ CD	00	01	11	10
00	0	0	X	0
01	0	X	0	X
11	X	1	1	0
10	0	X	1	X

E3 = AD

AB \ CD	00	01	11	10
00	0	0	X	0
01	0	X	0	X
11	X	0	0	1
10	0	X	0	X

E4 = AC$\overline{D}$

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):
a) Update Truth Table 2 based on the simulation result.

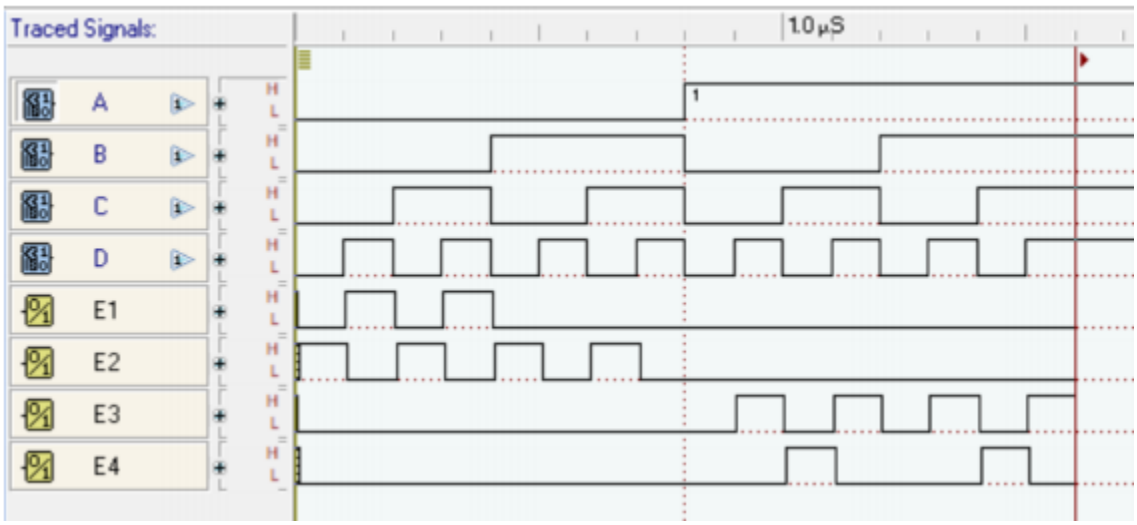
INPUT				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Truth Table 2

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

In Truth table 1, we have x (don't care term) in the output. While in Truth table 2, the don't care has be consider when construct K – map, therefore the output is 1 or 0, Thus, Truth table 2 does not have don't care, x in output. This can be accepted.

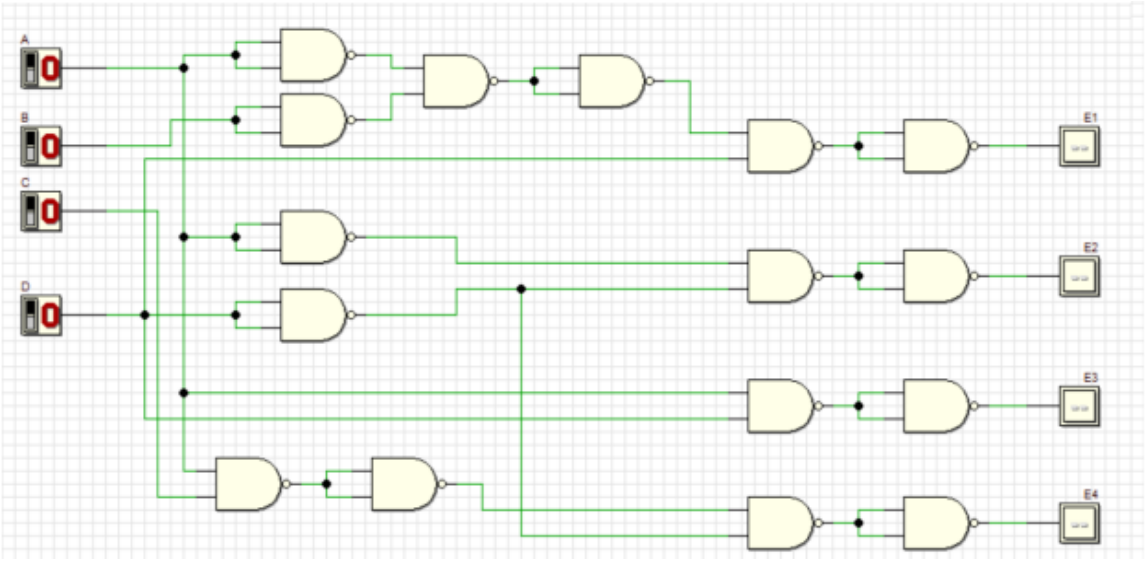
b) Timing Diagram



Explain some analysis values based on your timing diagram:

The outputs are depend on input ABCD. The output in E1 is HIGH(1) when the input ABCD is 0001 and 0011. The output in E2 is HIGH(1) when the input ABCD is 0000, 0010, 0100 and 0110. The output in E3 is HIGH(1) when the input ABCD is 1001, 1011, 1101 and 1111. The output in E4 is HIGH(1) when the input ABCD is 1010 and 1110.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):
a) Update Truth Table 3 based on the simulation result.

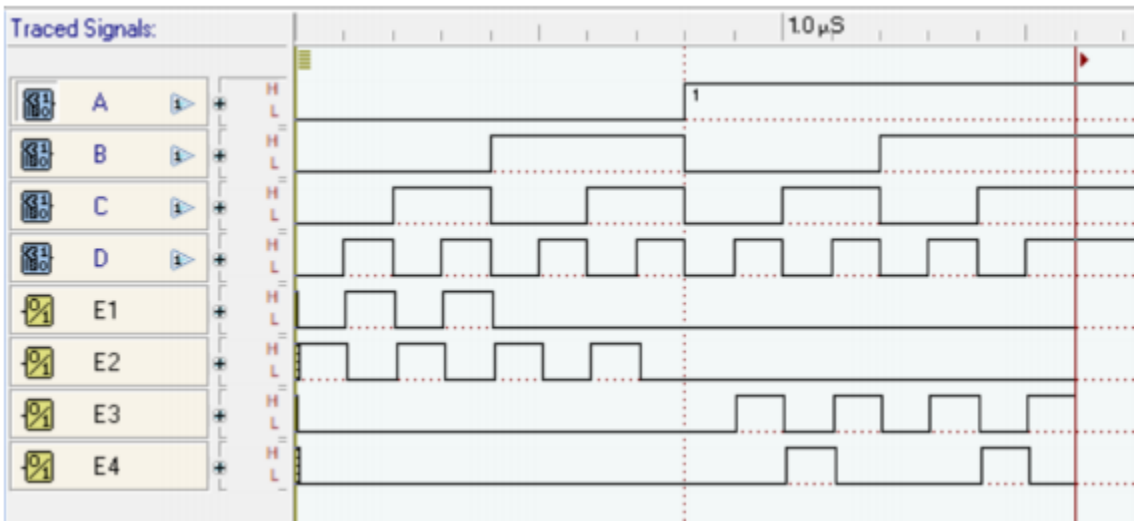
INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Truth Table 3

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

The output result in Truth Table 2 and Truth Table 3 are the same for E1, E2, E3 and E4. Therefore, it can be concluded that the circuit with AND, OR, NOT gate can be replaces by using NAND gate. NAND gate is an universal gate is proved.

Timing Diagram:



Explain some analysis values based on your timing diagram:

This timing diagram is same as the timing diagram for the previous circuit in 4(b). Therefore the circuit is equivalent although different gates is used. The outputs is depend on the input ABCD. The output in E1 is HIGH(1) when the input ABCD is 0001 and 0011. The output in E2 is HIGH(1) when the input ABCD is 0000, 0010, 0100 and 0110. The output in E3 is HIGH(1) when the input ABCD is 1001, 1011, 1101 and 1111. The output in E4 is HIGH(1) when the input ABCD is 1010 and 1110.