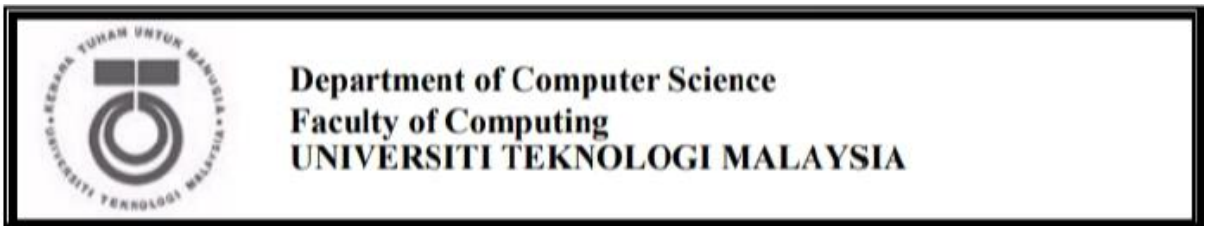


SUBJECT: SECR1013 DIGITAL LOGIC

SESSION/SEMESTER: 01/2020 2021

LAB 1: COMBINATIONAL LOGIC

NAME 1: YASSER EHAB MOHIELDIN FAHMY (A17CS3013)

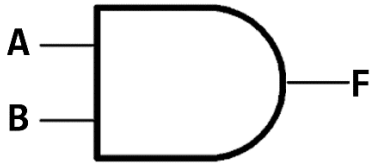
NAME 2: SAYANG ELYIANA AMIERA BINTI HELMEY (A20EC0143)

Preliminary Work:

1.

AND

Symbol:



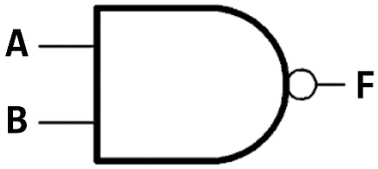
IC Number: 7408 Quad 2-input AND

Truth Table 1:

Input		Output
A	**B**	**F**
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

NAND

Symbol:

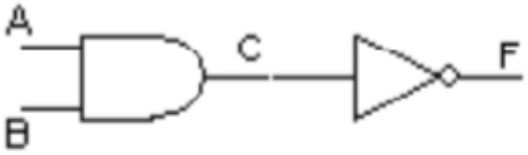


IC Number: 7400 Quad 2-input NAND

Truth Table 2:

Input		Output
A	**B**	**F**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

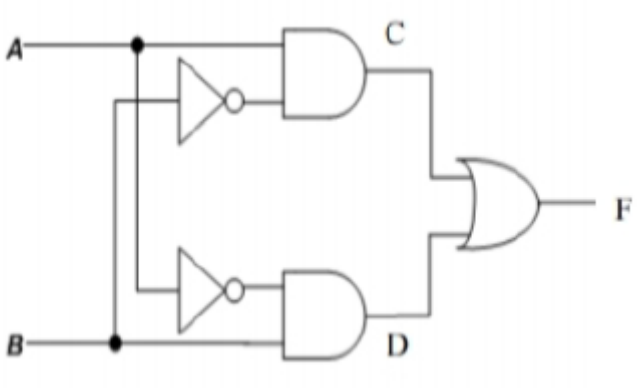
2.



Truth Table 3

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

3.



$C = A \bullet \overline{B}$

$D = \overline{A} \bullet B$

$F = C + D$

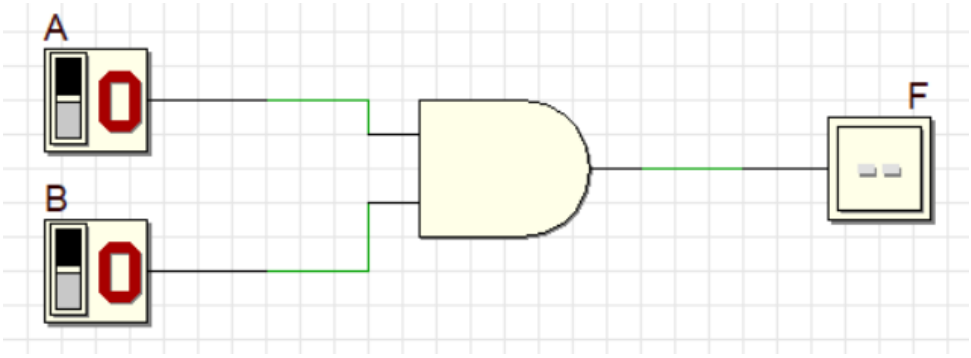
4. Truth Table 4

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

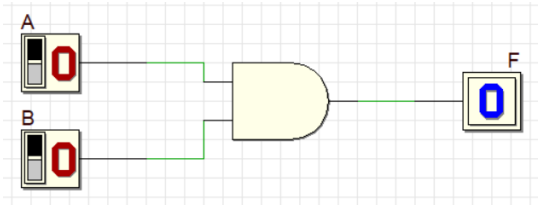
Laboratory Work:

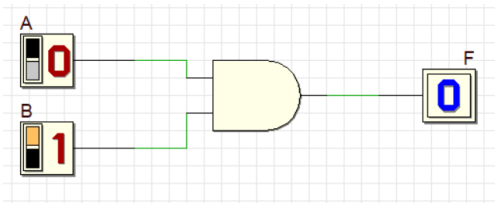
Part 1:

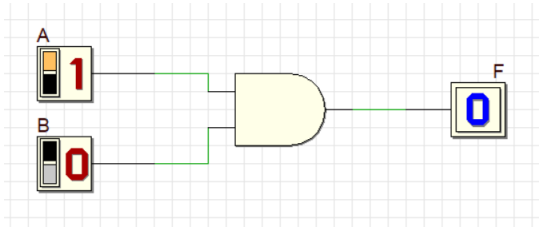
1. Circuit 1

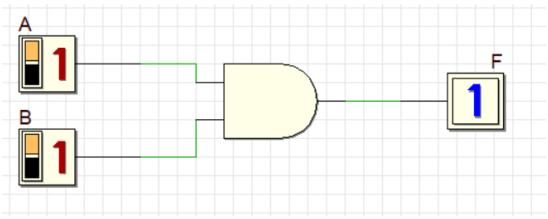


2.







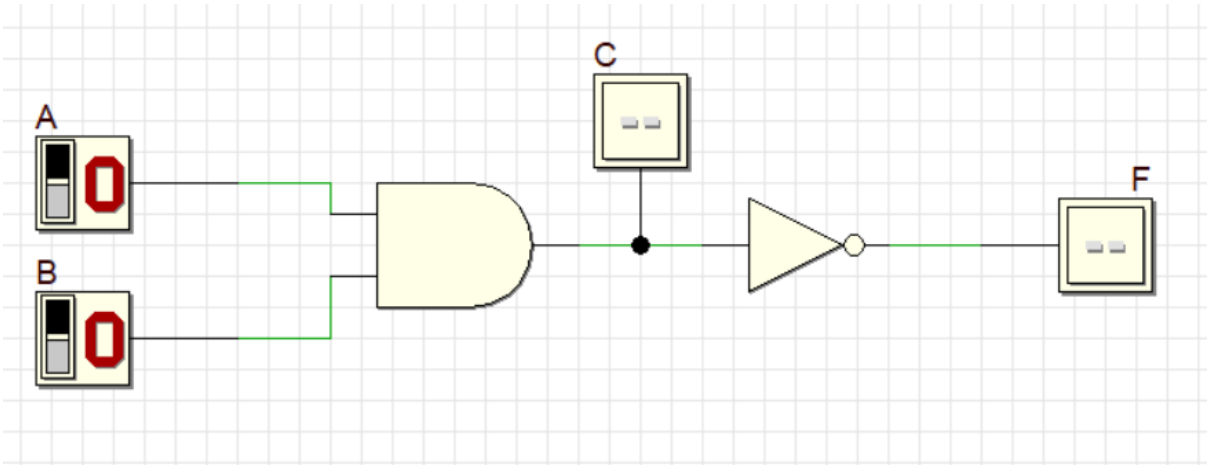


Truth Table 5

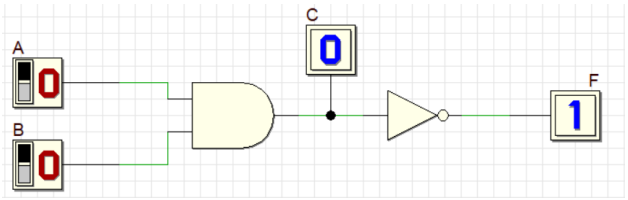
Input		Output
A	**B**	**F**
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

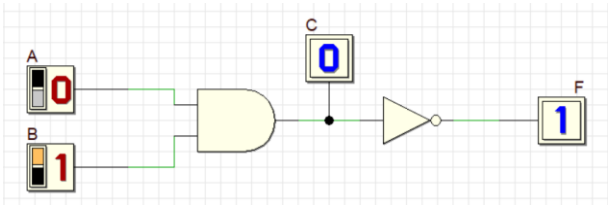
Part 2:

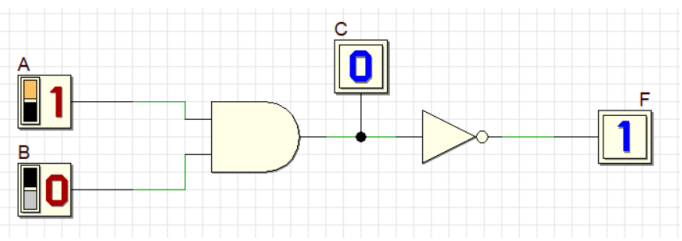
3. Circuit 2

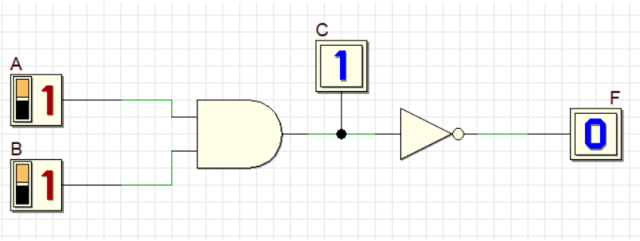


4. .









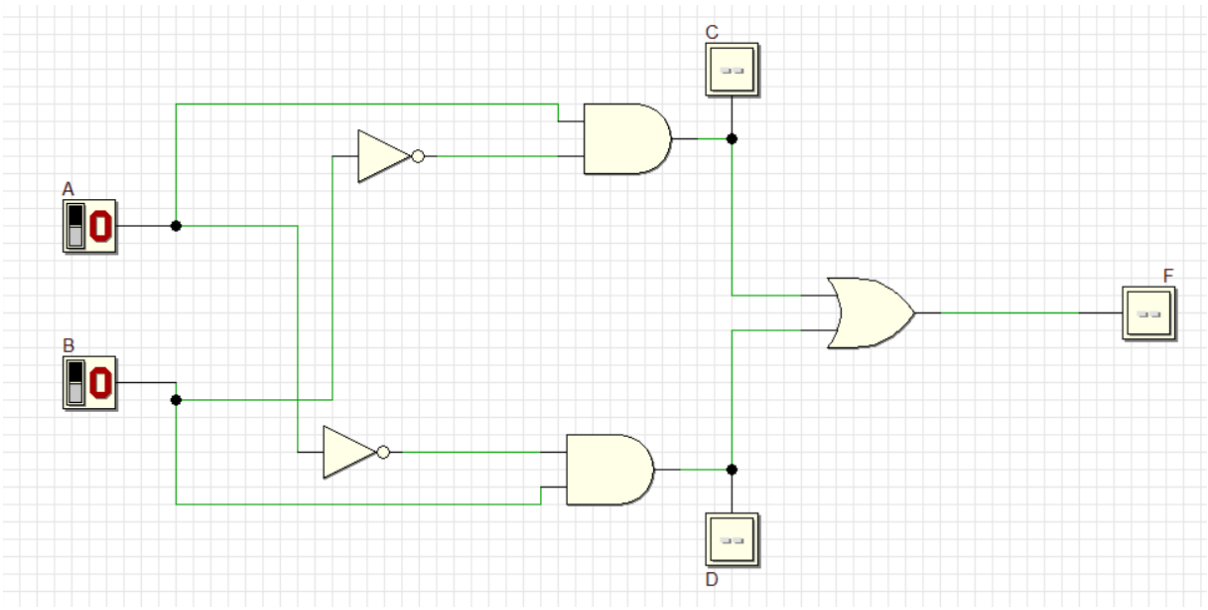
Truth Table 6

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

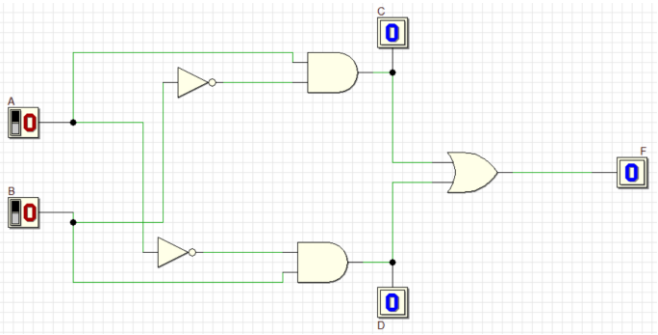
5. Truth table 6 shows the inputs and outputs of the AND gate that is then connected to a NOT inverter (NOT-AND), this is the same as the outputs of truth table 2 which is a NAND gate. Thus, we can conclude that NOT-AND could be simplified as NAND.

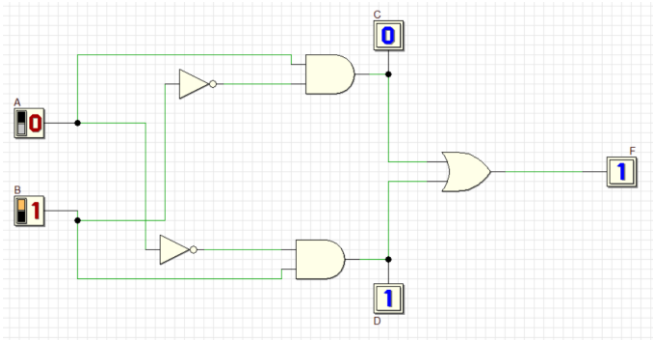
Part 3:

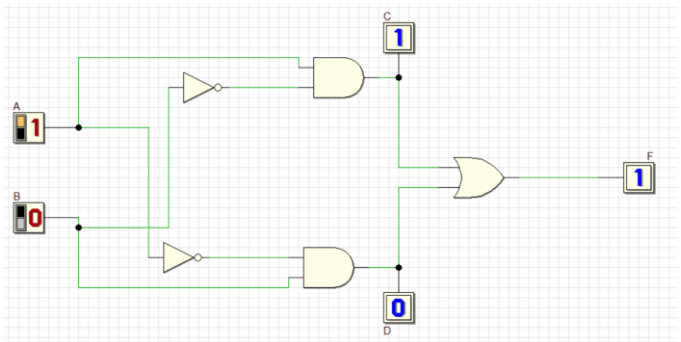
6. Circuit 3

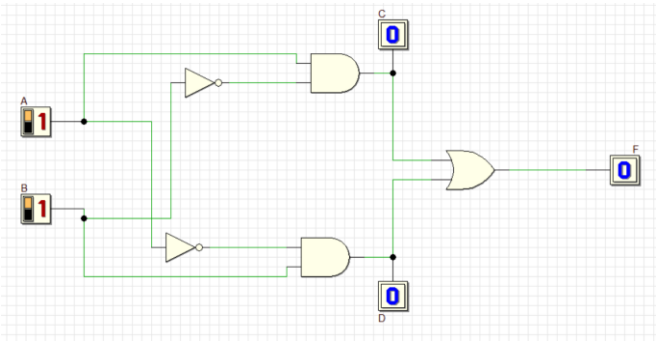


7.





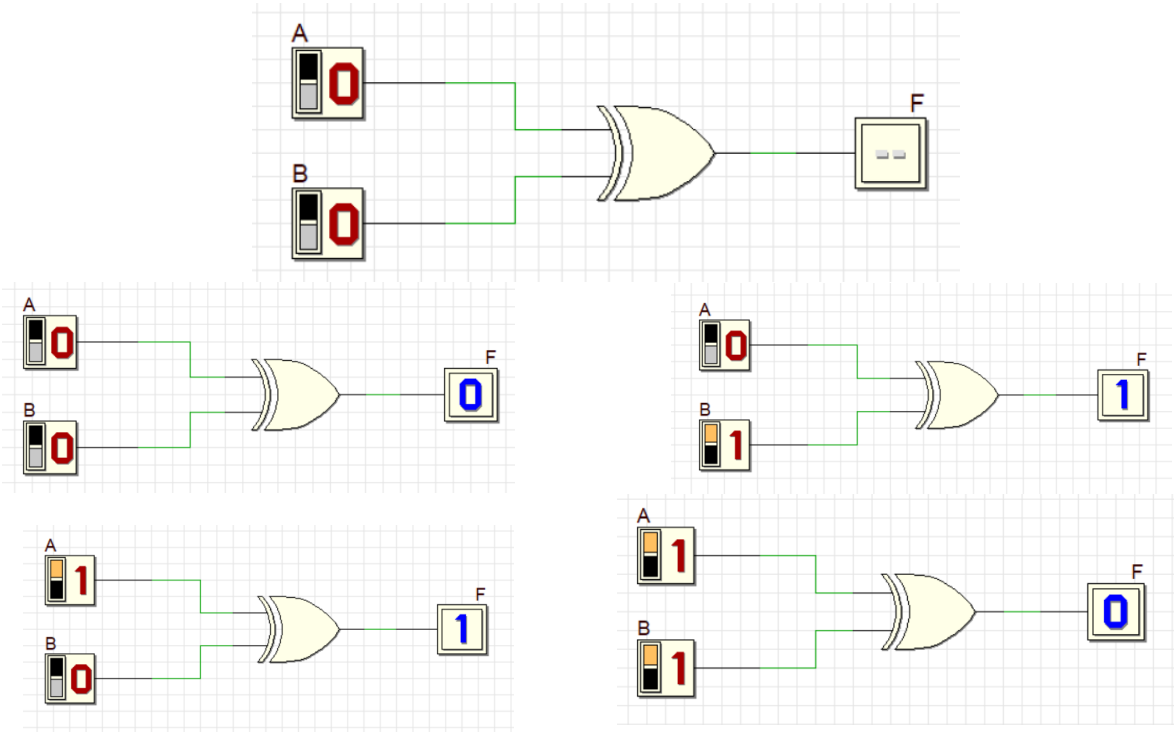




Truth Table 7

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

8. Circuit 3 represents XOR gate



Truth table for XOR:

Input		**Output**
A	**B**	**F**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**