



**School of Computing**  
**Faculty of Engineering**  
**UNIVERSITI TEKNOLOGI MALAYSIA**

**SUBJECT** : SECR1013 DIGITAL LOGIC

**SESSION/SEM** : SEMESTER 1  
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**LAB 3** : SYNCHRONOUS DIGITAL COUNTER

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**DATE** : 28/1/2021  
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### **Lab #3**

#### **Identifying the Properties of a Synchronous Counter**

##### **A. Aims**

- 1) Expose the student with experience on constructing synchronous counter circuit using Flip-Flop IC, Basic Gate ICs, Breadboard and ETS-5000 Digital Kit.
- 2) Promote critical thinking among students by analysing the given circuit and identifying the behaviour of the digital circuit.

##### **B. Objectives**

The objectives of this lab activity are to:

- 1) Implement a synchronous counter circuit into physical circuit using Breadboard, Flip-Flops, Basic Gates and Switches.
- 2) Completing the next-state table of the counter circuit.
- 3) Sketch the state diagram of the counter circuit.
- 4) Identify the properties of the counter.

##### **C. Materials And Equipment**

Materials and equipment required for this lab are as follows:

| <b>Item Name</b>           | <b>Number of Item</b> |
|----------------------------|-----------------------|
| 1. Breadboard              | 1                     |
| 2. 7408 Quad 2-Input AND   | 1                     |
| 3. 7404 Hex Inverter       | 1                     |
| 4. 7432 Quad 2-input OR    | 1                     |
| 5. 7476 Dual J-K Flip Flop | 1                     |
| 6. ETS-5000 Digital Kit    | 1                     |

#### D. Preliminary Works

- 1) Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

**Table 1**

| Desired Result                                     | $\overline{PRE}$ | $\overline{CLR}$ | J | K | CLK | Q |
|----------------------------------------------------|------------------|------------------|---|---|-----|---|
| Set initial value Q = 1                            | 0                | 1                | X | X | --  | 1 |
| Output Q stays the same                            | 1                | 1                | 0 | 0 | ↓   | 1 |
| Output Q become 0, no change in asynchronous input | 1                | 1                | 0 | 1 | ↓   | 0 |
| Output Q is not the previous Q                     | 1                | 1                | 1 | 1 | ↓   | 1 |
| RESET Q                                            | 1                | 1                | 0 | 1 | ↓   | 0 |
| SET Q                                              | 1                | 1                | 1 | 0 | ↓   | 1 |

- 2) Answer all questions.

- a) Which state that JK flip-flop has, but not on SR flip-flop.

Toggle state.

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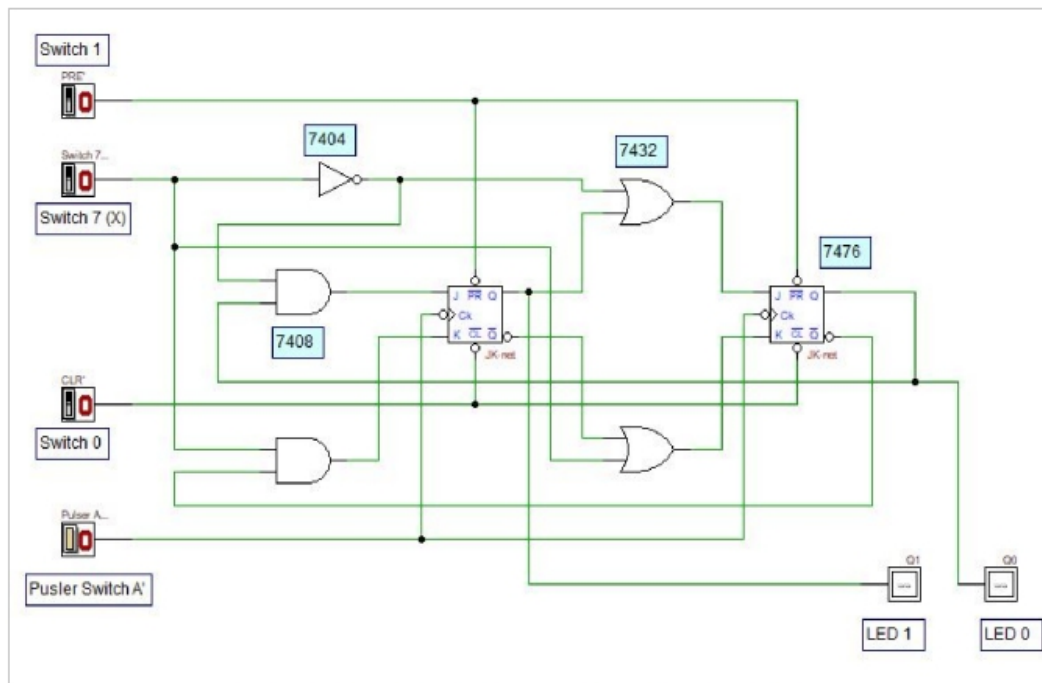
- b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

Negative-edge triggered flip flop.

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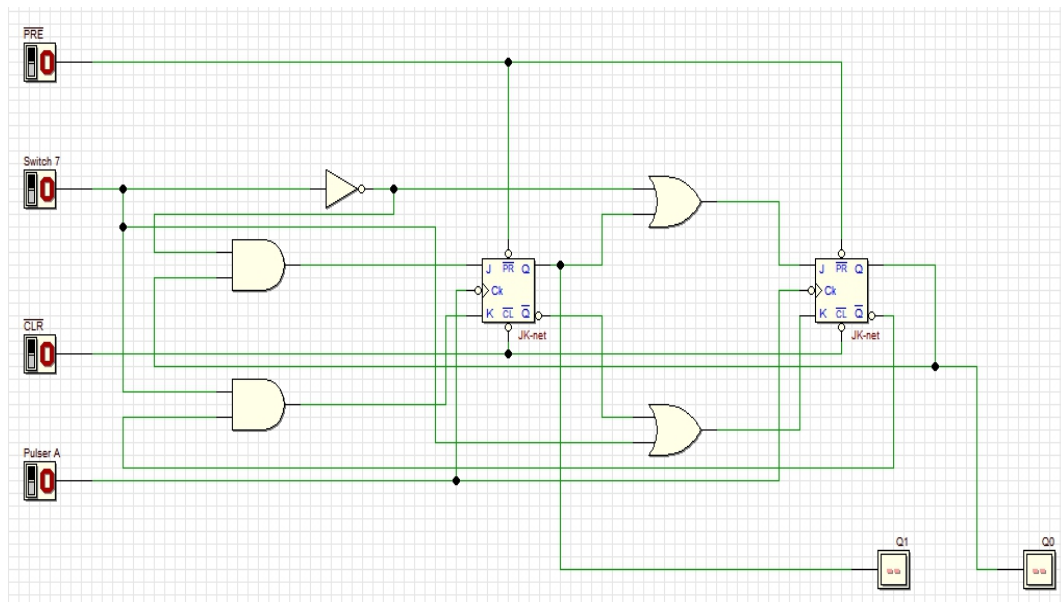
## E. Lab Activities

1) You are given a counter circuit as shown in Figure 4.



**Figure 4: A Synchronous Counter Circuit**

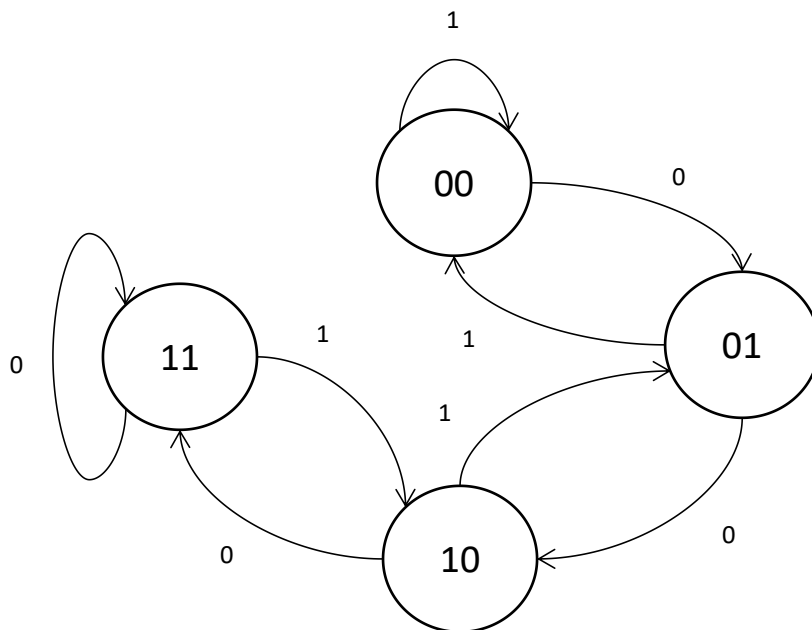
2) By using all the materials and equipment's listed in section C, construct the physical circuit of Figure 4.(Make sure all ICs are connected to Vcc and GND).



3) Investigate the behaviour of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the *NextState* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state.  
(0=LOW, 1=HIGH)

| Switch 7 | Present State |             | Next State  |             |
|----------|---------------|-------------|-------------|-------------|
| X        | Q1<br>LED 1   | Q0<br>LED 0 | Q1<br>LED 1 | Q0<br>LED 0 |
| 0        | 0             | 0           | 0           | 1           |
| 0        | 0             | 1           | 1           | 0           |
| 0        | 1             | 0           | 1           | 1           |
| 0        | 1             | 1           | 1           | 1           |
| 1        | 0             | 0           | 0           | 0           |
| 1        | 0             | 1           | 0           | 0           |
| 1        | 1             | 0           | 0           | 1           |
| 1        | 1             | 1           | 1           | 0           |

4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

- a) What is the main indicator to decide that the counter is a synchronous counter?  
The clock decides that the counter is a synchronous counter because the clock in Figure 4 circuit is from the same source.
- b) How many states are available for the counter and what are they?  
4 states which are state 00, 01, 10 and 11.
- c) What is the function of Switch 7 (X) in the circuit?  
The function of Switch 7 (X) is to indicate the direction of counter either it is counter up or counter down.
- d) What is the function of Switch 0 and Switch 1 in the circuit?  
The function of Switch 0 is to reset the output to 0 while the function of Switch 1 is to set the initial value of 1 to the output.
- e) Is the counter a saturated counter or recycle counter?  
The counter is a saturated counter.

6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Build the next state and transition table using the header in Table 3

| Input | Present State |    | Next State |     | D FF Transition |    |
|-------|---------------|----|------------|-----|-----------------|----|
| X     | Q1            | Q0 | Q1+        | Q0+ | D1              | D0 |
| 0     | 0             | 0  | 0          | 1   | 0               | 1  |
| 0     | 0             | 1  | 1          | 0   | 1               | 0  |
| 0     | 1             | 0  | 1          | 1   | 1               | 1  |
| 0     | 1             | 1  | 1          | 1   | 1               | 1  |
| 1     | 0             | 0  | 0          | 0   | 0               | 0  |
| 1     | 0             | 1  | 0          | 0   | 0               | 0  |
| 1     | 1             | 0  | 0          | 1   | 0               | 1  |
| 1     | 1             | 1  | 1          | 0   | 1               | 0  |

b) Get the optimized Boolean expression.

|   |   |      |    |    |    |
|---|---|------|----|----|----|
|   |   | Q1Q0 |    |    |    |
|   |   | 00   | 01 | 11 | 10 |
| X | 0 | 0    | 1  | 1  | 1  |
|   | 1 | 0    | 0  | 1  | 0  |

$$001,011 = X'Q0$$

$$011,010 = X'Q1$$

$$011,111 = Q1Q0$$

$$D1 = X'Q0 + X'Q1 + Q1Q0$$

|   |   |      |    |    |    |
|---|---|------|----|----|----|
|   |   | Q1Q0 |    |    |    |
|   |   | 00   | 01 | 11 | 10 |
| X | 0 | 1    | 0  | 1  | 1  |
|   | 1 | 0    | 0  | 0  | 1  |

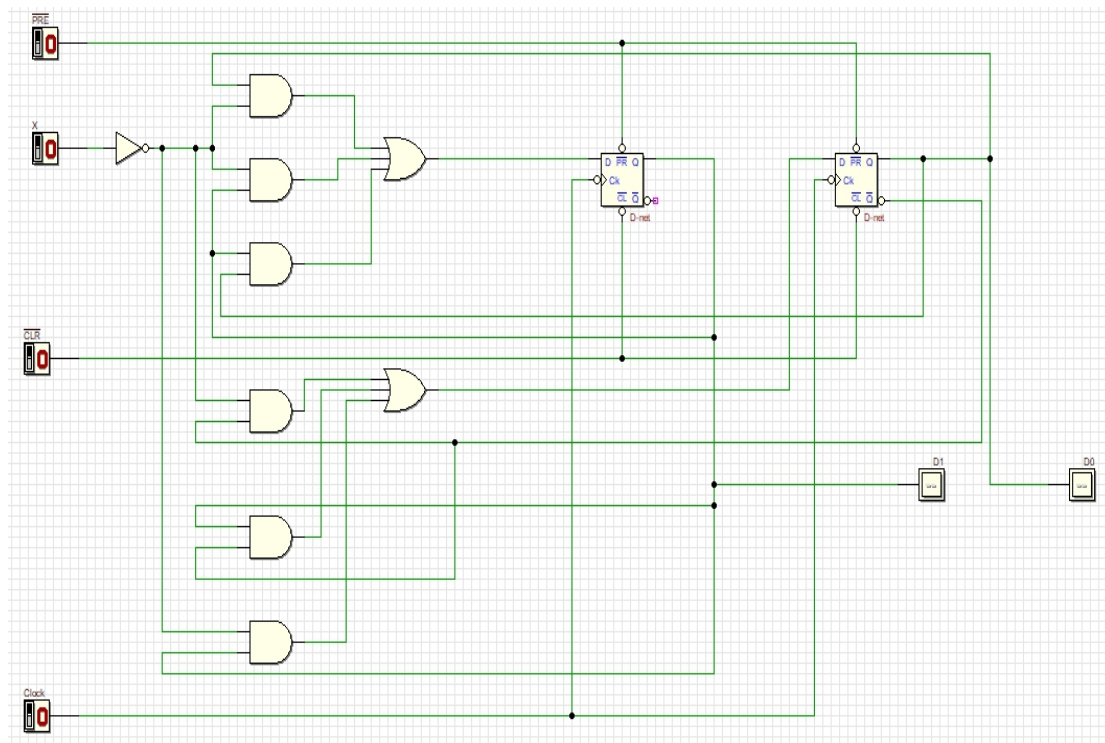
$$000,010 = X'Q0'$$

$$011,010 = X'Q1$$

$$010,110 = Q1Q0'$$

$$D0 = X'Q0' + X'Q1 + Q1Q0'$$

c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 3 is correct.

Table 4

| Input<br>X | Present State |    | Next State |     | D FF Transition |    |
|------------|---------------|----|------------|-----|-----------------|----|
|            | Q1            | Q0 | Q1+        | Q0+ | D1              | D0 |
| 0          | 0             | 0  | 0          | 1   | 0               | 1  |
| 0          | 0             | 1  | 1          | 0   | 1               | 0  |
| 0          | 1             | 0  | 1          | 1   | 1               | 1  |
| 0          | 1             | 1  | 1          | 1   | 1               | 1  |
| 1          | 0             | 0  | 0          | 0   | 0               | 0  |
| 1          | 0             | 1  | 0          | 0   | 0               | 0  |
| 1          | 1             | 0  | 0          | 1   | 0               | 1  |
| 1          | 1             | 1  | 1          | 0   | 1               | 0  |

Table 4 shows the result from the stimulation of circuit. Table 4 is same with table 3.

Thus, table 3 is correct.

7) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Build the next state and transition table using the header in Table 3

| Input | Present State |    | Next State |     | T FF Transition |    |
|-------|---------------|----|------------|-----|-----------------|----|
| X     | Q1            | Q0 | Q1+        | Q0+ | T1              | T0 |
| 0     | 0             | 0  | 0          | 1   | 0               | 1  |
| 0     | 0             | 1  | 1          | 0   | 1               | 1  |
| 0     | 1             | 0  | 1          | 1   | 0               | 1  |
| 0     | 1             | 1  | 1          | 1   | 0               | 0  |
| 1     | 0             | 0  | 0          | 0   | 0               | 0  |
| 1     | 0             | 1  | 0          | 0   | 0               | 1  |
| 1     | 1             | 0  | 0          | 1   | 1               | 1  |
| 1     | 1             | 1  | 1          | 0   | 0               | 1  |

b) Get the optimized Boolean expression.

|   |   |      |    |    |    |
|---|---|------|----|----|----|
|   |   | Q1Q0 |    |    |    |
|   |   | 00   | 01 | 11 | 10 |
| X | 0 |      | 1  |    |    |
|   | 1 |      |    |    | 1  |

$$001 = X'Q1'Q0$$

$$110 = XQ1Q0'$$

$$T1 = X'Q1'Q0 + XQ1Q0'$$

|   |   |      |    |    |    |
|---|---|------|----|----|----|
|   |   | Q1Q0 |    |    |    |
|   |   | 00   | 01 | 11 | 10 |
| X | 0 | 1    | 1  |    | 1  |
|   | 1 |      | 1  | 1  | 1  |

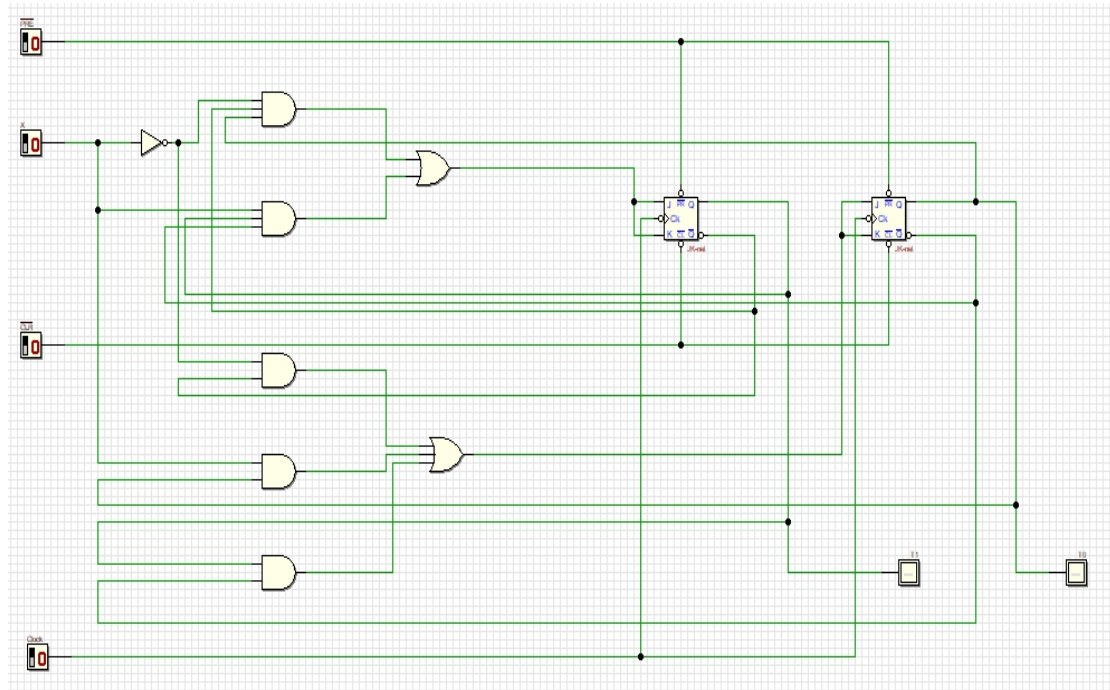
$$000,001 = X'Q1'$$

$$101,111 = XQ0$$

$$010,110 = Q1Q0'$$

$$T0 = X'Q1' + XQ0 + Q1Q0'$$

c) Draw the complete final circuit design in Deeds.



e) Simulate the circuit to prove that your Table 3 is correct.

Table 5

| Input | Present State |    | Next State |     | T FF Transition |    |
|-------|---------------|----|------------|-----|-----------------|----|
| X     | Q1            | Q0 | Q1+        | Q0+ | T1              | T0 |
| 0     | 0             | 0  | 0          | 1   | 0               | 1  |
| 0     | 0             | 1  | 1          | 0   | 1               | 1  |
| 0     | 1             | 0  | 1          | 1   | 0               | 1  |
| 0     | 1             | 1  | 1          | 1   | 0               | 0  |
| 1     | 0             | 0  | 0          | 0   | 0               | 0  |
| 1     | 0             | 1  | 0          | 0   | 0               | 1  |
| 1     | 1             | 0  | 0          | 1   | 1               | 1  |
| 1     | 1             | 1  | 1          | 0   | 0               | 1  |

Table 5 shows the result from stimulation of circuit. Table 5 is same with table 3.

Thus, table 3 is correct.