UTM

UNIVERSITI TEKNOLOGI MALAYSIA

Semester 2020/2021

Subject : Digital logic

Section : 06

Task : Lab 1

Submission : 21/12/2020

Group member

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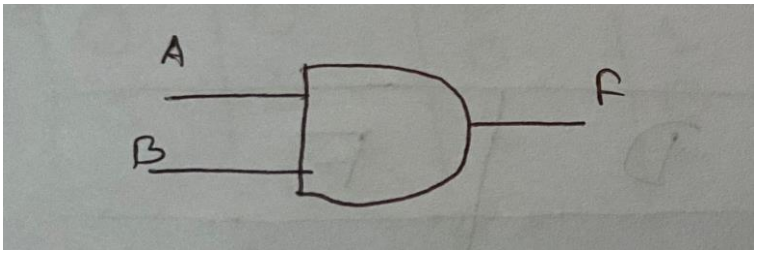
Lecturer: Dr. Yousuf

Preiminary work

1) AND

Symbol:



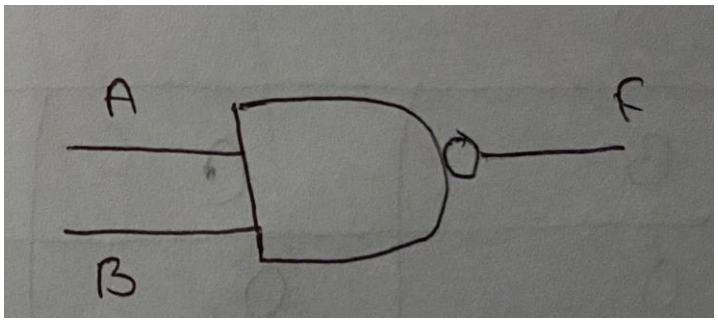
IC Number:7408

Truth table 1

Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

NAND

Symbol:



IC Number:7400

Truth table 2

Input		Output
A	B	F
0	0	1
0	1	1
1	0	1
0	0	0

2)

Truth table 3

A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

3) C= A.B'

D=A'.B

F= A.B'+ A'.B

4)

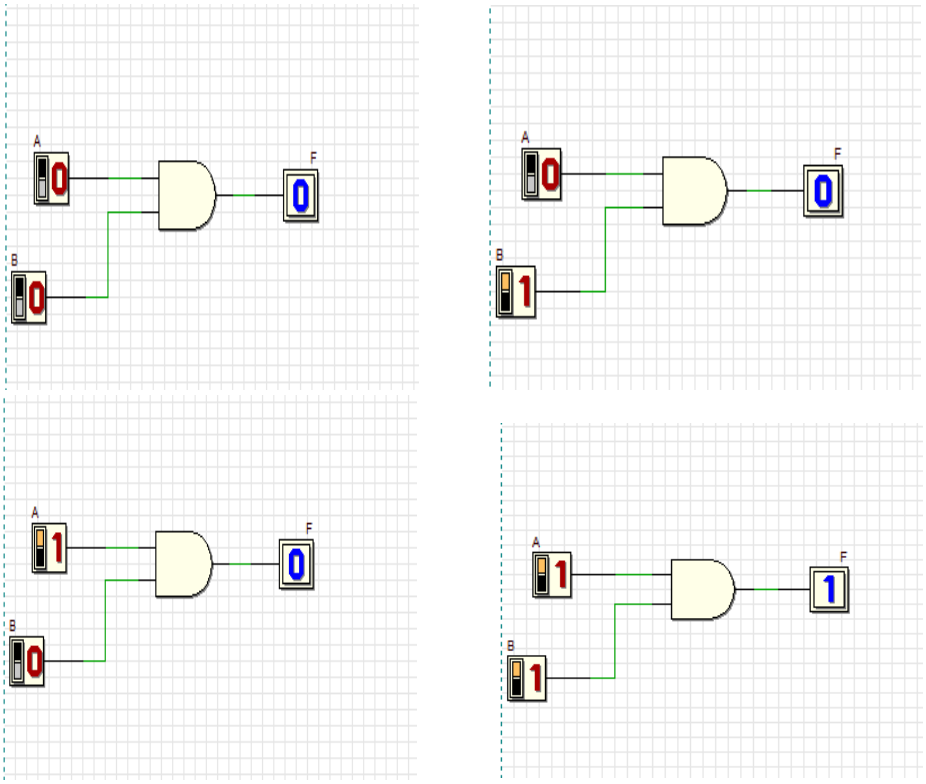
Truth table 4

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

Laboratory Work

Part 1

1)



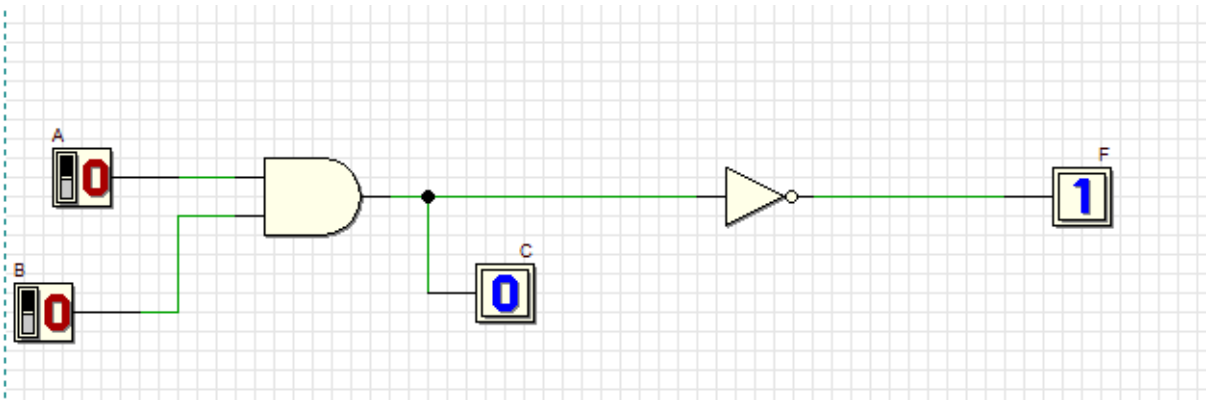
2)

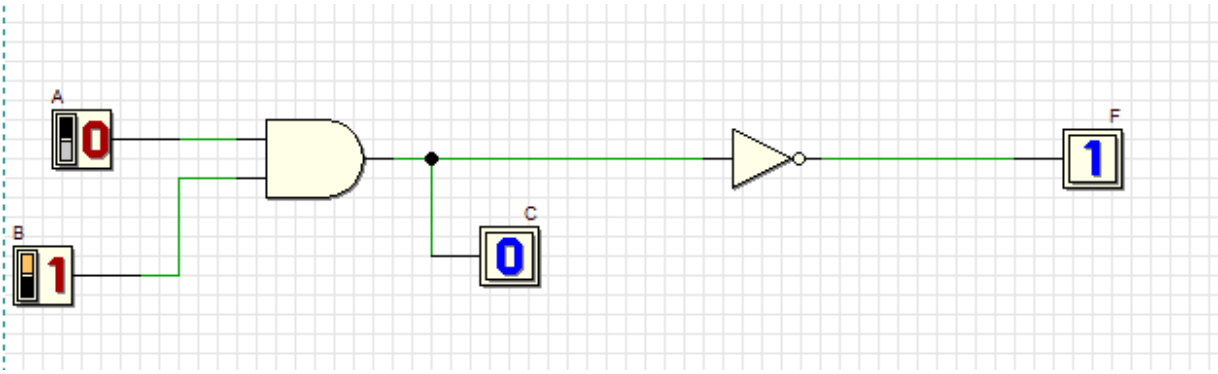
Truth table 5

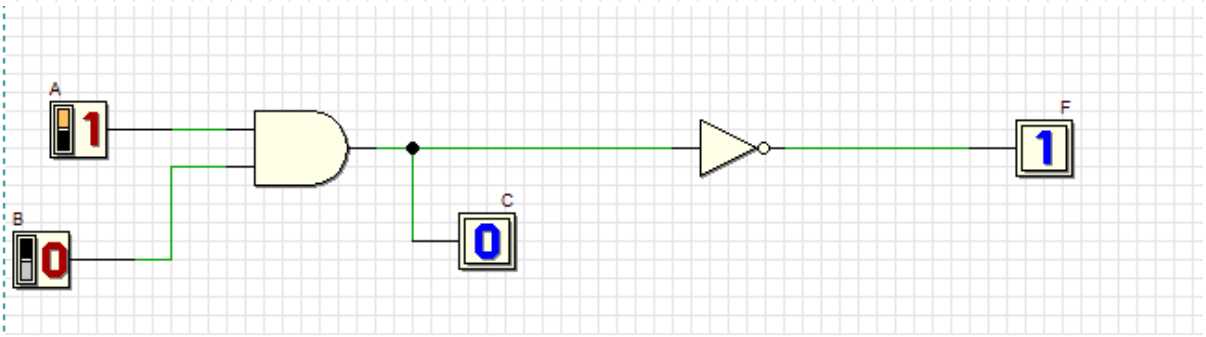
Input		Output
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

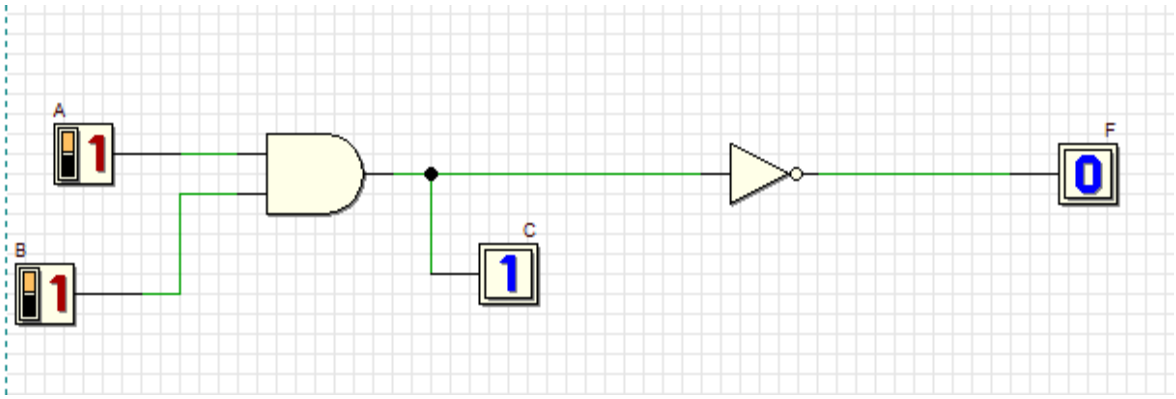
Part 2

3)









4)

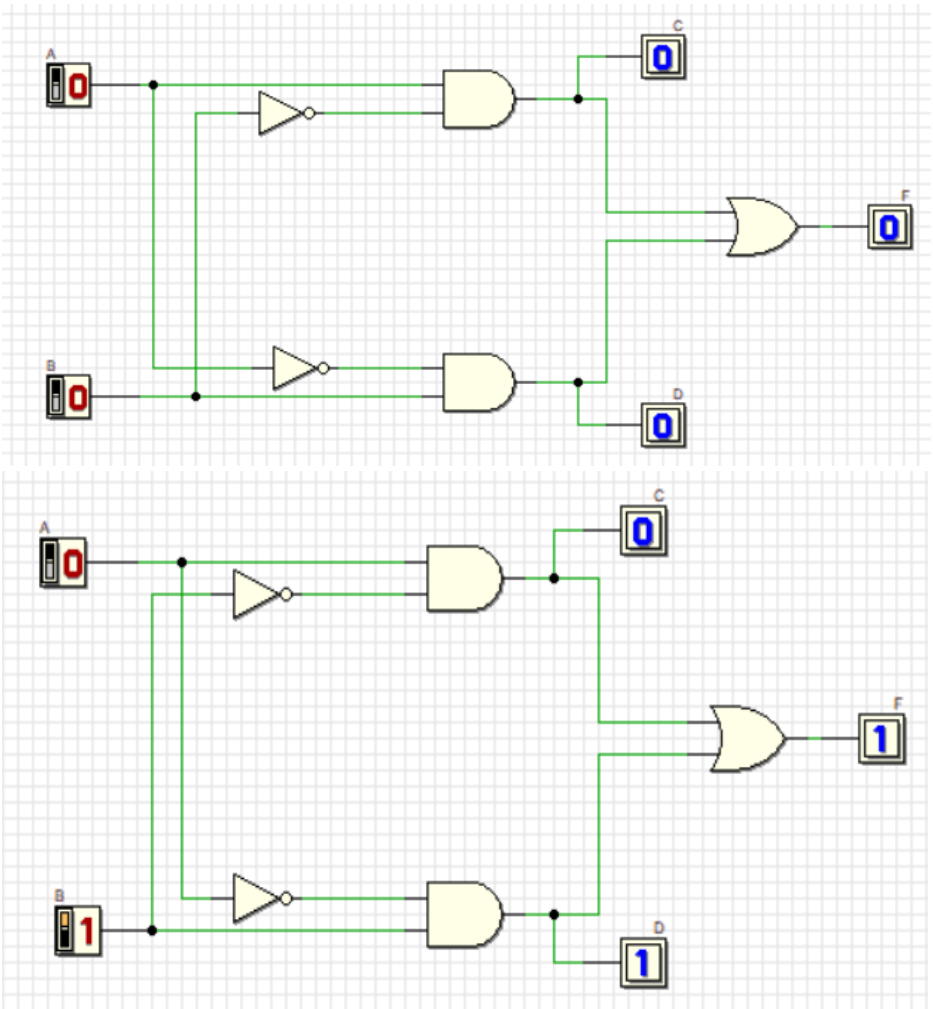
Truth table 6

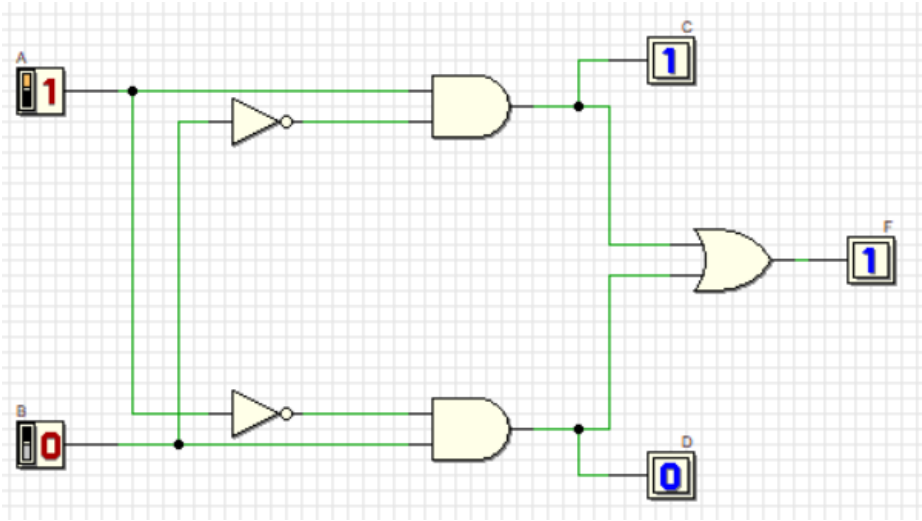
A	B	C	F
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

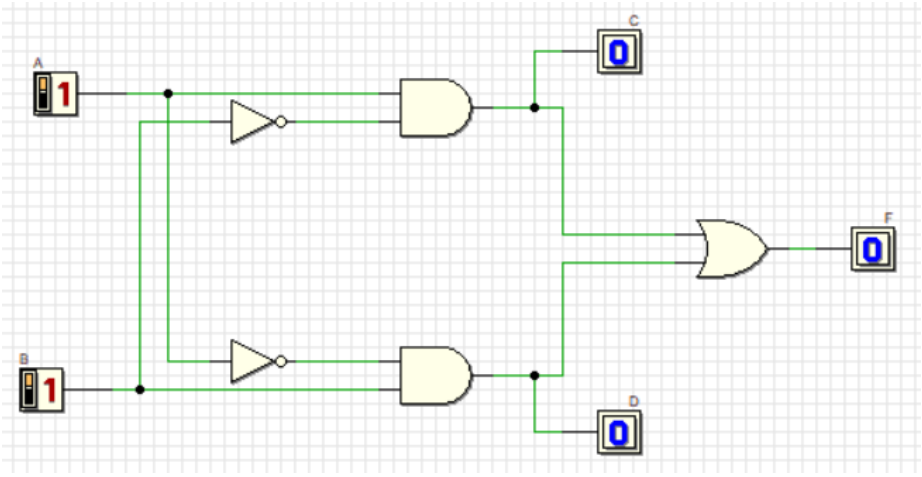
5) They have the same output

Part 3

6)







7)

Truth table 7

A	B	C	D	F
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

8) Inventor gate: negotiation of input.
AND gate: output is high when both inputs are high.
OR gate: output is false when both inputs are false.