Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT : SCSR1013 DIGITAL LOGIC

SESSION/SEM : 2020-21-01
SECTION : 06

LAB 2 : COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION

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D. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

$$Y=AB\,(C+\overline{C})+BC\,(A+\overline{A})+AC\,(B+\overline{B})$$

$$=ABC+AB\overline{C}+ABC+\overline{A}BC+ABC+A\overline{B}C$$
$$=ABC+AB\overline{C}+\overline{A}BC+A\overline{B}C$$

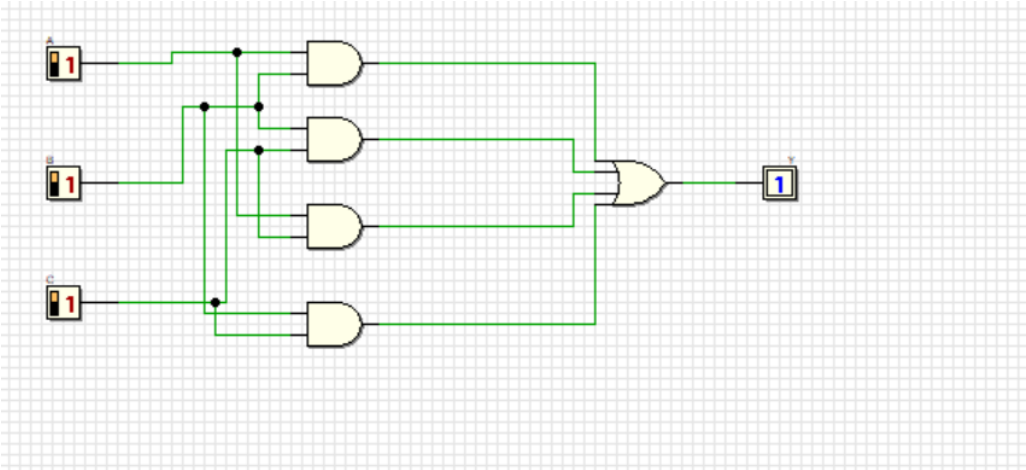
2. Based on standard form expression, complete the following truth table.

INPUT			**OUTPUT**
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3.

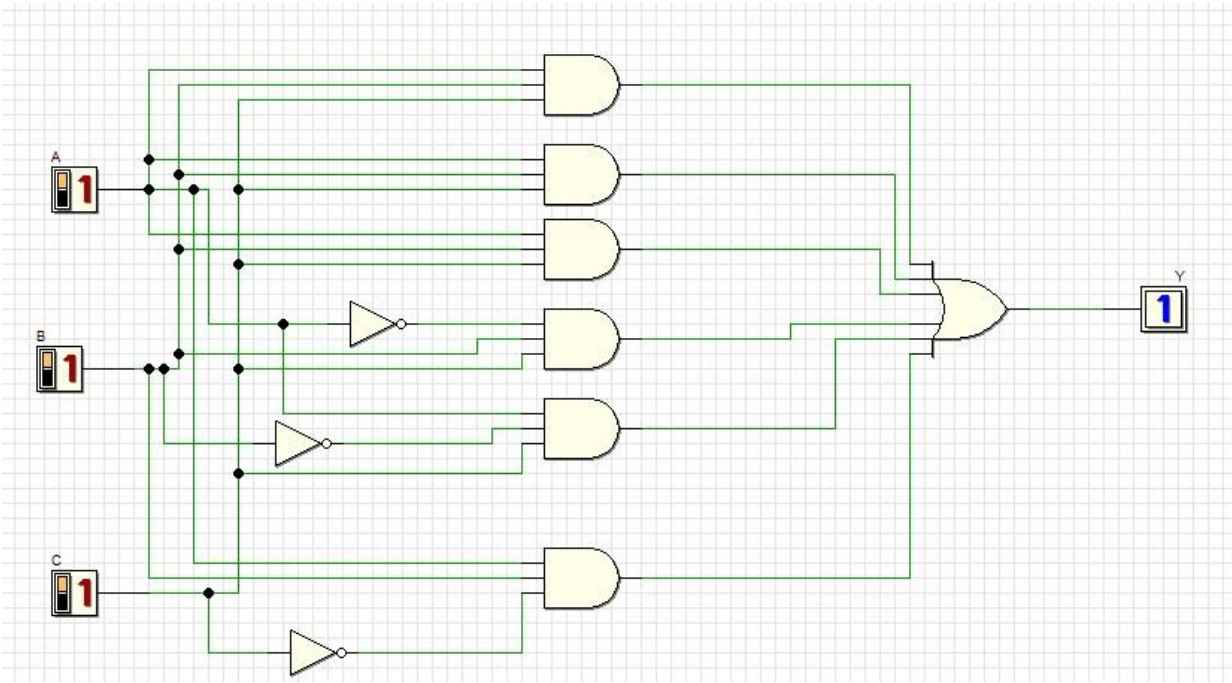
Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

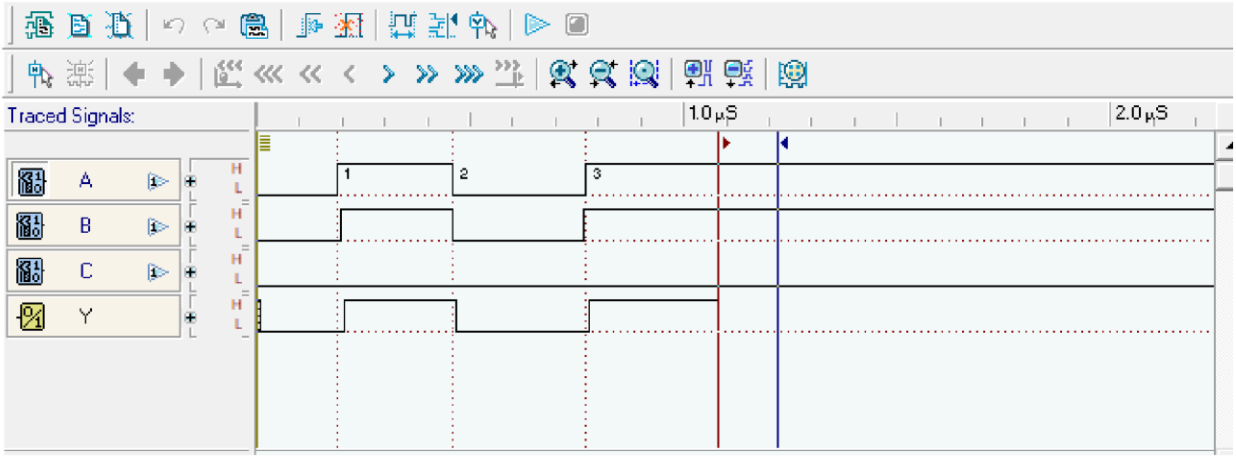
Circuit (ii)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

Truth table for both are same, so they are the same equation. Just that non-standard form is a simplified version of standard form.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



PART-02

Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 1

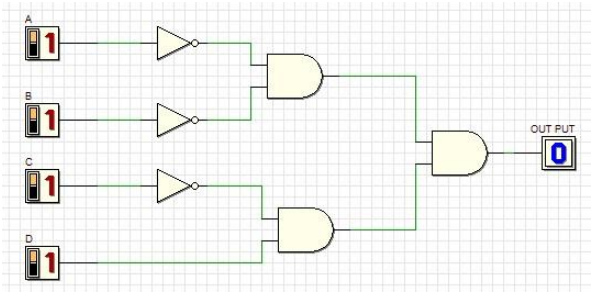
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	invalid	invalid	invalid	Invalid
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	invalid	invalid	invalid	Invalid

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.

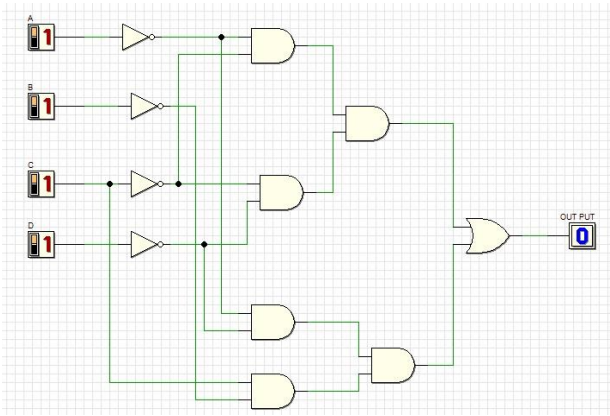
E1= $\overline{A}\ \overline{B}\ \overline{C}\ D$
E2= $A\overline{B}\ \overline{C}\ \overline{D} + \overline{A}\ \overline{B}\ C\overline{D}$
E3= $ABCD + A\overline{B}\ CD$
E4= $ABC\overline{D}$

3.From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.

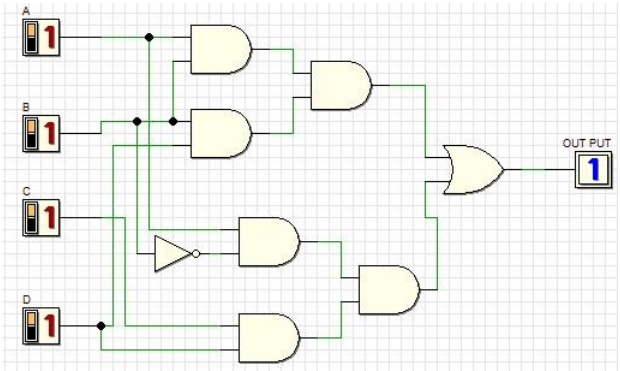
E1:



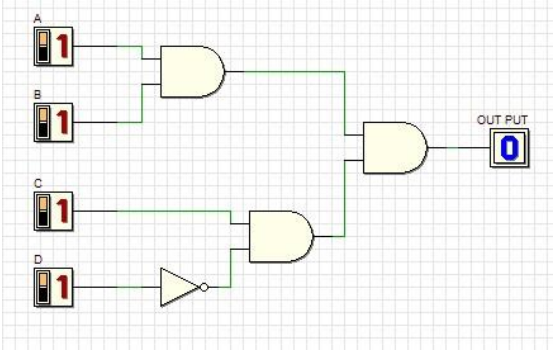
E2:



E3:



E4:



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

Truth Table 2

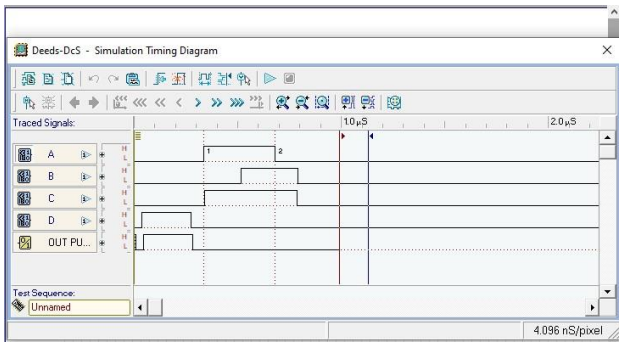
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	invalid	invalid	invalid	Invalid
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	invalid	invalid	invalid	Invalid

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

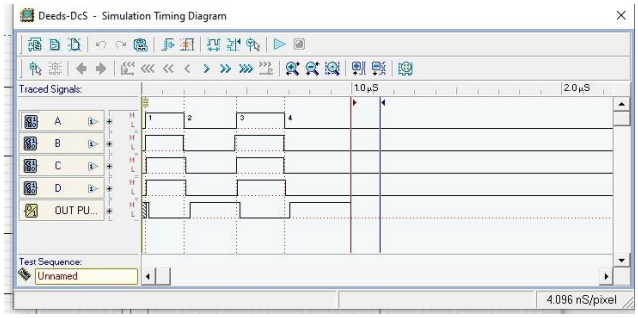
There, we can see that the outputs in the both of the tables are the same have same outputs.

b) Timing Diagram:

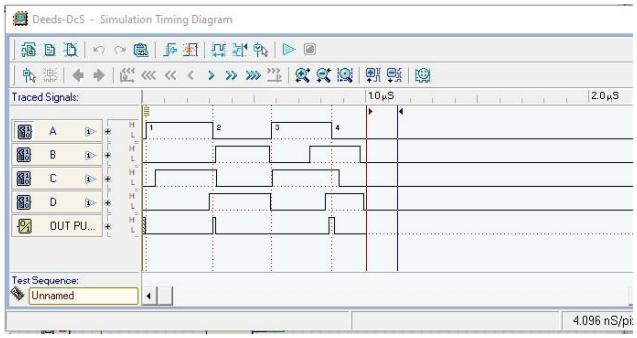
E1:



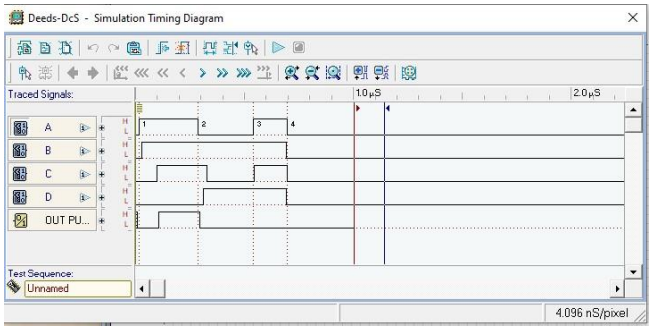
E2:



E3:



E4:

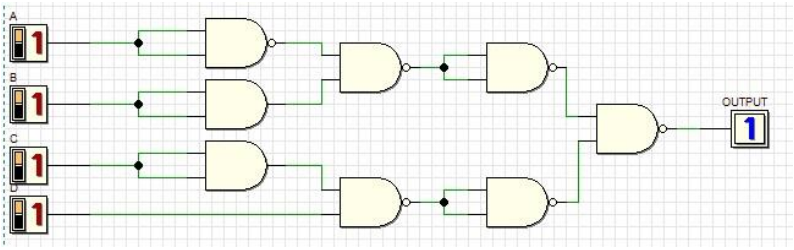


Explain some analysis values based on your timing diagram:

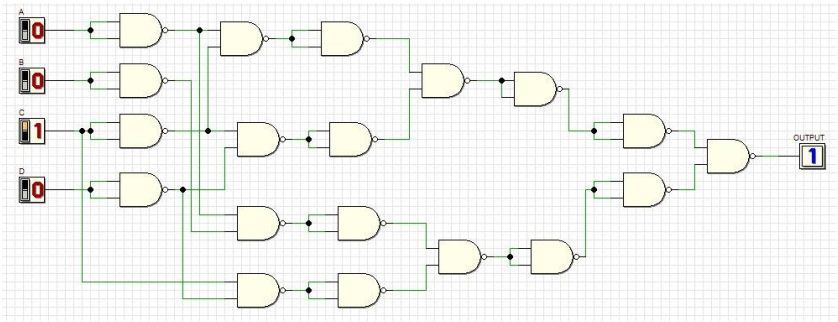
In E1: only input D value is come out as an output; for E2: if all input is low. Then output will be high. And for E3: if all input is high then output will be high. And lastly For E4: if the input for A, B, C is high and D is low then the output will be High.

5.Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.

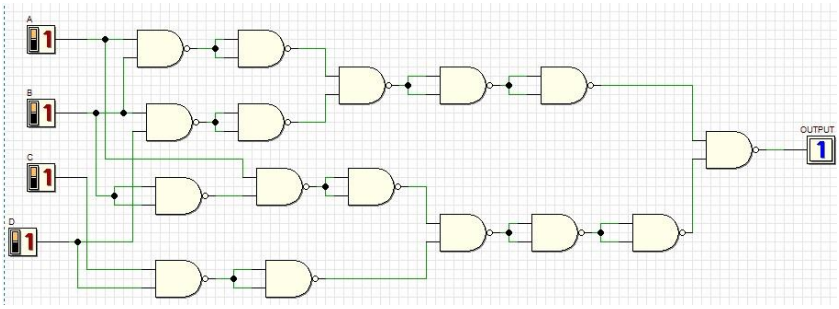
E1:



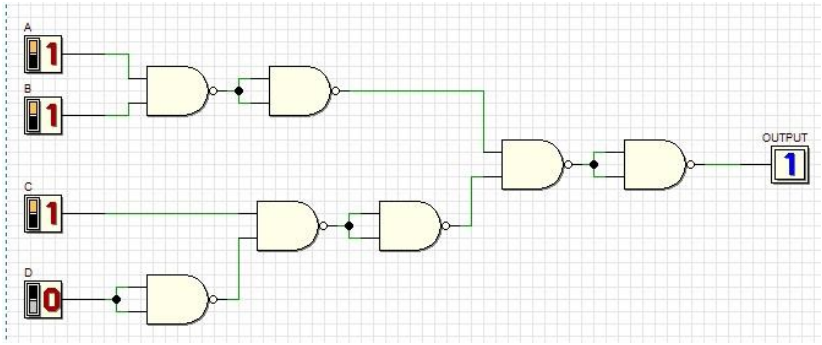
E2:



E3:



E4:



6.Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

Truth Table 3

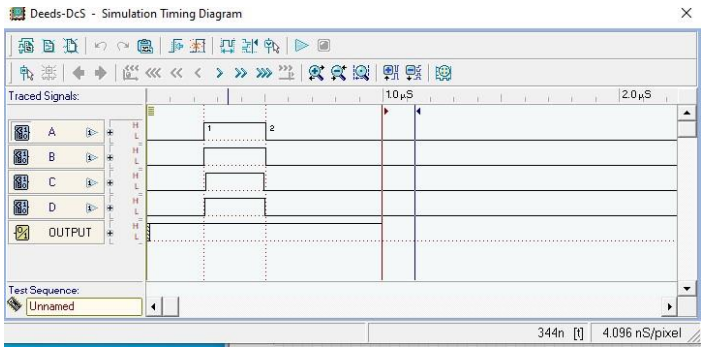
INPUTS				**OUTPUTS**			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	invalid	invalid	invalid	Invalid
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	invalid	invalid	invalid	Invalid

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

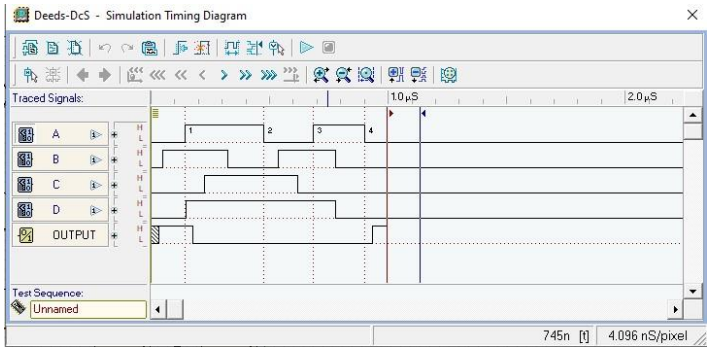
There we can see that both of truth table has the same out. Same output because NAND gates are universal gates.

b) Timing Diagram

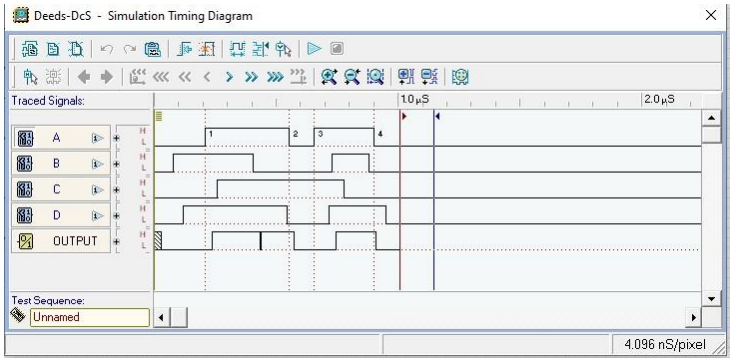
E1:



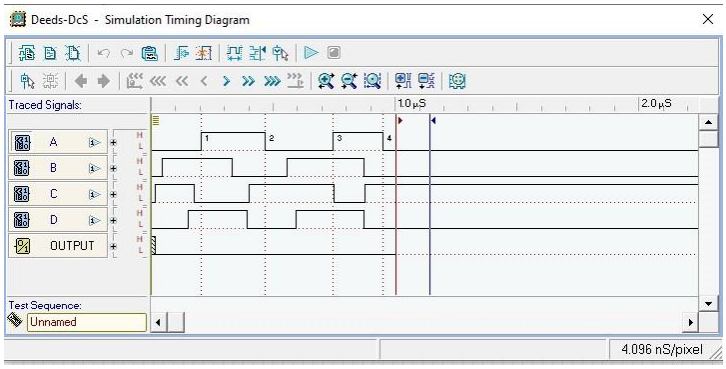
E2:



E3:



E4:



Explain some analysis values based on your timing diagram:

The timing diagram shows that when most of the input is low, output of E1 and E2 are low