



UTM
UNIVERSITI TEKNOLOGI MALAYSIA

SCHOOL OF COMPUTING
SESSION 2020/2021 SEMESTER 1

SECR1013
Section 08

Digital Logic
Lab 3

2021

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SUBMISSION DATE: 25th January 2021



**School of Computing
Faculty of Engineering
UNIVERSITI TEKNOLOGI MALAYSIA**

SUBJECT : SECR1013 DIGITAL LOGIC

SESSION/SEM : Session 2020/2021 Semester 1

LAB 3 : SYNCHRONOUS DIGITAL COUNTER

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DATE : 25 January 2021

Lab #3

Identifying the Properties of a Synchronous Counter

A. Aims

- 1) Expose the student with experience on constructing synchronous counter circuit using Flip-Flop IC, Basic Gate ICs, Breadboard and ETS-5000 Digital Kit.
- 2) Promote critical thinking among students by analysing the given circuit and identifying the behaviour of the digital circuit.

B. Objectives

The objectives of this lab activity are to:

- 1) Implement a synchronous counter circuit into physical circuit using Breadboard, Flip-Flops, Basic Gates and Switches.
- 2) Completing the next-state table of the counter circuit.
- 3) Sketch the state diagram of the counter circuit.
- 4) Identify the properties of the counter.

C. Materials And Equipment

Materials and equipment required for this lab are as follows:

Item Name	Number of Item
1. Breadboard	1
2. 7408 Quad 2-Input AND	1
3. 7404 Hex Inverter	1
4. 7432 Quad 2-input OR	1
5. 7476 Dual J-K Flip Flop	1
6. ETS-5000 Digital Kit	1

D. Preliminary Works

- 1) Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	$\overline{PRE}$	$\overline{CLR}$	J	K	CLK	Q
Set initial value Q = 1	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	↓	1
Output Q become 0, no change in asynchronous input	1	1	1	1	↓	0
Output Q is not the previous Q	1	1	1	1	↓	1
RESET Q	1	1	0	1	↓	0
SET Q	1	1	1	0	↓	1

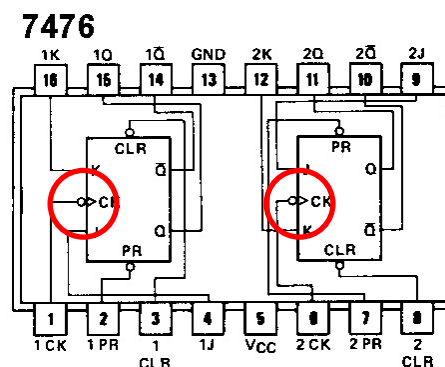
- 2) Answer all questions.

- a) Which state that JK flip-flop has, but not on SR flip-flop.

Toggle state, when J = 1 and K = 1

- b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

According to the pin layout diagram as shown to the right, 7476 Dual J-K Flip-Flop IC is negative-edge triggered flip flop



E. Lab Activities

- 1) You are given a counter circuit as shown in Figure 4.

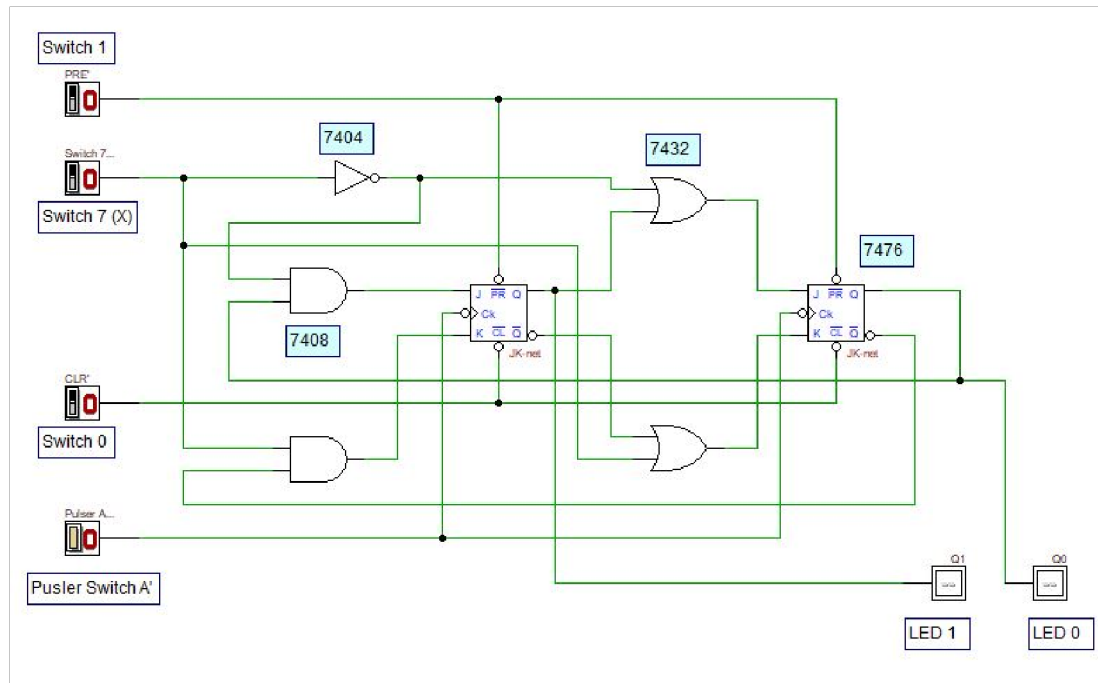
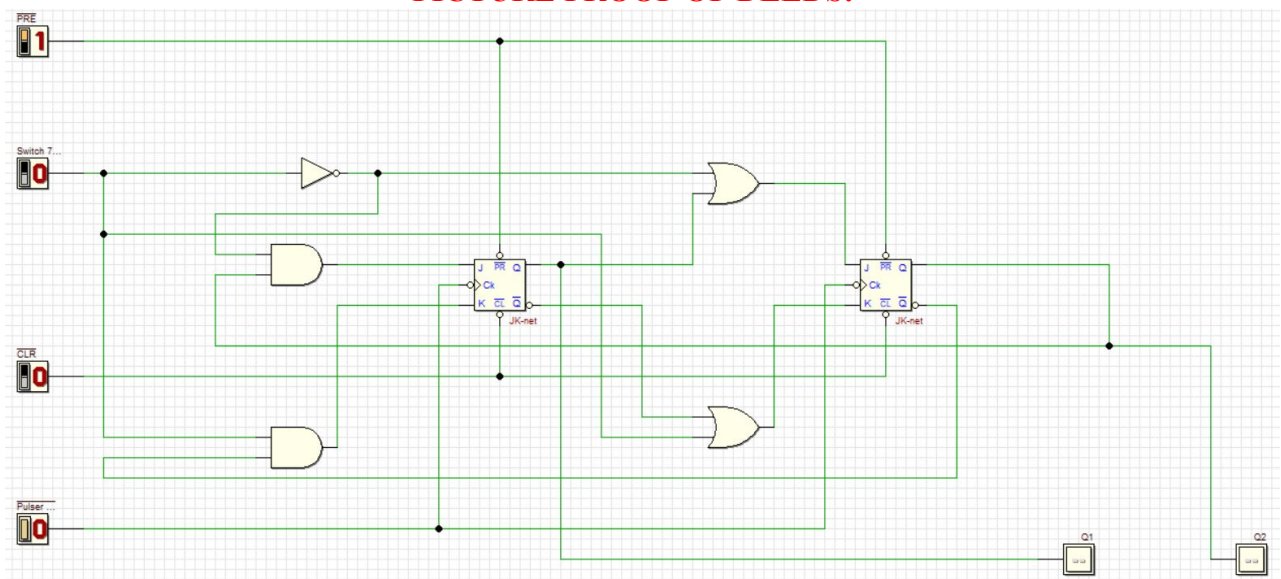


Figure 4: A Synchronous Counter Circuit

- 2) By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to Vcc and GND).

PICTURE PROOF OF DEEDS:

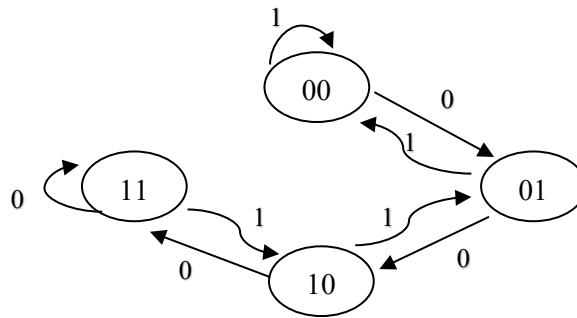


- 3) Investigate the behaviour of the counter by observing the next state of the counter for all combination of *Present State* and *X* values. Complete the *NextState* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state.
(0=LOW, 1=HIGH)

Table 2

Switch 7	Present State		Next State	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?

Pulser switch A (Clock) which is connected to both clock JK flip-flop.

b) How many states are available for the counter and what are they?

4 states which are 00,01,10,11

c) What is the function of Switch 7 (X) in the circuit?

As a controller to change the mode of counter to either count-up or count-down

d) What is the function of Switch 0 and Switch 1 in the circuit?

Switch 0 as clear, switch 1 as preset. Both are for asynchronous input for Flip flops

e) Is the counter a saturated counter or recycle counter?

Saturated counter. Once the highest or lowest value is reached the counter won't cycle back

6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

a) Built the next state and transition table using the header in Table 3

Table 3

Input X	Present State		Next State		D FF Transition	
	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

b) Get the optimized Boolean expression.

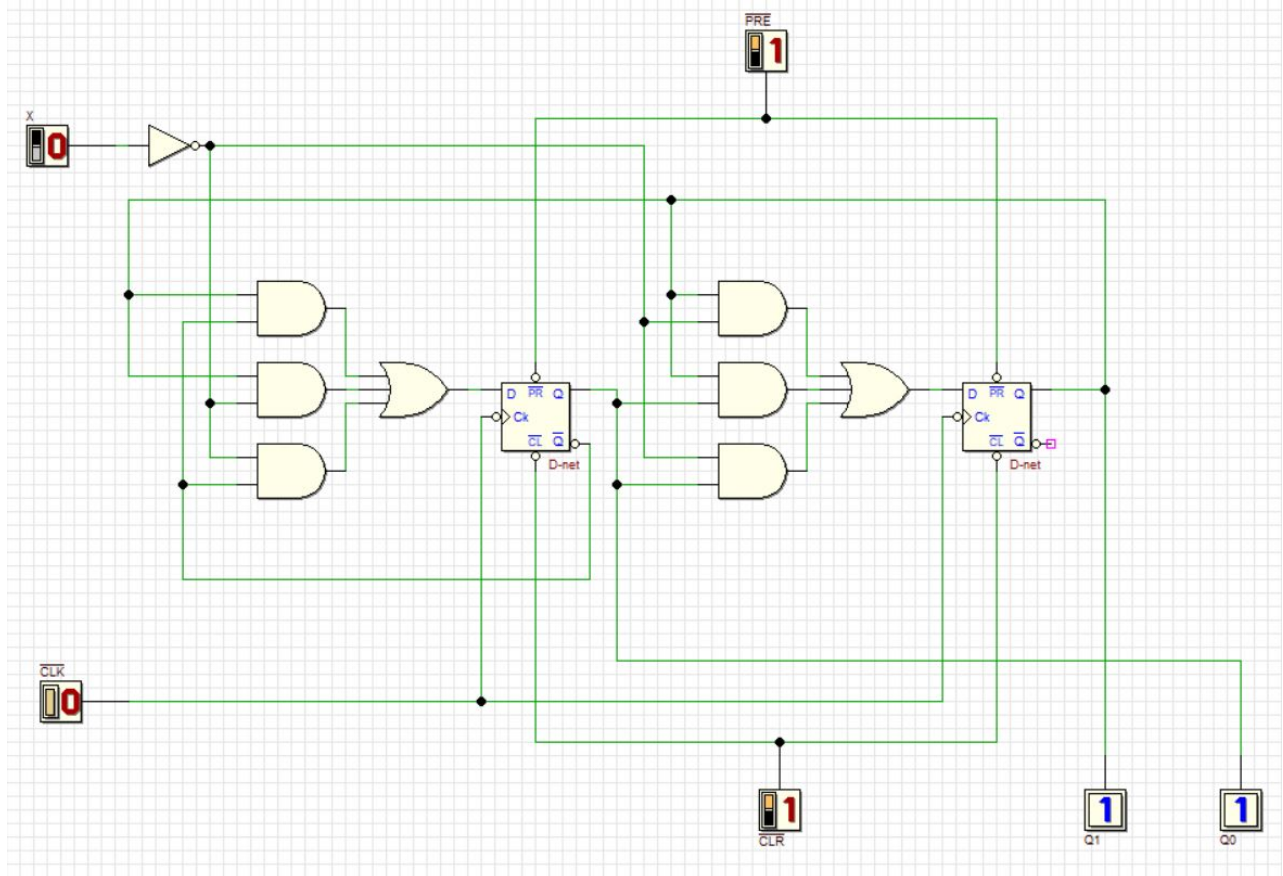
X \ Q1Q0	00	01	11	10
0	0	1	1	1
1	0	0	1	0

$$D_1 = X'Q_0 + X'Q_1 + Q_1Q_0$$

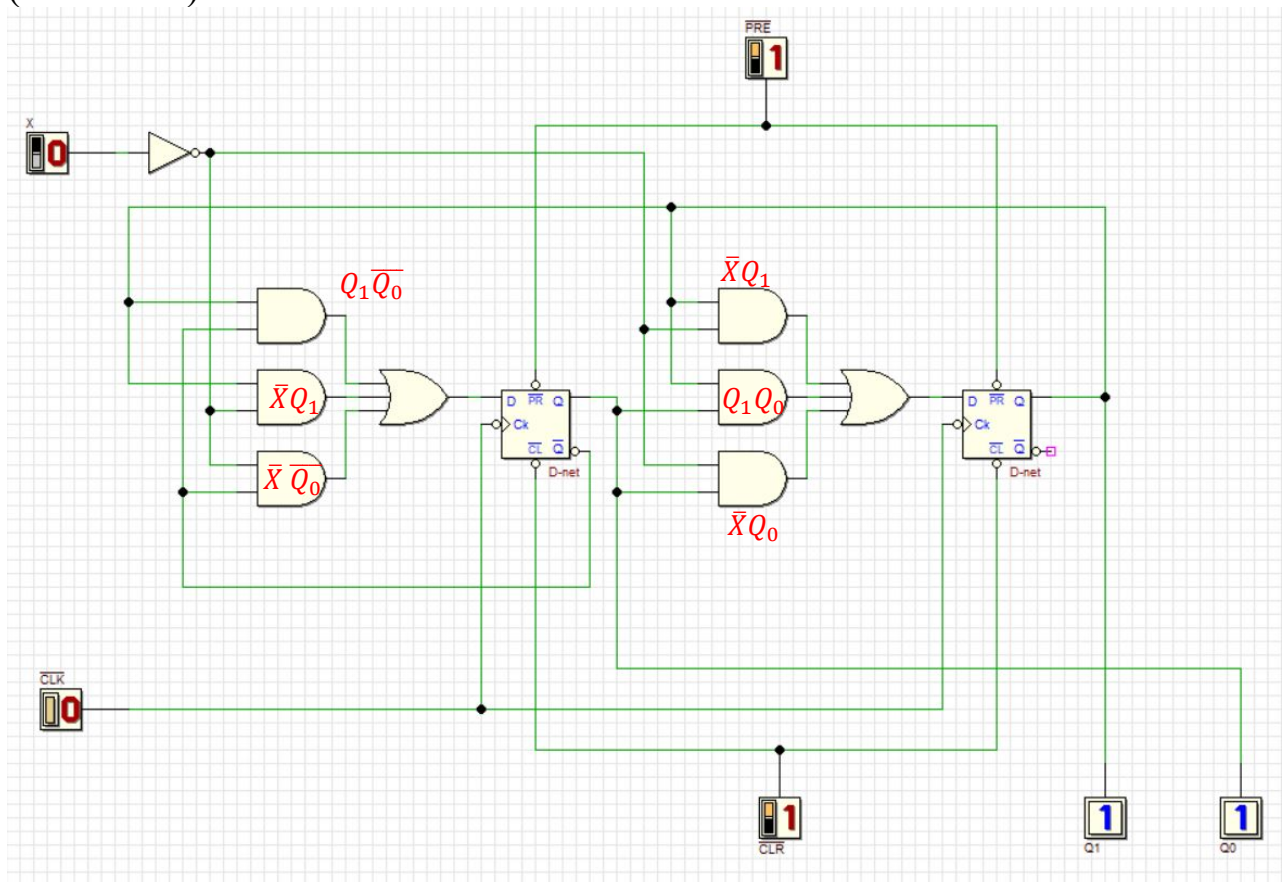
X \ Q1Q0	00	01	11	10
0	1	0	1	1
1	0	0	0	1

$$D_0 = X'Q_0' + X'Q_1 + Q_1Q_0'$$

c) Draw the complete final circuit design in Deeds.

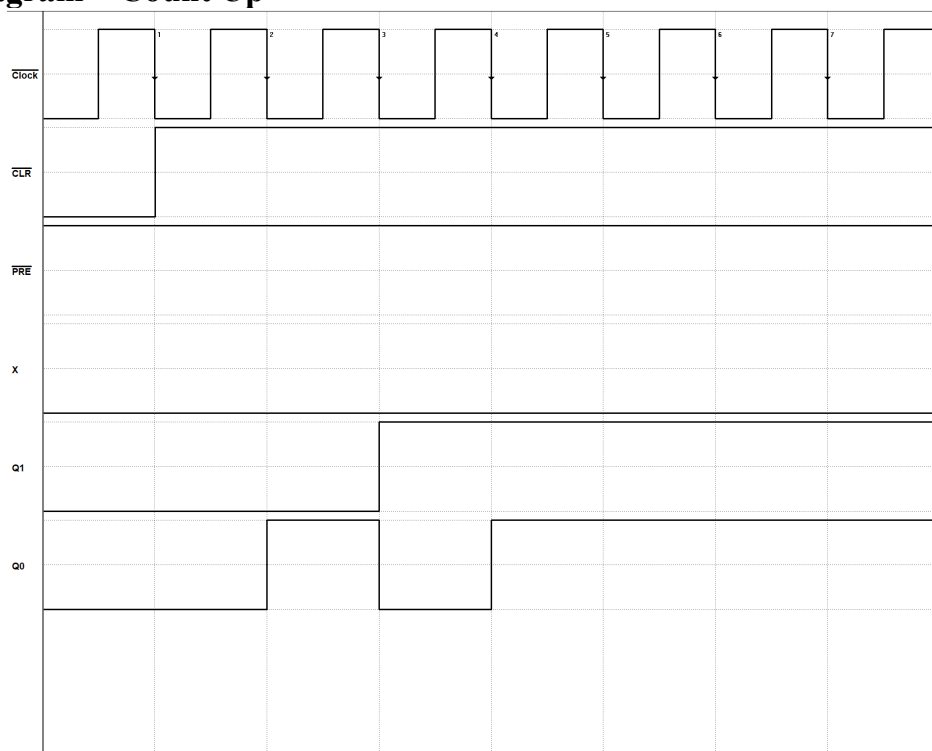


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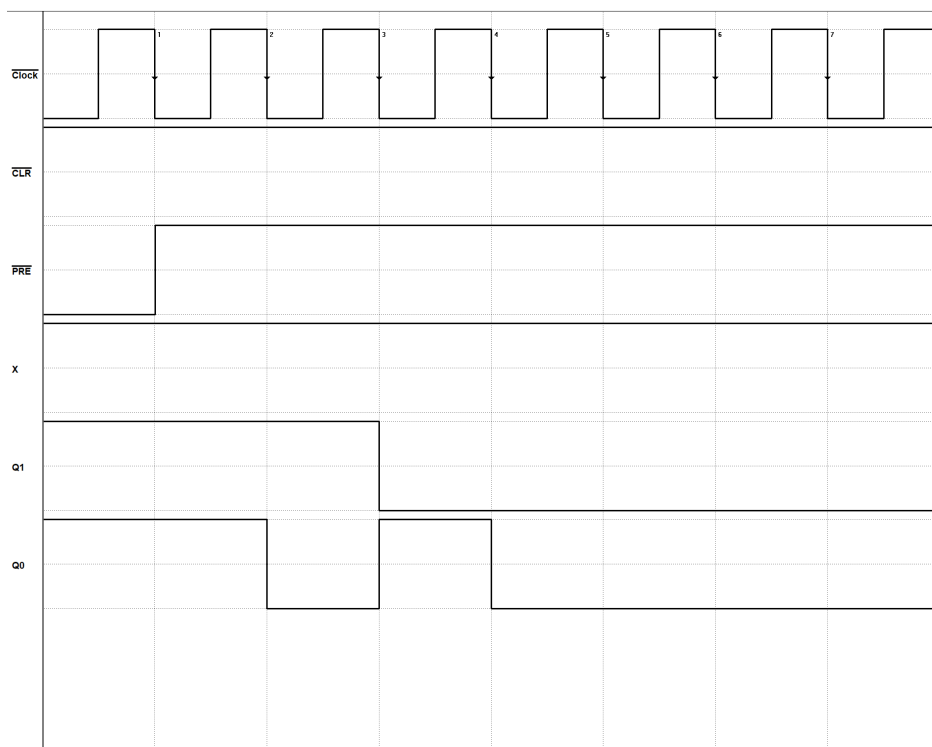


- d) Simulate the circuit to prove that your Table 3 is correct.

Timing Diagram – Count Up



Timing Diagram – Count Down



7) Repeat steps in Q(6) using T flip-flop.

a) Built the next state and transition table using the header in Table 3

Table 3

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

b) Get the optimized Boolean expression.

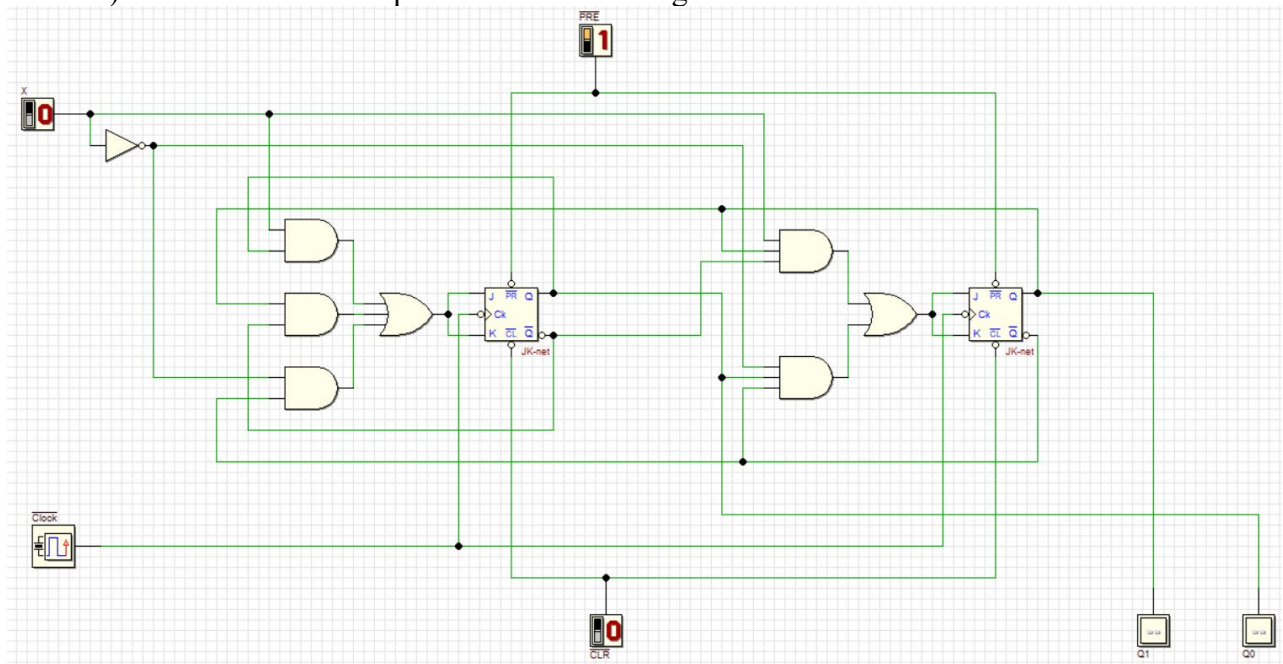
x \ Q1Q0	00	01	11	10
0	0	1	0	0
1	0	0	0	1

$$T_1 = X'Q_1'Q_0 + XQ_1Q_0'$$

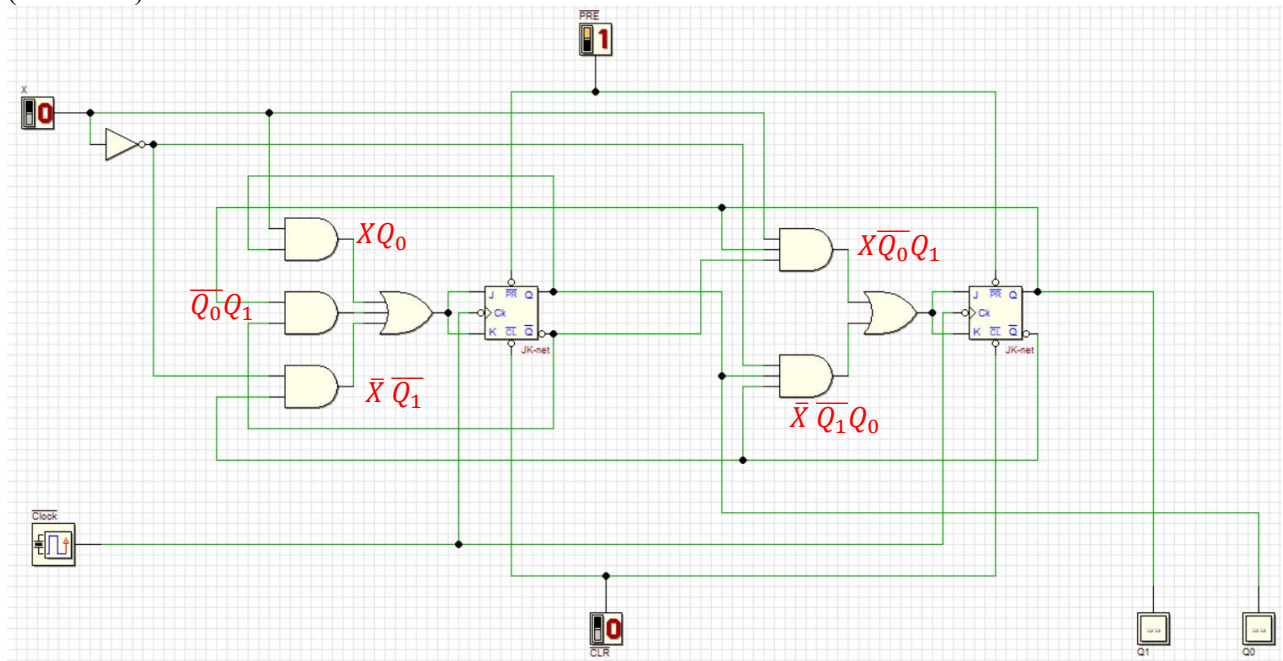
x \ Q1Q0	00	01	11	10
0	1	1	0	1
1	0	1	1	1

$$T_0 = X'Q_1' + XQ_0 + Q_1Q_0'$$

c) Draw the complete final circuit design in Deeds.

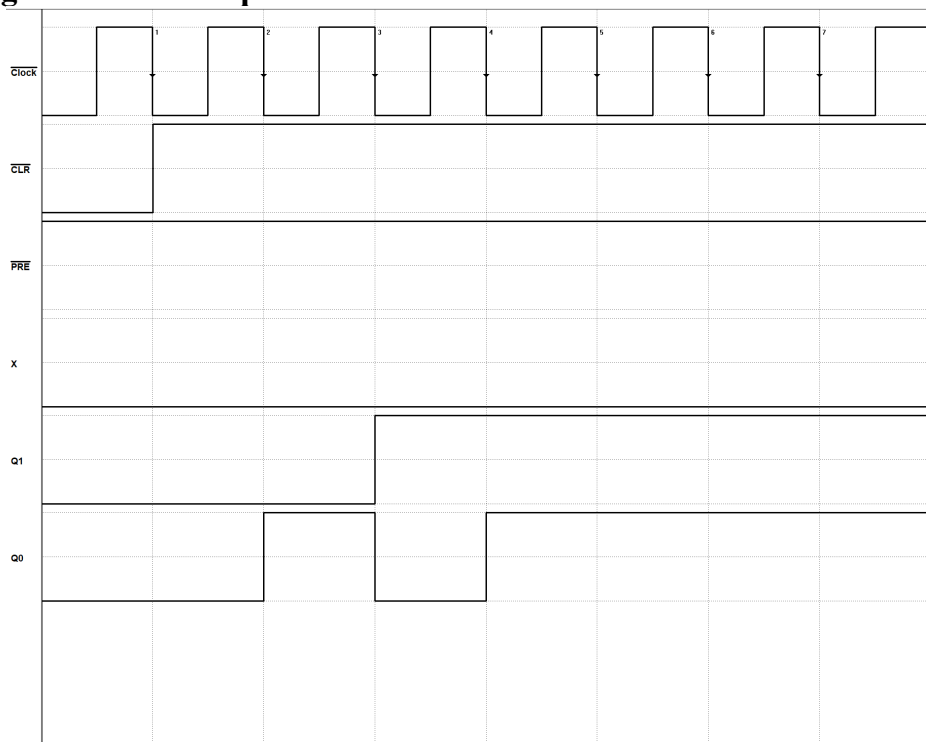


(Labeled)



- d) Simulate the circuit to prove that your Table 3 is correct.

Timing Diagram – Count Up



Timing Diagram – Count Down

