



UTM
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SCHOOL OF COMPUTING
SESSION 2020/2021 SEMESTER 1

SECR1013
Section 08

Digital Logic
Lab 2

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**Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA**

SUBJECT : SECR1013 DIGITAL LOGIC

SESSION/SEM : Semester 1 2020/2021

**LAB 2 : COMBINATIONAL LOGIC CIRCUIT DESIGN
SIMULATION**

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DATE : 17 January 2021

REMARKS :

MARKS:

A. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

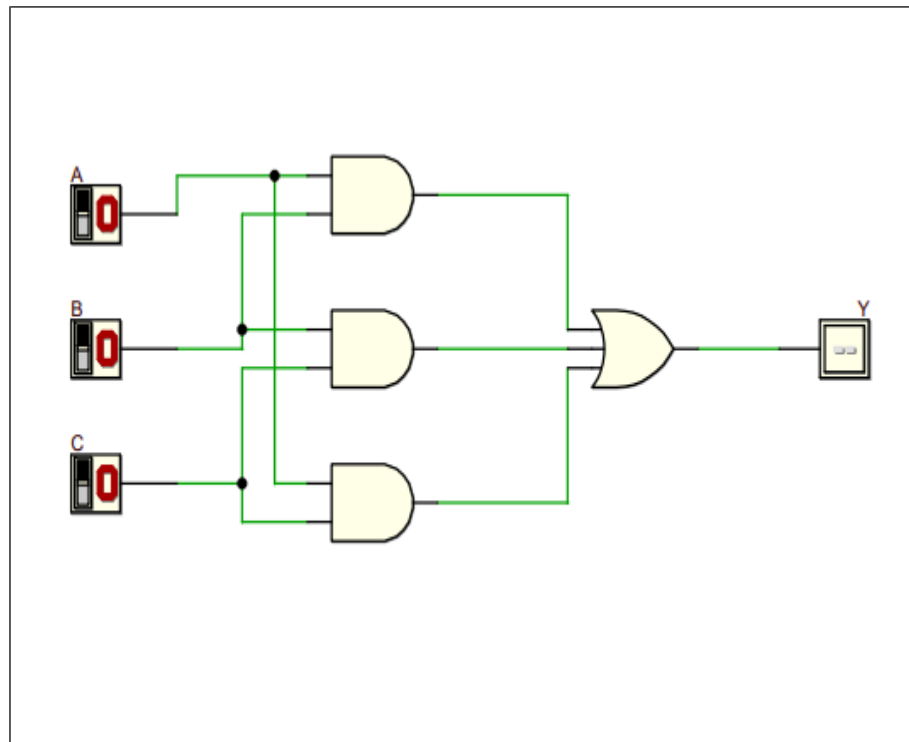
$$\begin{aligned} Y &= AB(C+C') + (A+A')BC + A(B+B')C \\ &= ABC + ABC' + ABC + A'BC + ABC + AB'C \\ &= ABC + ABC' + A'BC + AB'C \end{aligned}$$

2. Based on standard form expression, complete the following truth table.

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

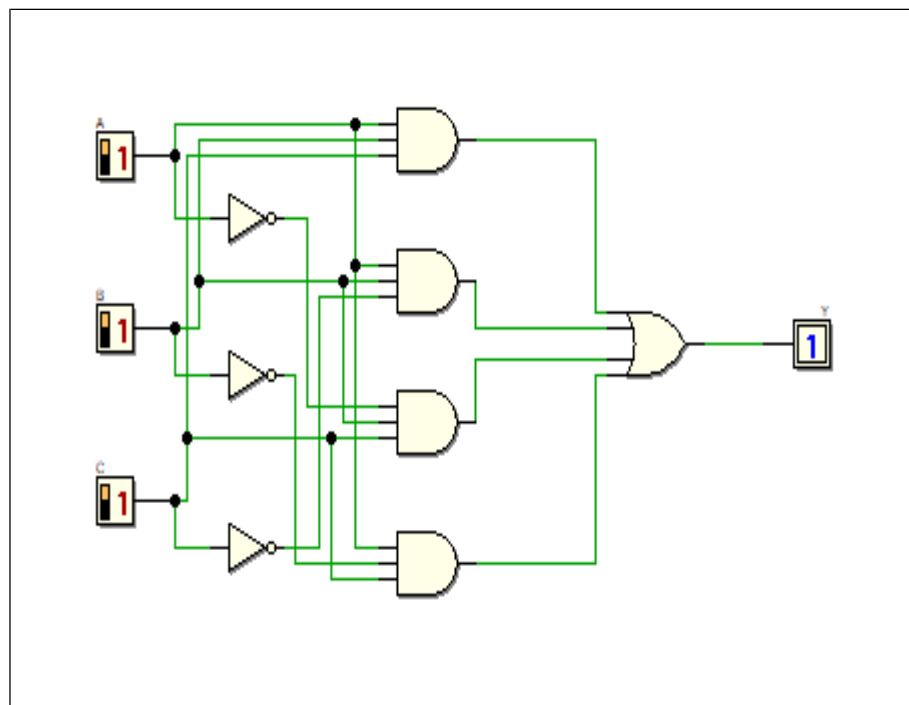
3. Using Deeds Simulator, draw the following circuits:

- a) Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

- b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Circuit (ii)

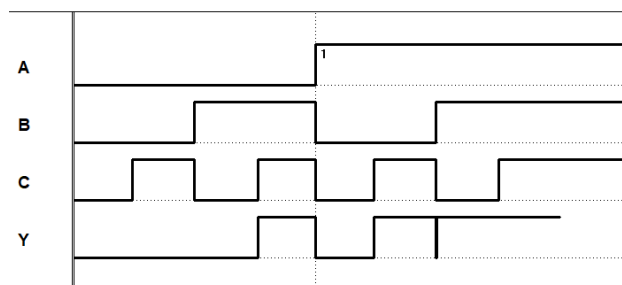
INPUT			OUTPUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

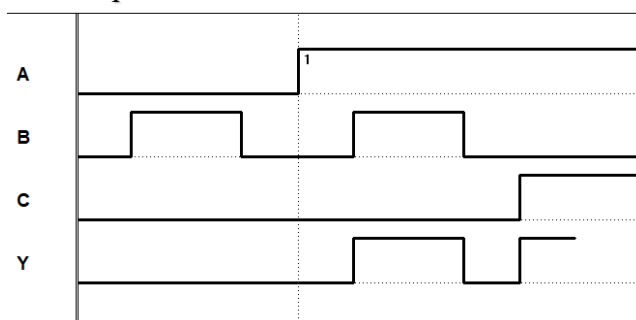
Both truth table of circuits have same result. Circuit(i) is a non-standard form while circuit (ii) is a standard form. Non-standard form and standard form of circuits both can produce same result. Thus, non-standard form circuit is the simple form of standard form circuit.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.

From truth table



Different input



Part 2

Combinational circuit design process and simulate with Deeds Simulator.

Design Process

- i) Determine Parameter Input / Output and their relations.
- ii) Construct Truth Table.
- iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.
- iv) Draw the circuit and use duality symbol; convert AND-OR circuit to NAND gates ONLY.
- v) Simulate the design using Deeds Simulator. Check the results according to Truth Table and Timing Diagram Operation.

Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.

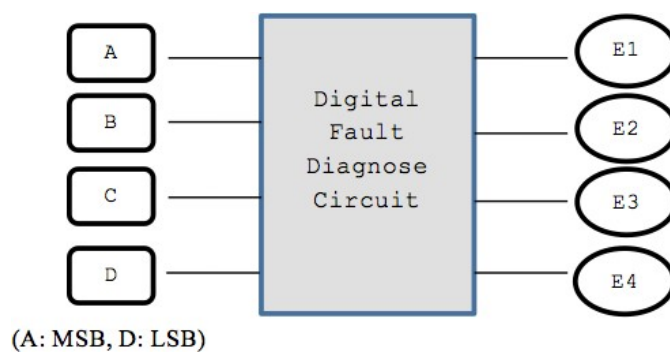


Figure 5

The following rules are used to activate the error's signal type:

- RULE 1:** E1 is activated if the input number is positive ODD and the majority of the bits is '0'.
- RULE 2:** E2 is activated if the input number is positive EVEN and the majority of the bits is '0'.
- RULE 3:** E3 is activated if the input number is negative ODD and the majority of the bits is '1'.
- RULE 4:** E4 is activated if the input number is negative EVEN and the majority of the bits is '1'.
- RULE 5:** The output of error signal is invalid if the input has equal bit '0' and bit '1'.
- (NOTE:** Positive ODD is positive numbers that are odd and negative EVEN is negative numbers that are even).

Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 1

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.

K-Map For E1

		CD			
		00	01	11	10
AB	00	0	1	X	0
	01	0	X	0	X
	11	X	0	0	0
	10	0	X	0	X

SOP Exp for E1: $\bar{A} \bar{B} D$

K-Map For E2

		CD			
		00	01	11	10
AB	00	1	0	X	1
	01	1	X	0	X
	11	X	0	0	0
	10	0	X	0	X

SOP Exp for E2: $\bar{A} \bar{D}$

K-Map For E3:

		CD			
		00	01	11	10
AB	00	0	0	X	0
	01	0	X	0	X
	11	X	1	1	0
	10	0	X	1	X

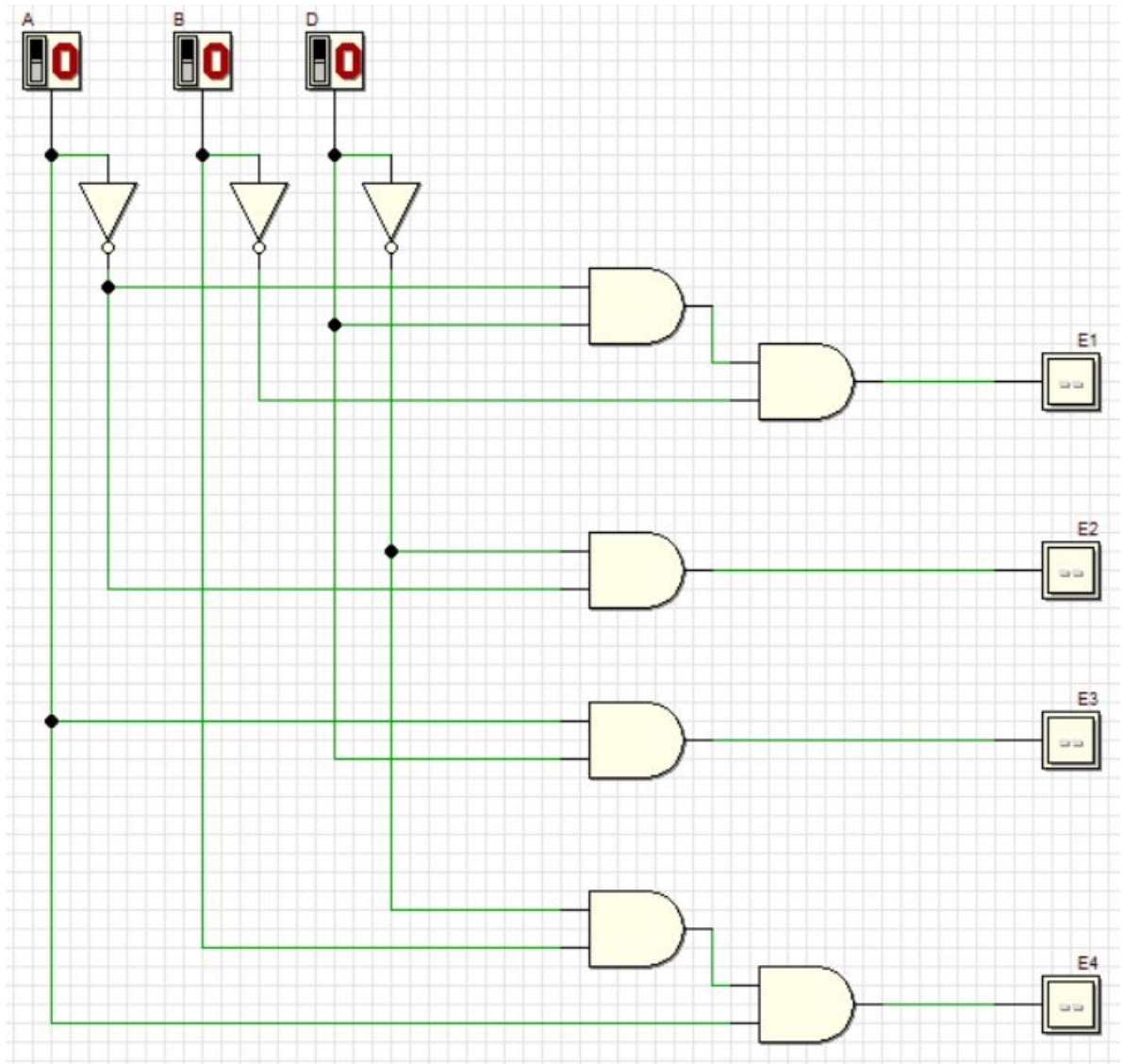
SOP Exp For E3: $A D$

K-Map For E4:

		CD			
		00	01	11	10
AB	00	0	0	X	0
	01	0	X	0	X
	11	X	0	0	1
	10	0	X	0	X

SOP Exp for E4: $A B \bar{D}$

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

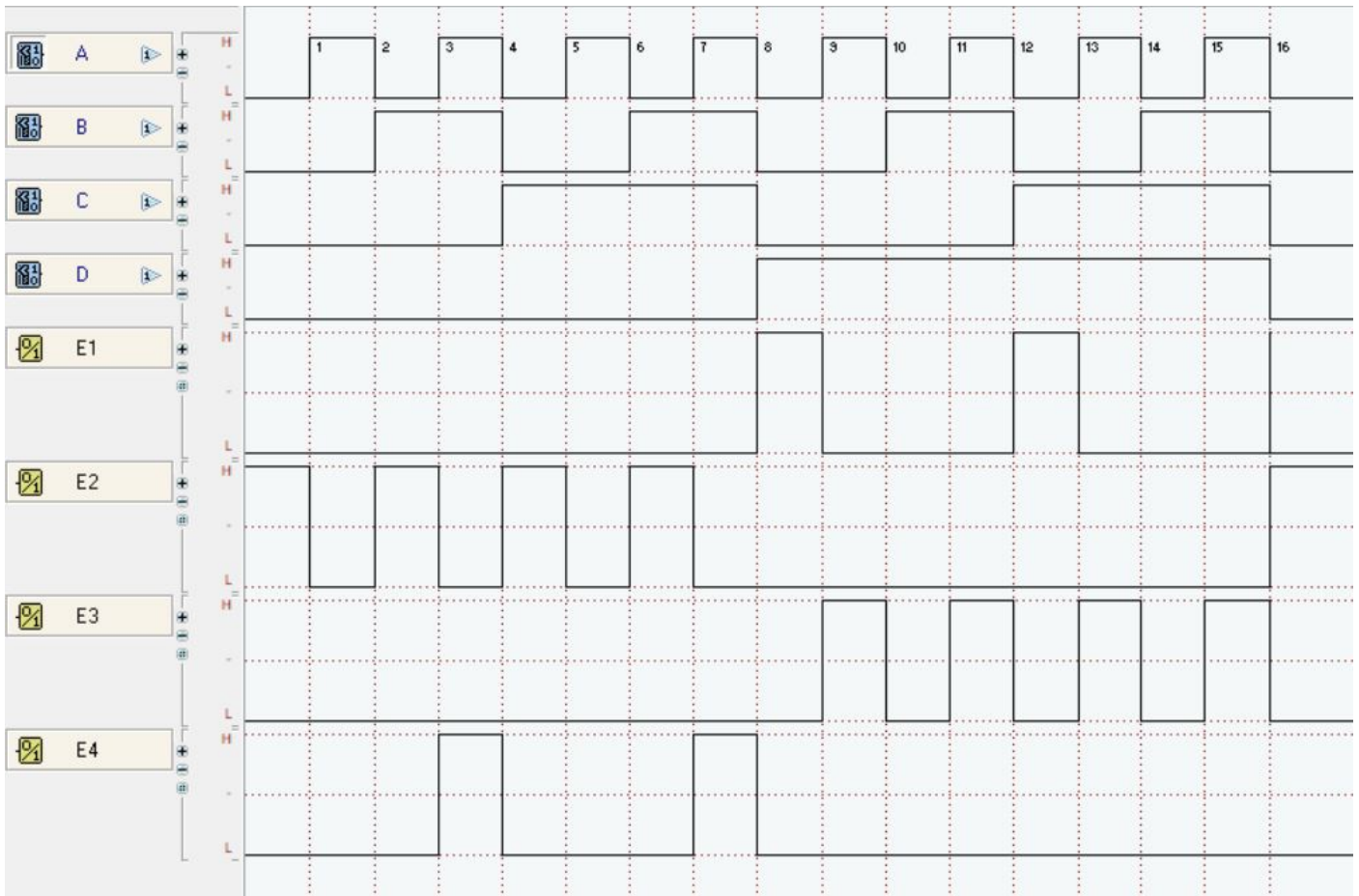
Truth Table 2

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	1
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

The output of E1, E2, E3 and E4 is same in Truth Table 2 and Truth Table 1. The only difference is the don't cares (X) in Truth Table 1 doesn't appear in Truth Table 2. However, the value of don't cares can be either 1 or 0. Thus it is accepted.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

The outputs is independent of the input C. Input C does not affect the outputs

Output E1 is only HIGH when:

- A = 0, B = 0, D = 1

Output E2 is only HIGH when:

- A = 0, B = 0, D = 0
- A = 0, B = 1, D = 0

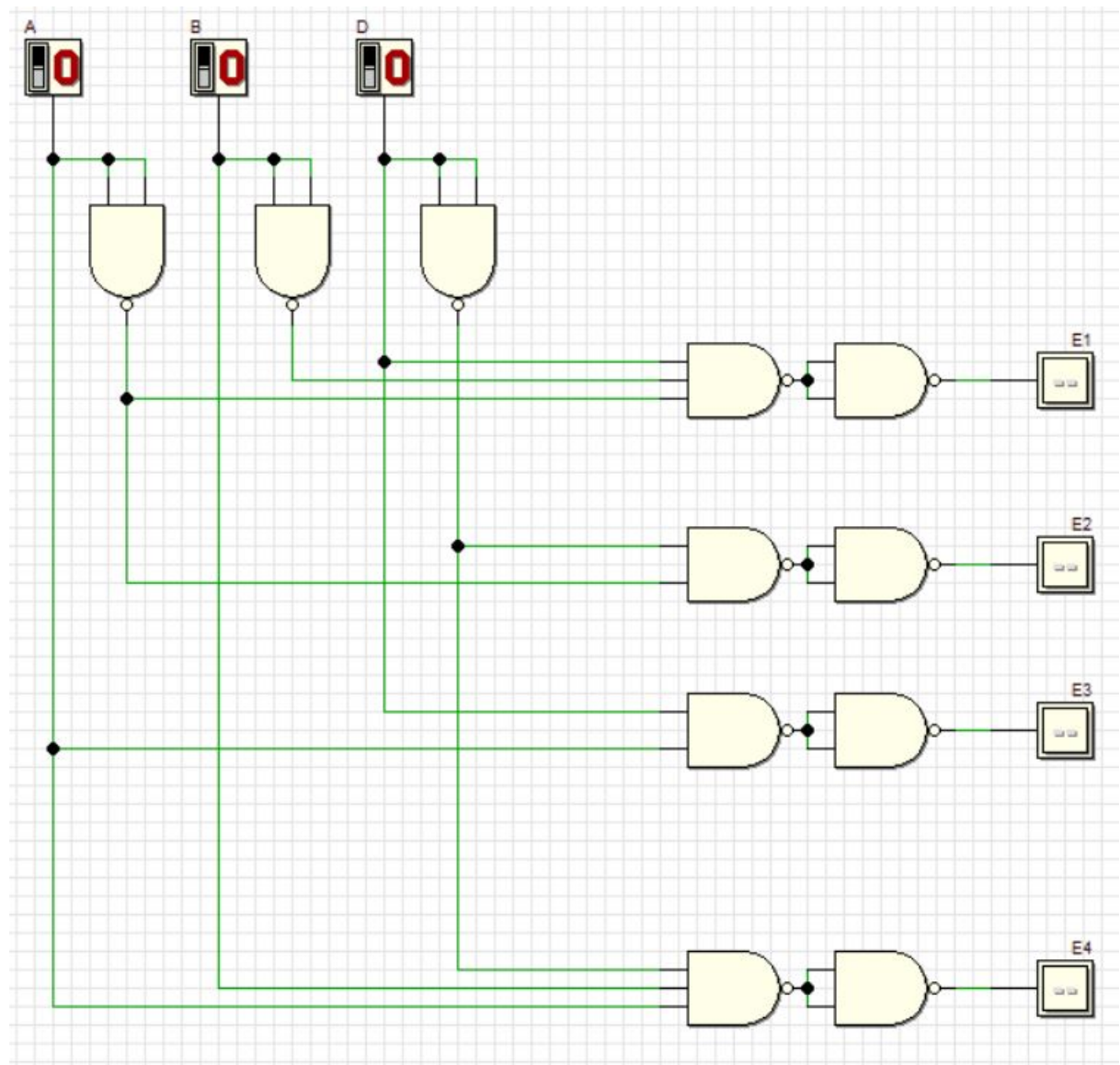
Output E3 is only HIGH when:

- A = 1, B = 0, D = 1
- A = 1, B = 1, D = 1

Output E4 is only HIGH when:

- A = 1, B = 1, D = 0

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

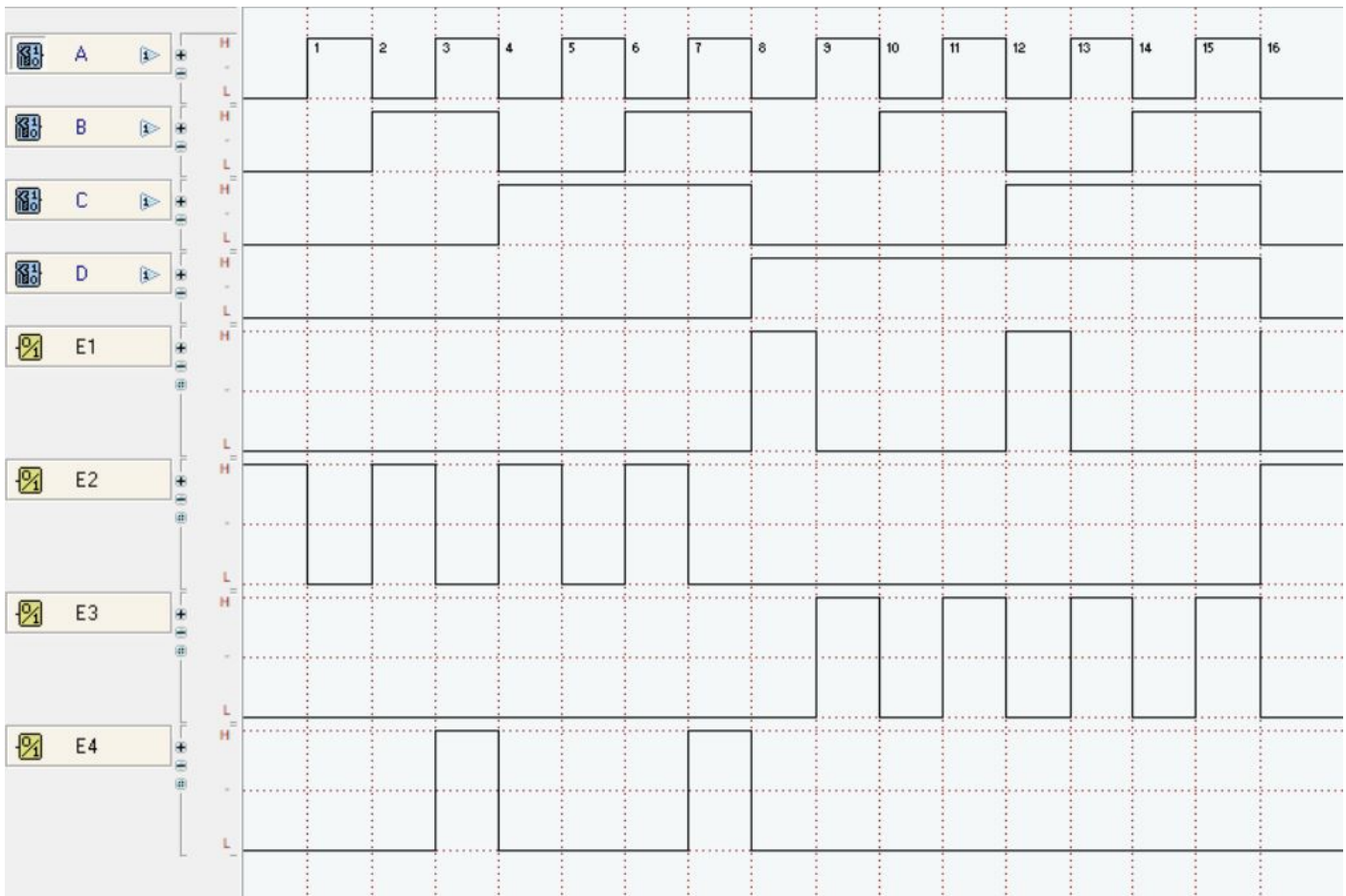
Truth Table 3

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	1
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

Both truth table 3 and Truth table 2 has the exact same outputs at E1, E2, E3 and E4. Therefore, it can be concluded that NAND gate is one of the universal gates which is able to replace basic gates

b) Timing Diagram



Explain some analysis values based on your timing diagram:

The Timing Diagram is exactly same as the timing diagram of previous circuit implemented using basic gates. Therefore the circuit is equivalent although the gates used is different

The outputs is independent of the input C. Input C does not affect the outputs

Output E1 is only HIGH when:

- $A = 0, B = 0, D = 1$

Output E2 is only HIGH when:

- $A = 0, B = 0, D = 0$
- $A = 0, B = 1, D = 0$

Output E3 is only HIGH when:

- $A = 1, B = 0, D = 1$
- $A = 1, B = 1, D = 1$

Output E4 is only HIGH when:

- $A = 1, B = 1, D = 0$



Fully
Completed



Partially
Completed



Checked

