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Date

Lab Activities

Part 1

simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow :

$$Y = AB + BC + AC$$

1) Convert the non-standard Boolean expression into standard form.

$$\begin{aligned} Y &= AB + BC + AC \\ &= AB(C + \bar{C}) + BC(A + \bar{A}) + AC(B + \bar{B}) \\ &= ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C \\ &= ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C \end{aligned}$$

2) Based on standard form expression, complete the following truth table.

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

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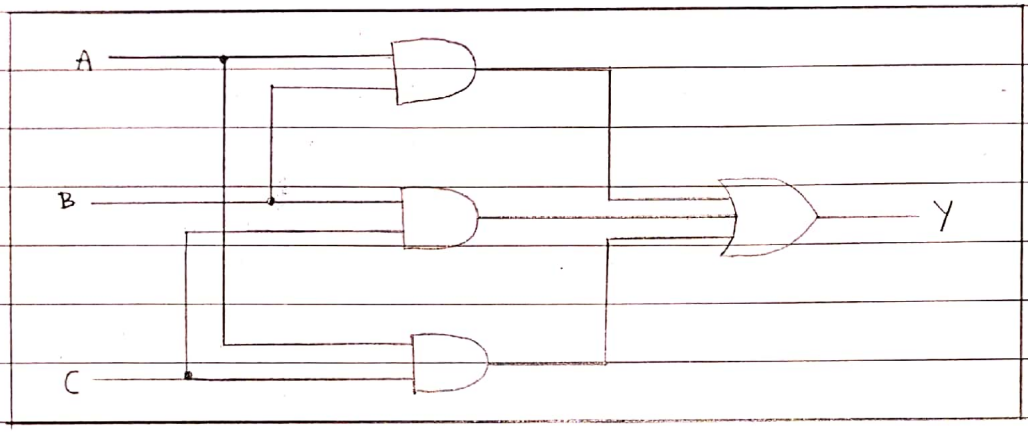
Date.....

3) Using Deeds Simulator, draw the following circuits:

a) circuit (i) for non-standard form (based on given expression)

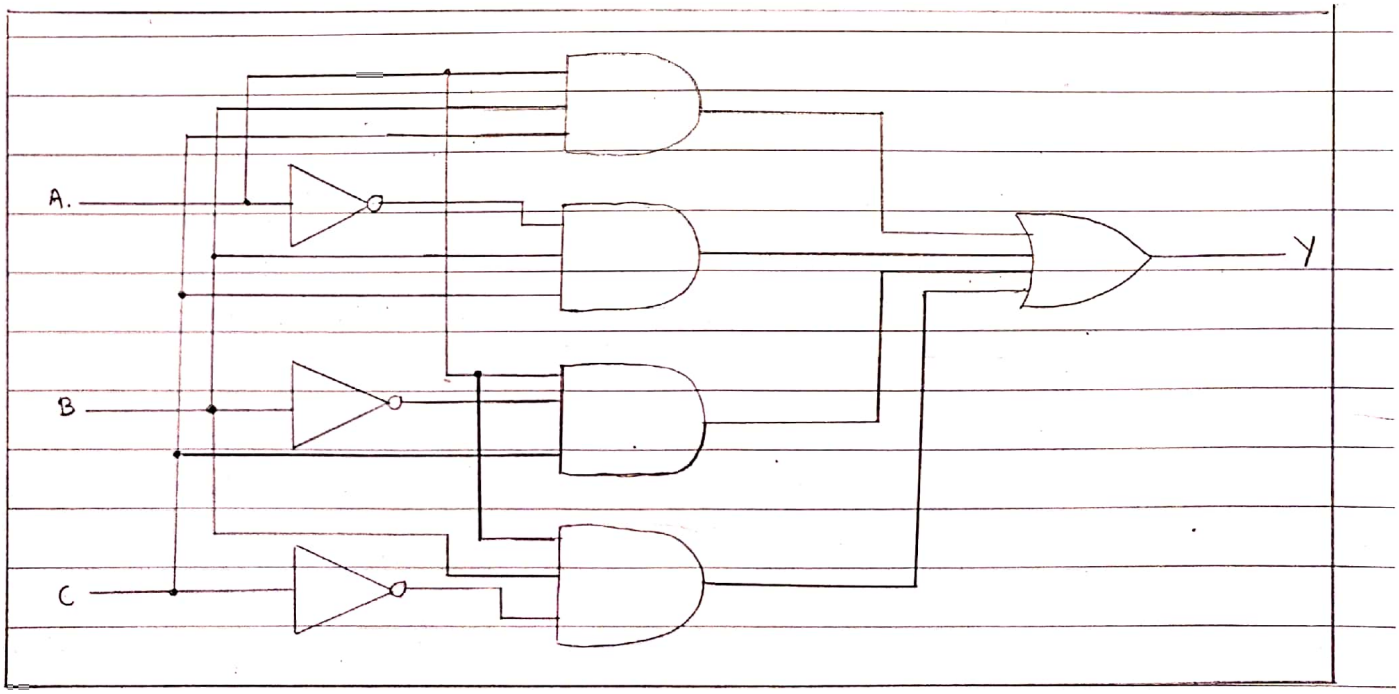
$$Y = AB + BC + AC$$



circuit (i)

b) circuit (ii) for standard form (from answer in question 1)

$$Y = ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$$



circuit (ii)

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4) Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables.

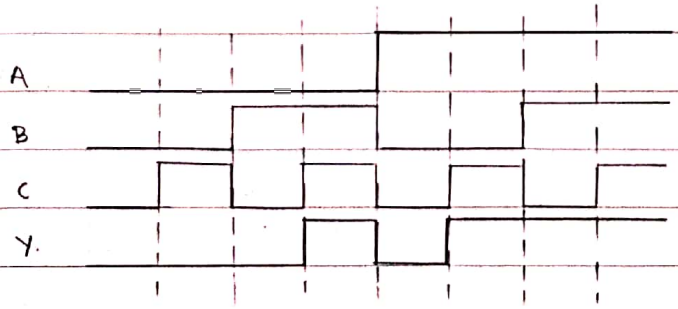
What is your conclusion?

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Input			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion : these two circuits in step 3 have same output. The non-standard and standard form expression provide same output.

5) Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



Part 2 (FATIN AIMI AYUNI BINTI AFFINDY & BILKIS MUSA)

Combinational circuit design process and simulate with Deeds Simulator.

Design Process

i) Determine Parameter Input / Output and their relations.
ii) Construct Truth Table.
iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.
iv) Draw the circuit and use duality symbol; convert AND-OR circuit to NAND gates ONLY.
v) Simulate the design using Deeds Simulator. Check the results according to Truth Table and Timing Diagram Operation.

Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.

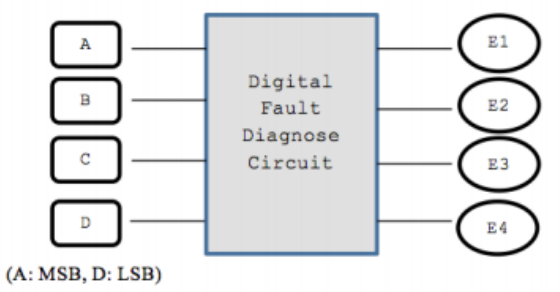


Figure 5

The following rules are used to activate the error's signal type:

RULE 1: E1 is activated if the input number is positive ODD and the majority of the bits is '0'.
RULE 2: E2 is activated if the input number is positive EVEN and the majority of the bits is '0'.
RULE 3: E3 is activated if the input number is negative ODD and the majority of the bits is '1'.
RULE 4: E4 is activated if the input number is negative EVEN and the majority of the bits is '1'.
RULE 5: The output of error signal is invalid if the input has equal bit '0' and bit '1'.

(NOTE: Positive ODD is positive numbers that are odd and negative EVEN is negative numbers that are even).

Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 1

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.

E1

AB \ CD	00	01	11	10
00	0	1	X	0
01	0	X	0	X
11	X	0	0	0
10	0	X	0	X

0001
0011
A'B'D

E2

AB \ CD	00	01	11	10
00	1	0	X	1
01	1	X	0	X
11	X	0	0	0
10	0	X	0	X

0000
0100
0010
0110
A'D'

E3

AB \ CD	00	01	11	10
00	0	0	X	0
01	0	X	0	X
11	X	1	1	0
10	0	X	1	X

1101
1111
1001
1011
AD

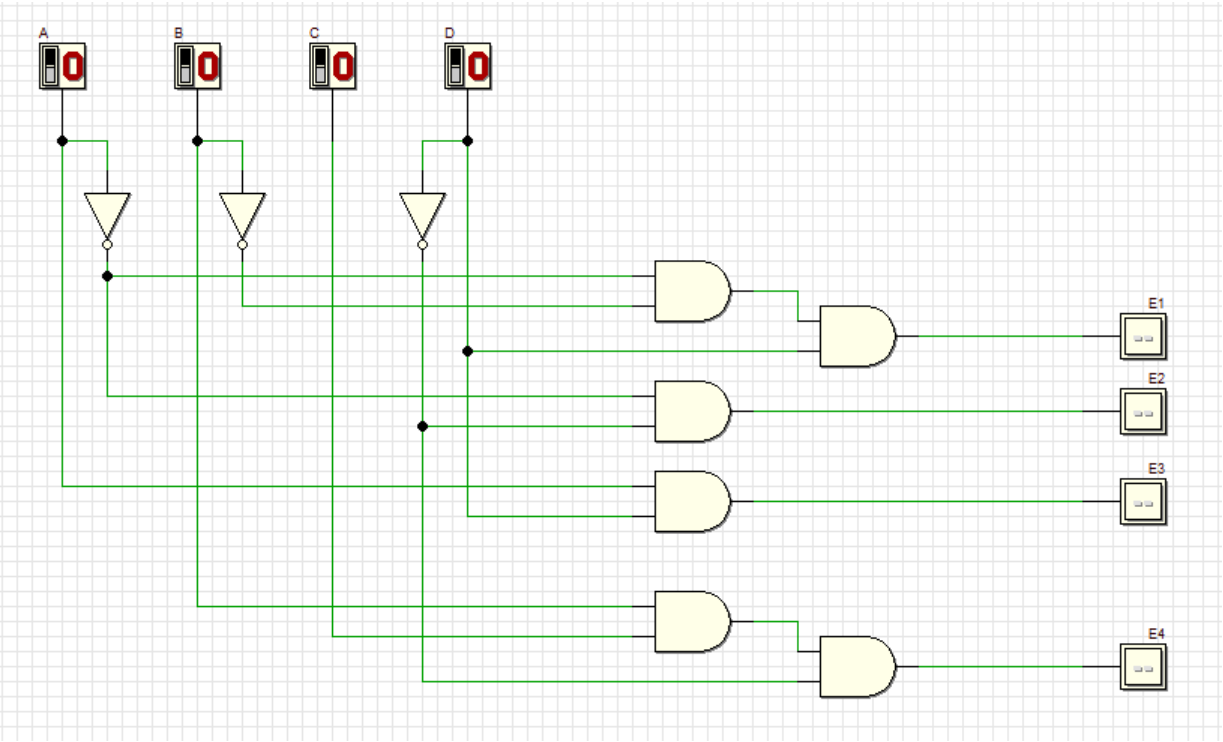
E4

AB \ CD	00	01	11	10
00	0	0	X	0
01	0	X	0	X
11	X	0	0	1
10	0	X	0	X

0110
1110
BCD'

E1 = A'B'D **E2 = A'D'** **E3 = AD** **E4 = BCD'**

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

Truth Table 2

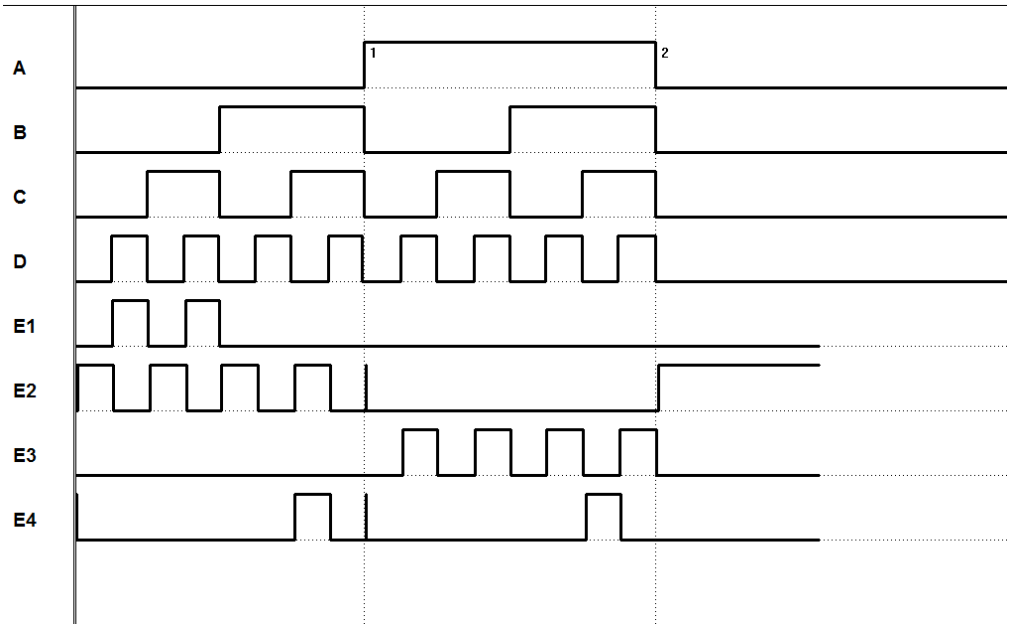
INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

In Truth Table 1, output for E1 will be high if the input is positive ODD and majority of bits '0', E2 will be high if the input is positive EVEN and majority of bits '0', E3 will be high if the input is negative ODD and majority of bits '1', E4 will be high if input is negative EVEN and majority of bits '1', and the output is error if the bit '0' and '1' are equal which we treat them as a don't care value.

In Truth Table 2, output for E1 will be high if A=0, B=0, C=0, D=1 **or** A=0, B=0, C=1, D=1, E2 will be high if all inputs are LOW **or** A=0, B=0, C=1, D=0 **or** A=0, B=1, C=0, D=0 **or** A=0, B=1, C=1, D=0, E3 will be high if A=1, B=0, C=0, D=1 **or** A=1, B=0, C=1, D=1 **or** A=1, B=1, C=0, D=1 or all inputs are HIGH and E4 will be high if A=0, B=1, C=1, D=0 **or** A=1, B=1, C=1, D=0. There is no don't care value in Truth Table 2

b) Timing Diagram



Explain some analysis values based on your timing diagram:

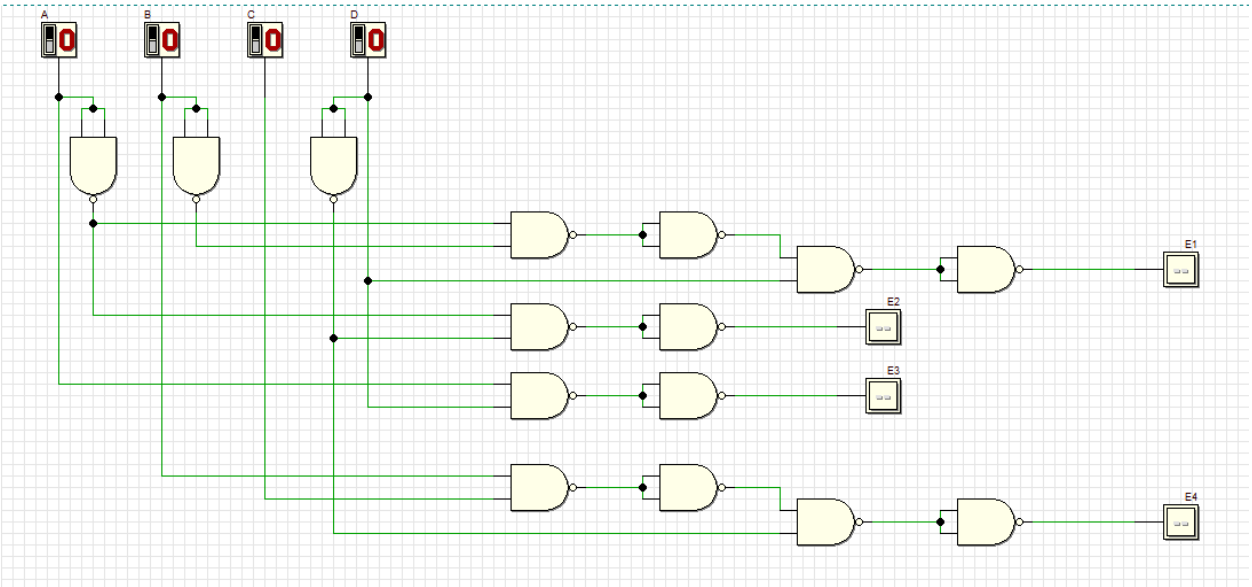
Output E1will be HIGH if A and B are LOW and D is HIGH

Output E2 will be HIGH if A and D are LOW

Output E3 will be HIGH if A and D are HIGH

Output E4 will be HIGH if B and C are HIGH and D is LOW

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

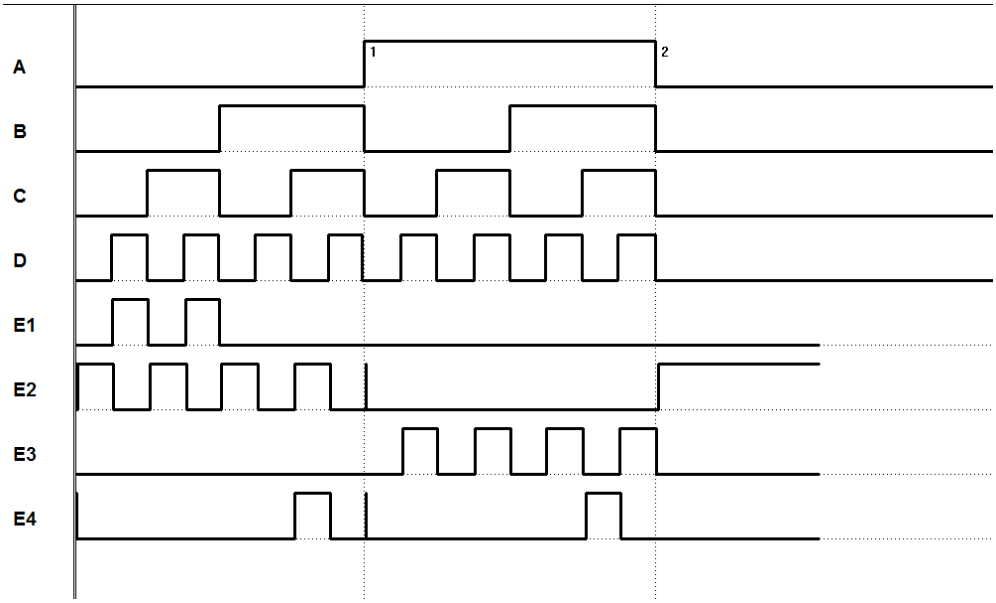
Truth Table 3

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

The output results in Truth Table 3 and Truth Table 2 are the same because both circuits are actually the equivalent, only the gates are not the same. Truth Table 3 uses the same gate for the whole circuit meanwhile the Truth Table 2 uses different gates in the circuit. However, both are actually the same.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

Output E1will be HIGH if A and B are LOW and D is HIGH

Output E2 will be HIGH if A and D are LOW

Output E3 will be HIGH if A and D are HIGH

Output E4 will be HIGH if B and C are HIGH and D is LOW