Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT	:	SCSR1013 DIGITAL LOGIC
SESSION/SEM	:	02/1
LAB 1	**:**	**COMBINATIONAL LOGIC**
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DATE	:	17 November 2020

REMARKS :

MARKS:

Lab # 1

Introduction to Logic Circuits

A. Objectives

The objectives of this laboratory are to introduce the student to:

- basic bread boarding and wiring techniques
- the use of input switches and output LEDs in generating truth tables for a combinational logic circuit
- to verify the characteristic of the basic gates

B. Materials

- Breadboard
- 7408 Quad 2-input AND - 1
- 7404 Hex Inverter - 1
- 7400 Quad 2-input NAND - 1
- 7432 Quad 2 –input OR - 1
- ETS-5000 Digital Training kit

C. Introduction

This lab focuses on several practical issues related to bread boarding and testing combinational logic circuits. Several helpful points are made below.

Wire gauge - Use only 22-gauge wire. The breadboard may be damaged by forcing smaller gauge (larger diameter) wire into the holes.

Wire color - Use organized color schemes when wiring circuits. For example, use RED wire for all V_{cc} connections, BLACK wire for all ground connections, BLUE wire for all input switches, and YELLOW wire for all intermediate signal connections.

Wire length and placement - Use wires that are the appropriate length so that they can lie flat on the breadboard. Avoid running wires over IC's in case the IC's need to be removed.

Testing IC's - Chip tester is available in lab, always check your IC's before you begin wiring the circuit.

Inserting IC's - IC's are not difficult to insert in the socket strips once they have been properly adjusted. Brand new IC's are shipped with their pins bent apart from the vertical (typically 15° outward) in order to facilitate handling by automatic insertion equipment. Therefore, before an IC is used for the first time its pins must be bent back so that their spacing is vertical.

IC Orientation - Arrange all IC's in the same direction. This will facilitate connecting V_{cc} on each IC to a 5V strip on the breadboard and GND on each IC to a ground strip. If an IC is reversed (thus V_{cc} and ground are reversed), it may be destroyed. It is recommended that you begin wiring by making all V_{cc} and ground connections.

IC Removal - It is recommended that you use some sort of extraction tool for removing IC's. Attempts to remove IC's by hand may result in bent pins.

Monitoring the logic level of the circuit

Use the LED (at the top right of the digital kit) to monitor the logic level of the digital circuit. A GREEN indicates that the logic level is LOW (0) and a RED means the logic level is HIGH (1). If the LED does not lit, there is something wrong with the circuit. Switch off the power supply and recheck the circuit.

Note: Please be certain that the MODE switch is flip to TTL not CMOS.

You can use a logic probe (at the bottom right of the digital circuit) to monitor the logic level of any node (point) of the circuit. **H** indicates logic HIGH (1), **L** means LOW (0) and **P** means pulse (the signal keeps on changing between HIGH and LOW).

Switches

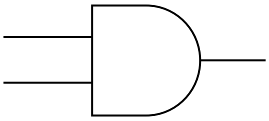
There are 8 toggle switches at the bottom row of the digital circuit. These switches will provide a logic input of HIGH (1) and LOW (0) to the circuit.

D. Preiminary Work

1. Draw a symbol, determine the IC number and produce a truth table for the following gate.

AND

Symbol:



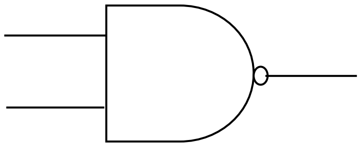
IC Number: 7408

Truth Table 1

Input		Output
A	B	F
1	1	1
1	0	0
0	1	0
0	0	0

NAND

Symbol:

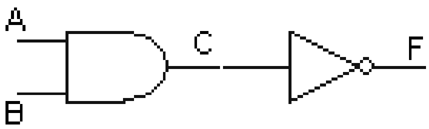


IC Number: 7400

Truth Table 2

Input		Output
A	B	F
1	1	0
1	0	1
0	1	1
0	0	1

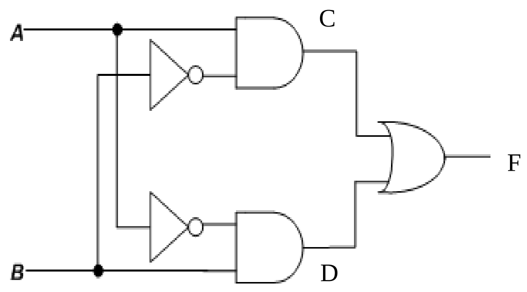
2. Complete the truth table for the following circuit.



Truth Table 3

A	B	C	F
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	1

3. Write the Boolean expression for output C, D and F the following circuit.



C $= (A \wedge - B)$

D $= (-A \wedge B)$

F $=(A \wedge - B) \vee (-A \wedge B)$

4. Complete the truth table for the circuit in (3) based on the Boolean expression produced for C, D and F.

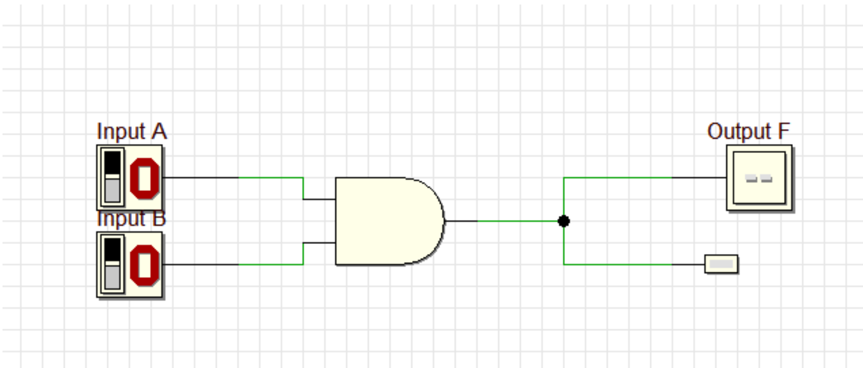
Truth Table 4

A	B	C	D	F
1	1	0	0	0
1	0	1	0	1
0	1	0	1	1
0	0	0	0	0

E. Laboratory Work

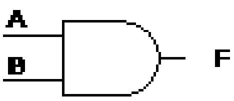
Part 1

1. Construct Circuit 1 on the breadboard. Connect all inputs (A, B) to a switches and output F to LEDs.



Truth Table 5

Input		Output
A	B	F
1	1	1
1	0	0
0	1	0
0	0	0



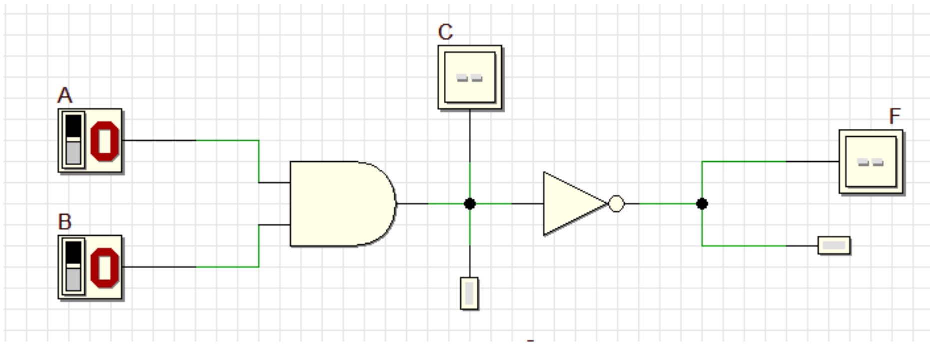
Circuit 1

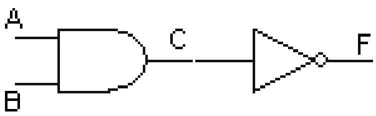
2. Test Circuit 1 and fill in Truth Table 5 for the circuit response to all possible input combinations. The Truth Table 5 should match the Truth Table 1 prepared in the Preliminary Work.

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* ________

Part 2

3. Construct Circuit 2 on the breadboard. Connect all inputs (A, B) to a switches and output C and F to LEDs.





Circuit 2

Truth Table 6

A	B	C	F
1	1	1	0
1	0	0	1
0	1	0	1
0	0	0	1

4. Test Circuit 2; fill in Truth Table 6, for the circuit response to all possible input combinations.

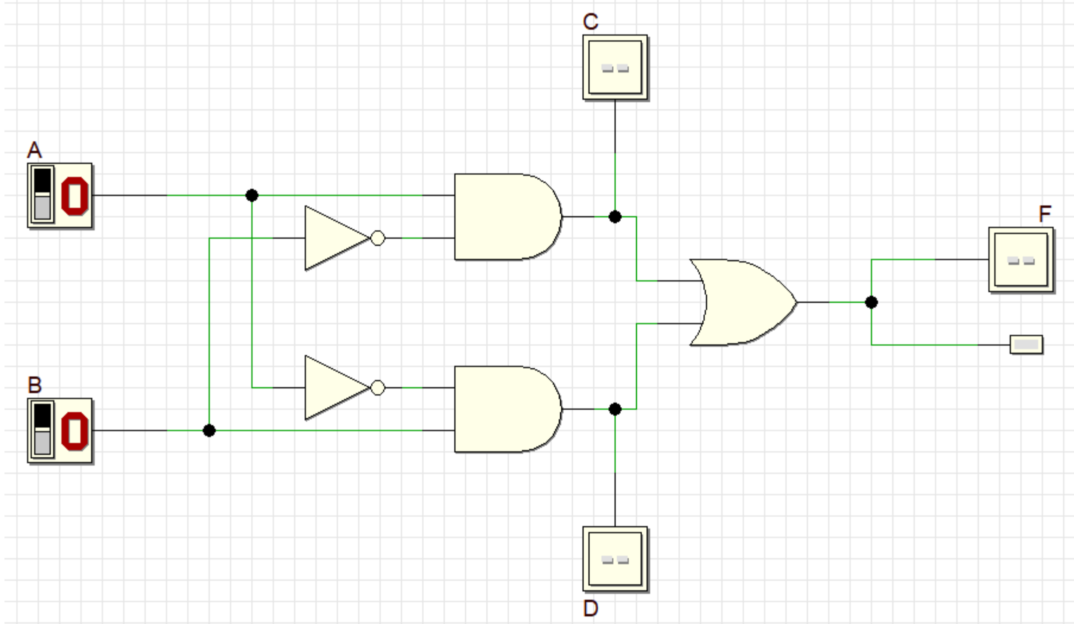
5. Compare Truth Table 6 to Truth Table 2. What conclusion can you make?

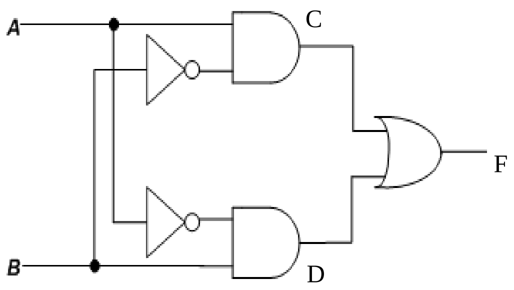
   Conclusion that I can make is AND gate combine with NOT gate will produce NAND gate.

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* ________

Part 3

6. Construct circuit 3 on the breadboard. Connect all inputs (A, B) to a switches and output C, D and F to LEDs.





Circuit 3

Truth Table 7

A	B	C	D	F
1	1	0	0	0
1	0	1	0	1
0	1	0	1	1
0	0	0	0	0

7. Test Circuit 3; fill in Truth Table 7 for the circuit outputs (C, D, and F) for all possible input combinations.

8. What single gate does Circuit 3 represent?

- EXOR Gate

Fully Completed ☐ *Partially Completed* ☐ *Checked by:* ________