Digital Logic Lab 3

E. Preliminary Works

1. Using 7476 IC, connect the synchronous input (J, K) of a JK flip-flop to switches and its output (Q) to an LED. Connect the CLK input to a pulser switch, A. Determine the logic level for each input combinations in Table 1so that the desired result can be realized.

Desired Result	$\overline{PRE}$	$\overline{CLR}$	J	K	CLK	Q
Set initial value Q=1	0	1	**X**	**X**	--	1
Output Q stays the same	**1**	**1**	0	0	⇓	1
Output Q become 0, no change in asynchronous input	1	1	0	1	⇓	0
Output Q is not previous Q	**1**	**1**	1	0	⇓	1
RESET Q	**1**	**1**	0	1	⇓	0
SET Q	**1**	**1**	1	0	⇓	1

2. Answer all questions.
   a) Which state that JK flip-flop has, but not on SR flip-flop.
      - Toggle state

   b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip-flop.
      - Negative edge triggered.

F. Lab Activities

1. You are given a counter circuit as shown in Figure 4.

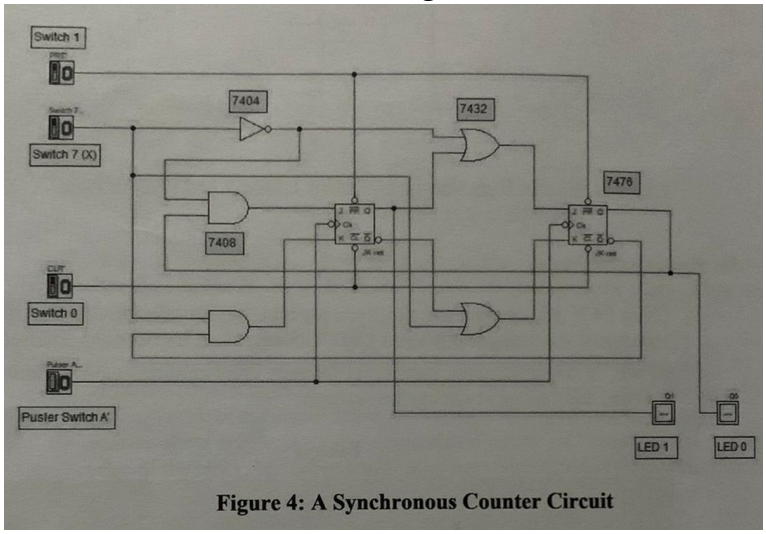
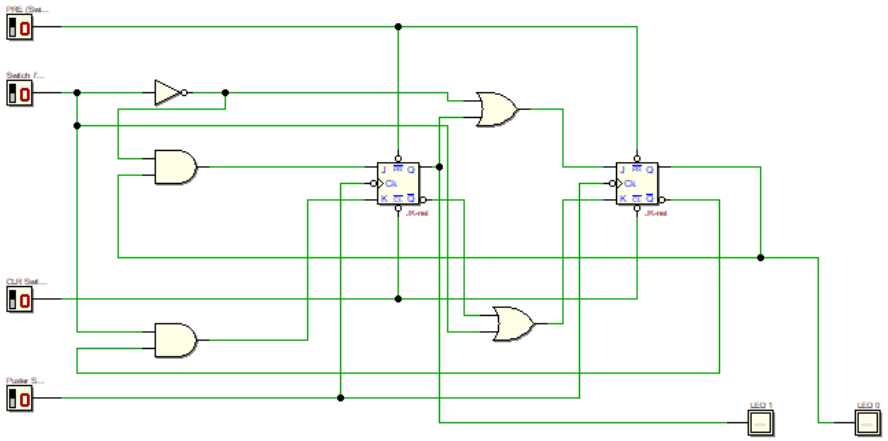


Figure 4: A Synchronous Counter Circuit

2. By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4.

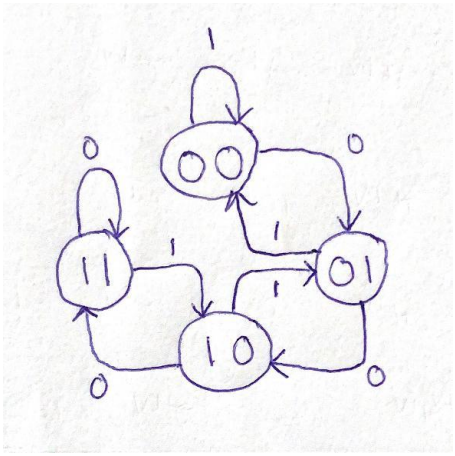


3. Investigate the behavior of the counter by observing the next state of the counter for all combination of Present State and X values. Complete the Next State table of the counter in Table 2. Ensure the Switch 0 is in HIGH state.

Table 2

Switch 7	Present State		Next State	
X	Q1 LED	Q0 LED	Q1 LED	Q0 LED
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

4. By referring to the Next-State in Table 2, sketch the state diagram of the counter.



5. By referring to the Next-State in Table 2 and the state diagram in (4), answer all questions.

a) What is the main indicator to decide that the counter is a synchronous counter?
   - Pulser Switch. The Next-State is referred by the changes in pulser switch only.

b) How many states are available for the counter and what are they?
   - There are three states available, which are no change, Set and Reset.

c) What is the function of Switch 7 (X) in the circuit?
   - Switch 7 (X) acts as a count up and count down.

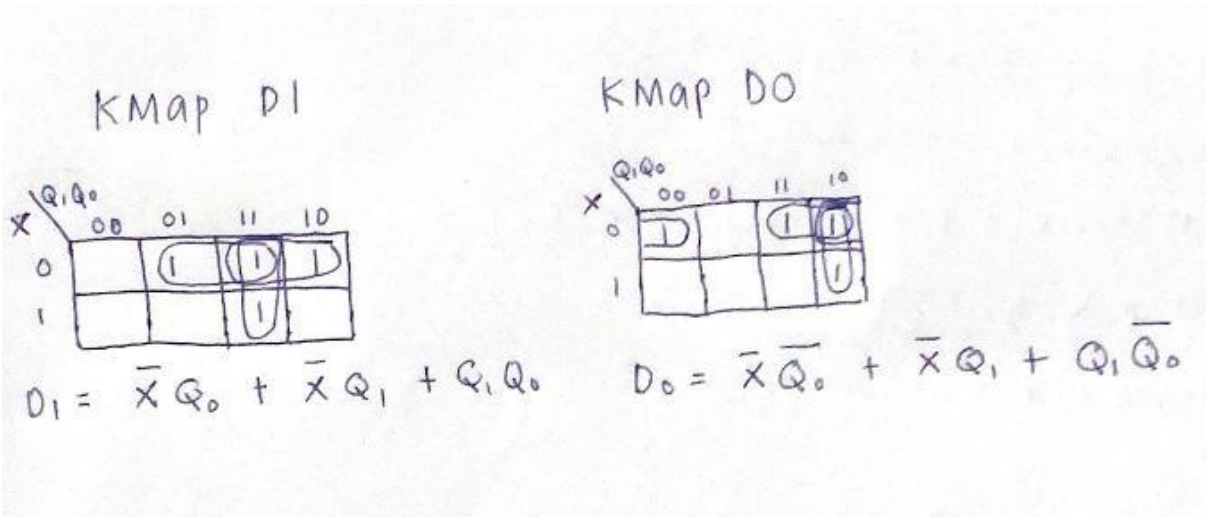
d) What is the function of Switch 0 and Switch 1 in the circuit?
   - Both switches are set as HIGH to make the counter as synchronous counter.

e) Is the counter a saturated counter or recycle counter?
   - Saturated counter.

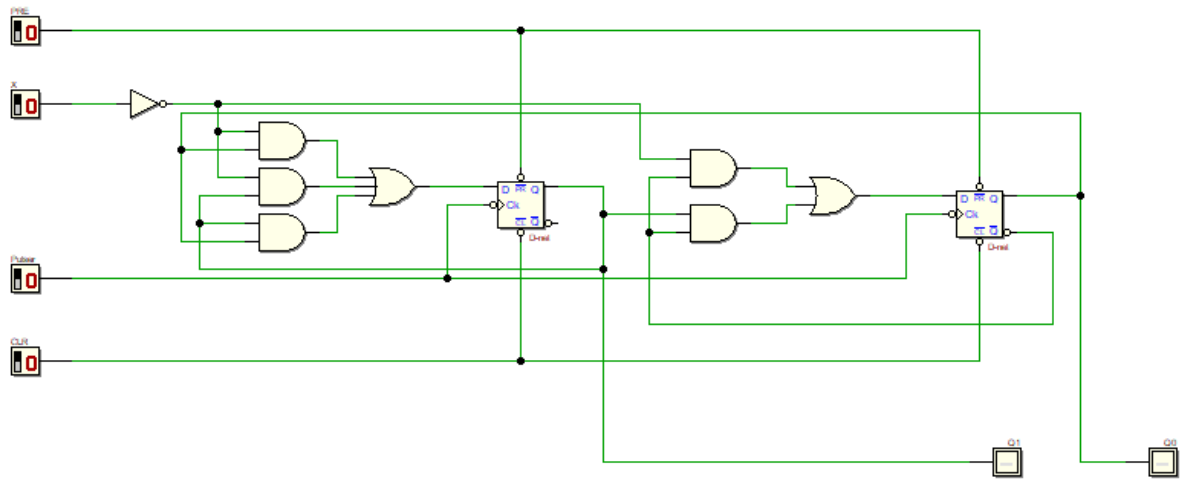
6. Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.
   a) Built the next state and transition table using the header in Table 3.

Input	Present State		Next State		D FF Transition	
X	**Q1**	**Q0**	**Q1+**	**Q0+**	**D1**	D0
0	**0**	**0**	**0**	**1**	**0**	1
0	**0**	**1**	**1**	**0**	**1**	0
0	**1**	**0**	**1**	**1**	**1**	1
0	**1**	**1**	**1**	**1**	**1**	1
1	**0**	**0**	**0**	**0**	**0**	0
1	**0**	**1**	**0**	**0**	**0**	0
1	**1**	**0**	**0**	**1**	**0**	1
1	1	1	1	0	1	0

   b) Get the optimized Boolean expression.

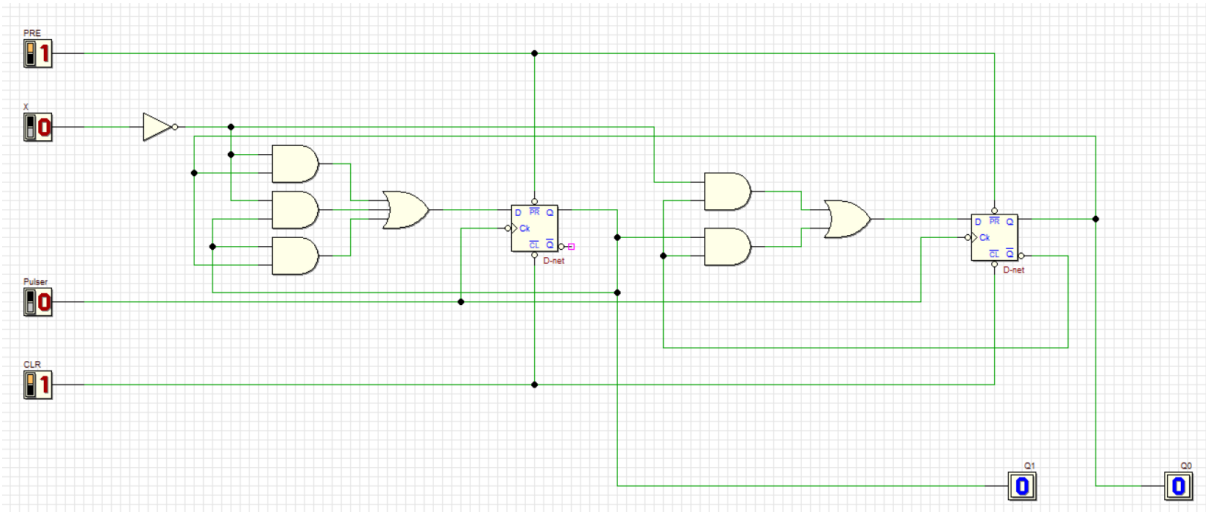


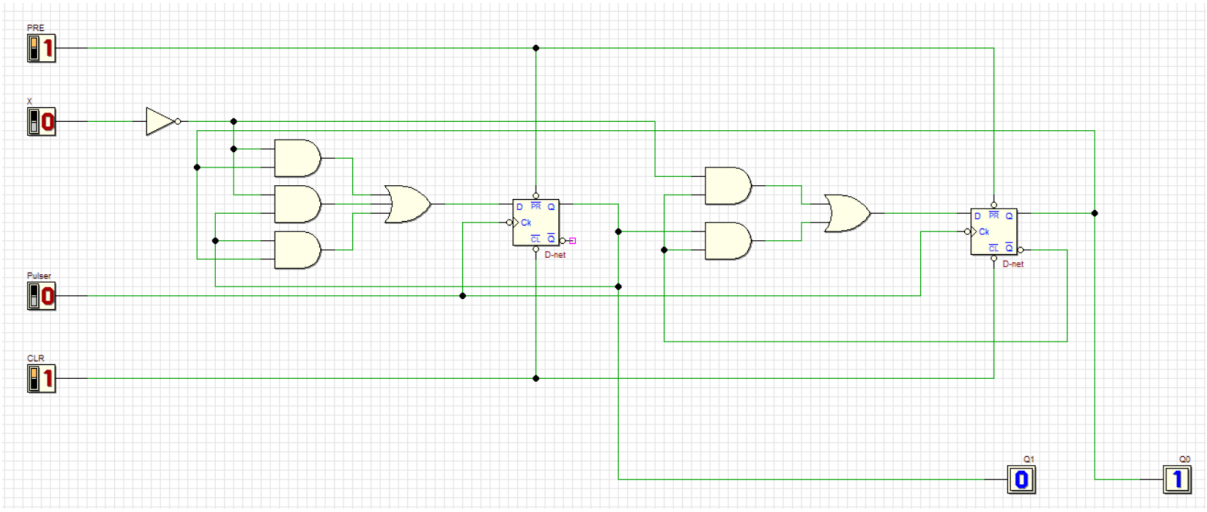
   c) Draw the complete final circuit design in Deeds.

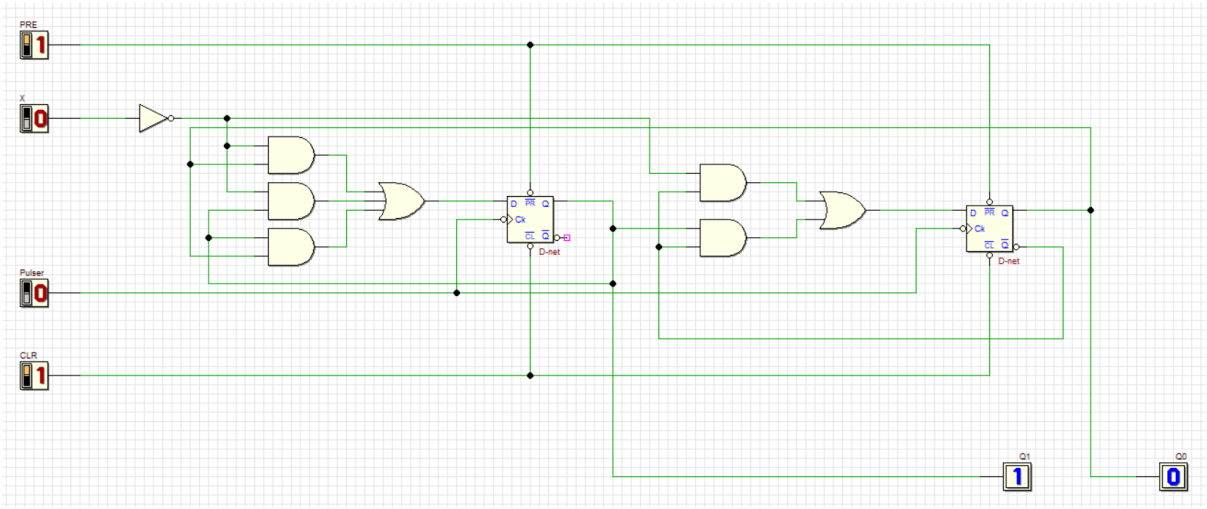


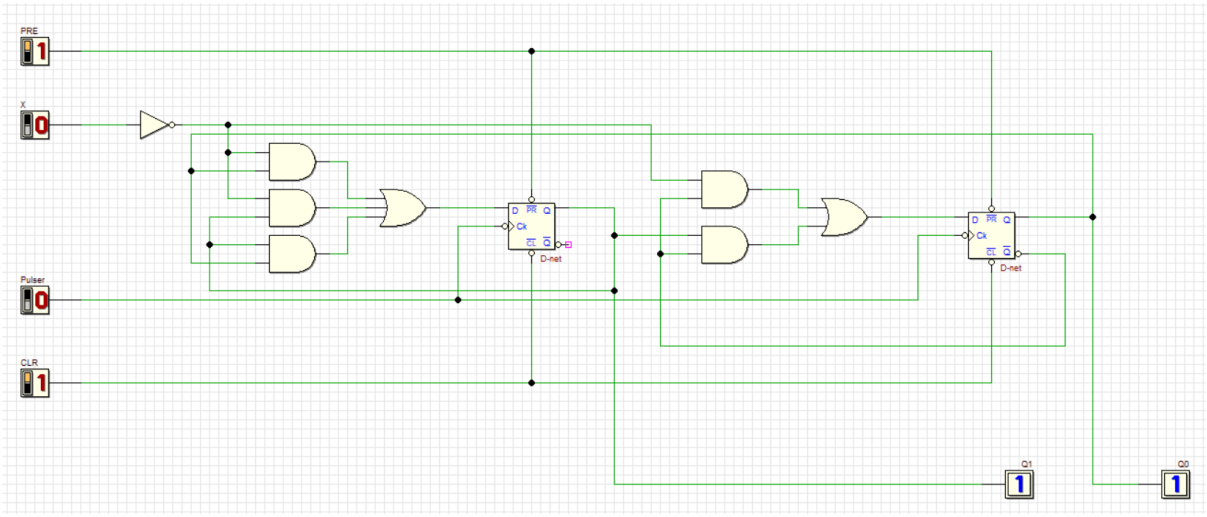
d) Simulate the circuit to prove that your Table 3 is correct.

Input Switch X = 0

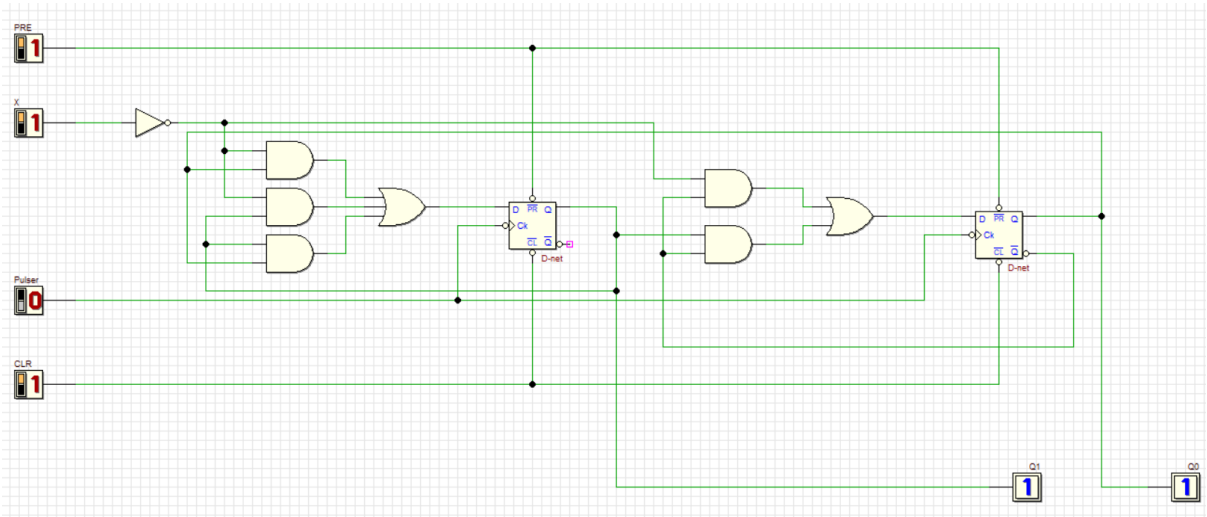


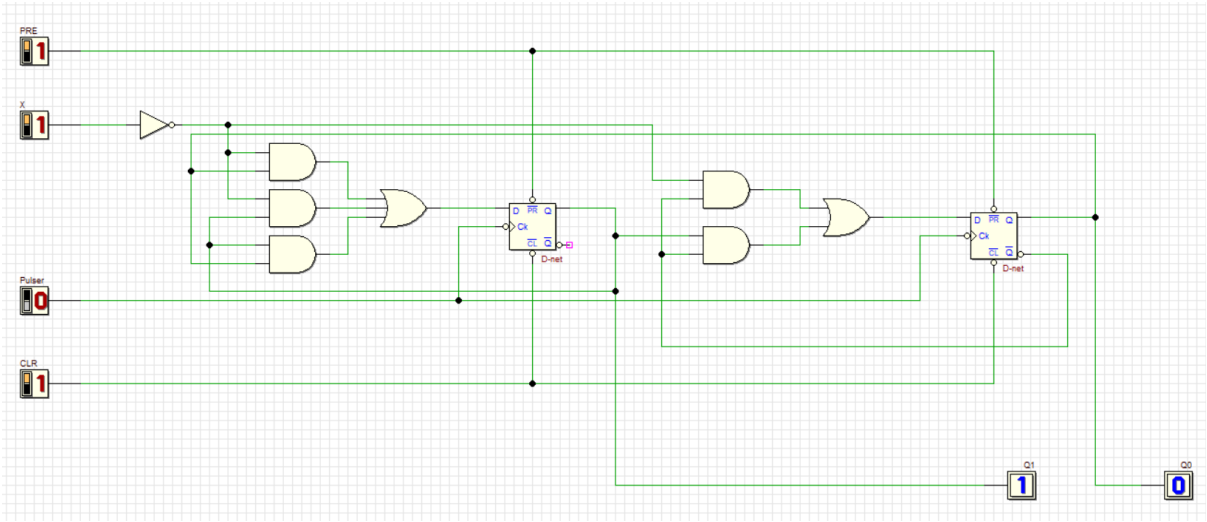


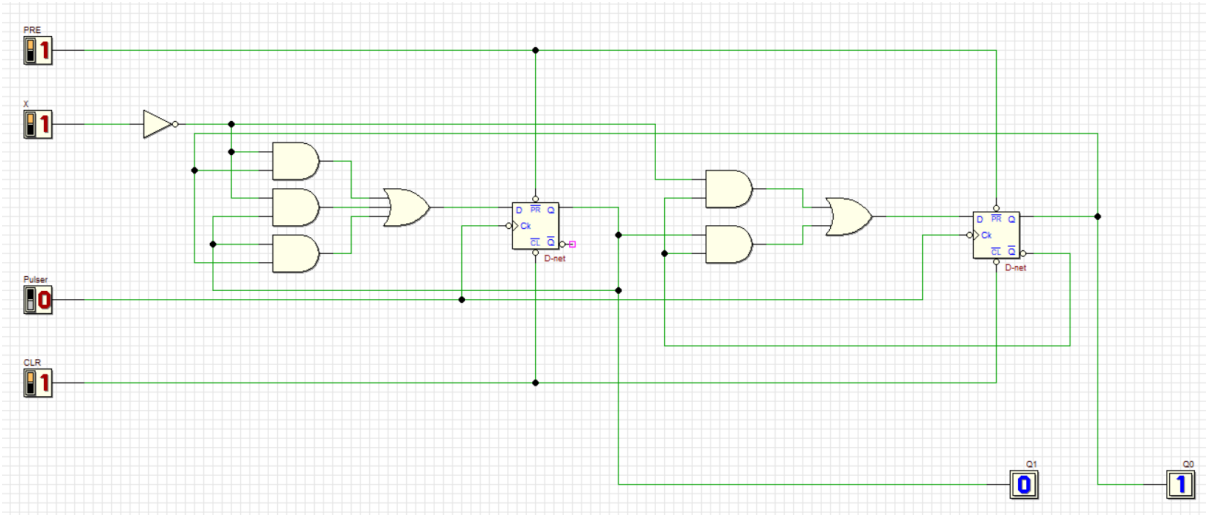


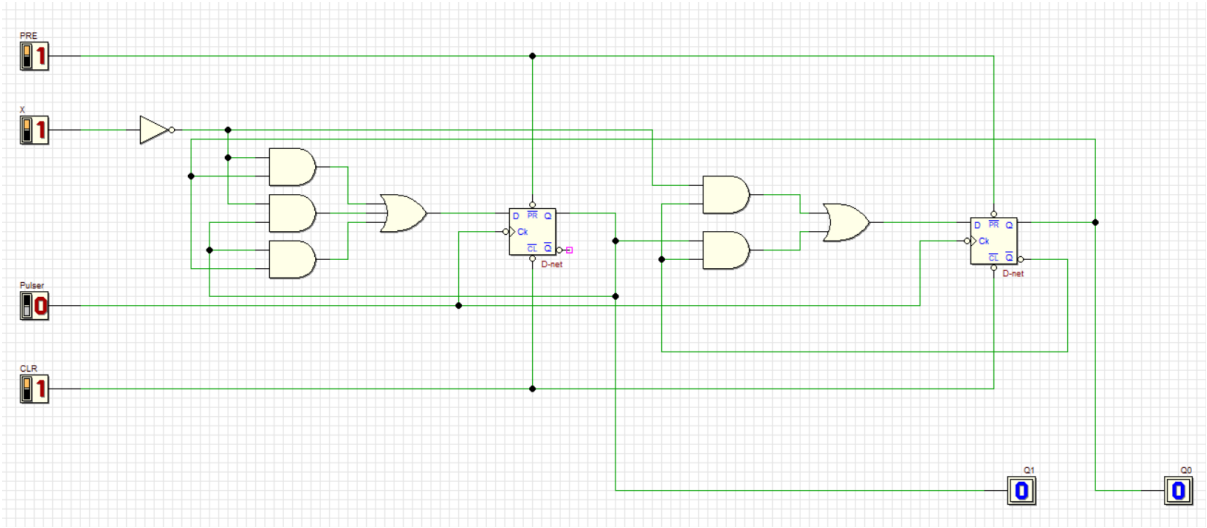


Input Switch X = 1





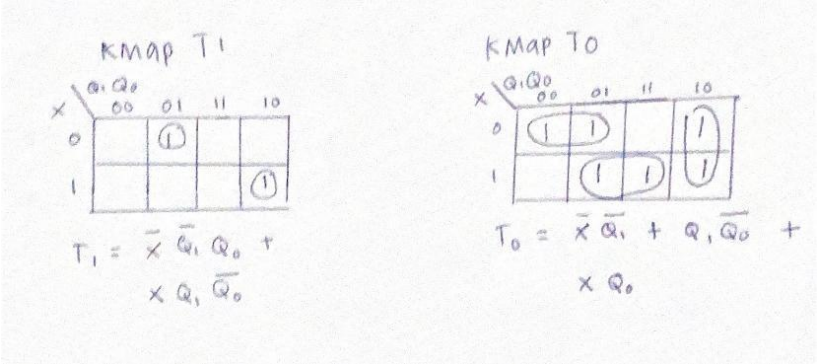




7. Repeat steps in Q (6) using T flip-flop
   a)

Input	Present State		Next State		T FF Transition	
X	**Q1**	**Q0**	**Q1+**	**Q0+**	**T1**	T0
0	**0**	**0**	**0**	**1**	**0**	1
0	**0**	**1**	**1**	**0**	**1**	1
0	**1**	**0**	**1**	**1**	**0**	1
0	**1**	**1**	**1**	**1**	**0**	0
1	**0**	**0**	**0**	**0**	**0**	0
1	**0**	**1**	**0**	**0**	**0**	1
1	**1**	**0**	**0**	**1**	**1**	1
1	1	1	1	0	0	1

b)



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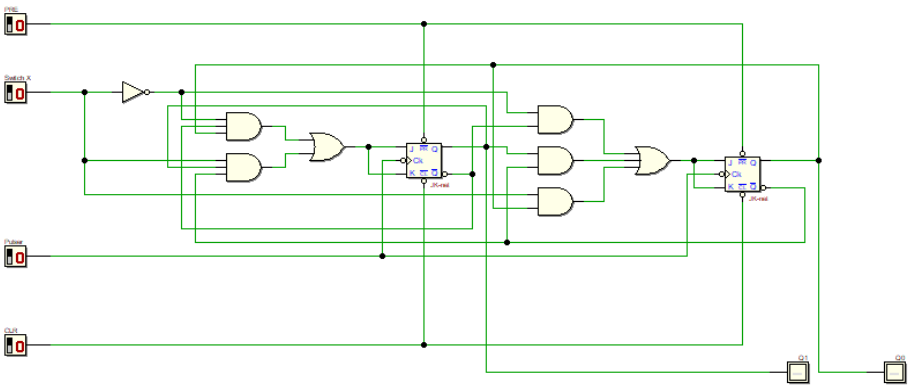

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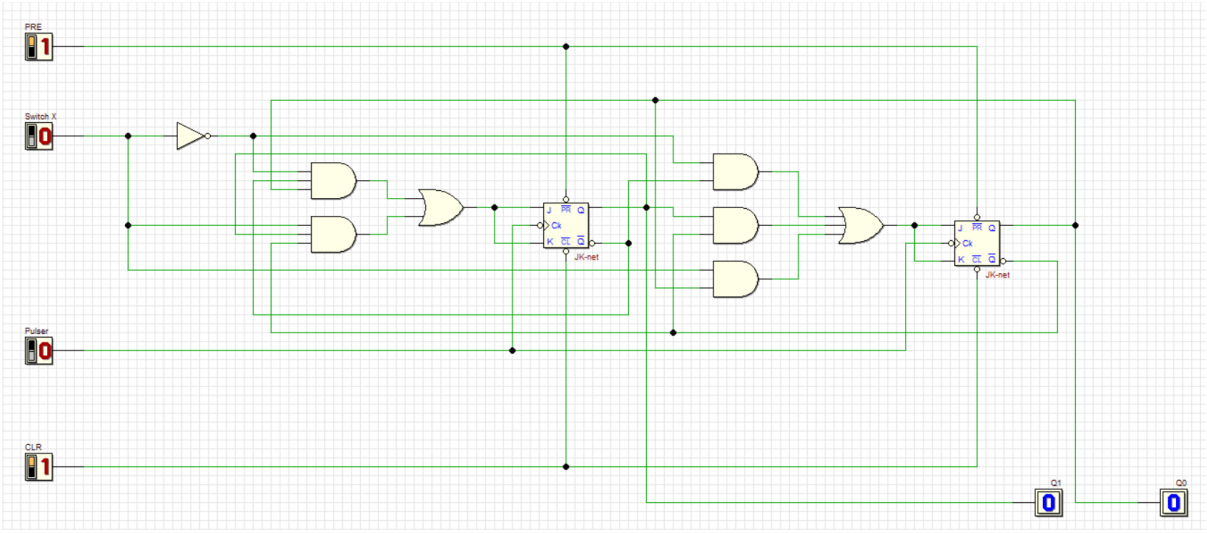
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Switch X
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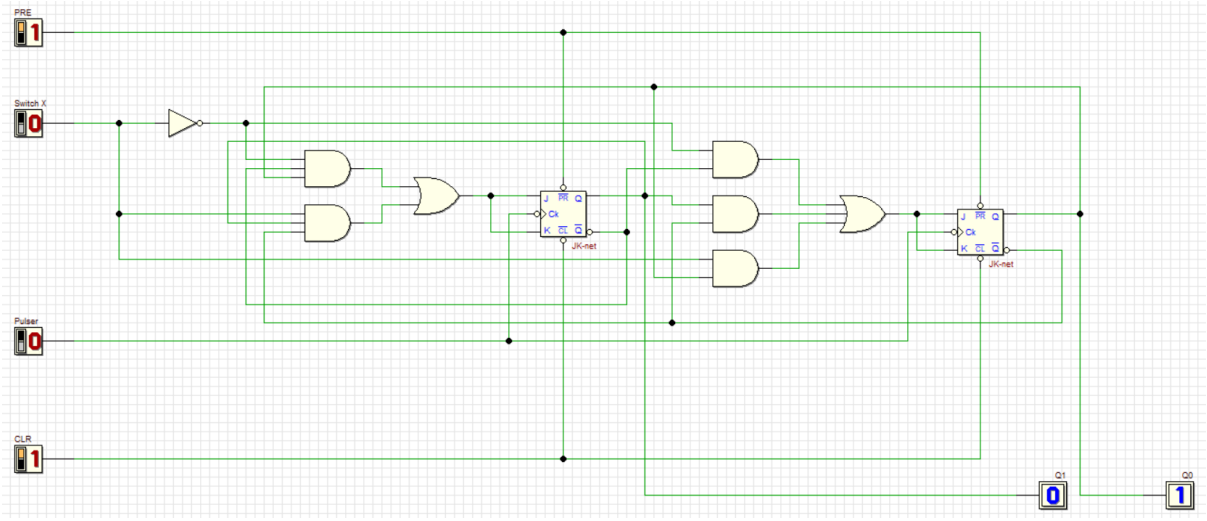
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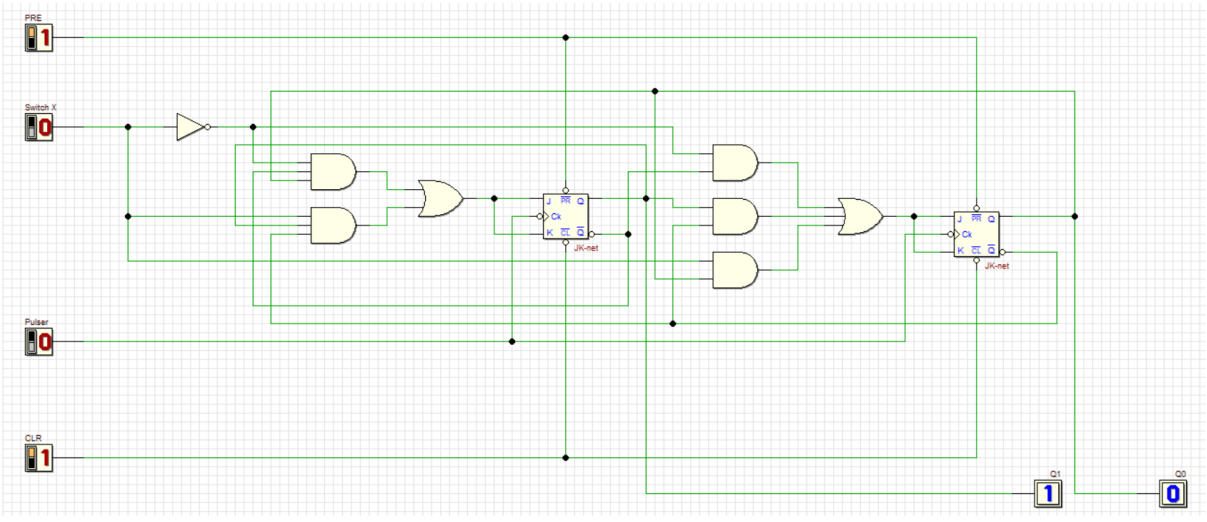
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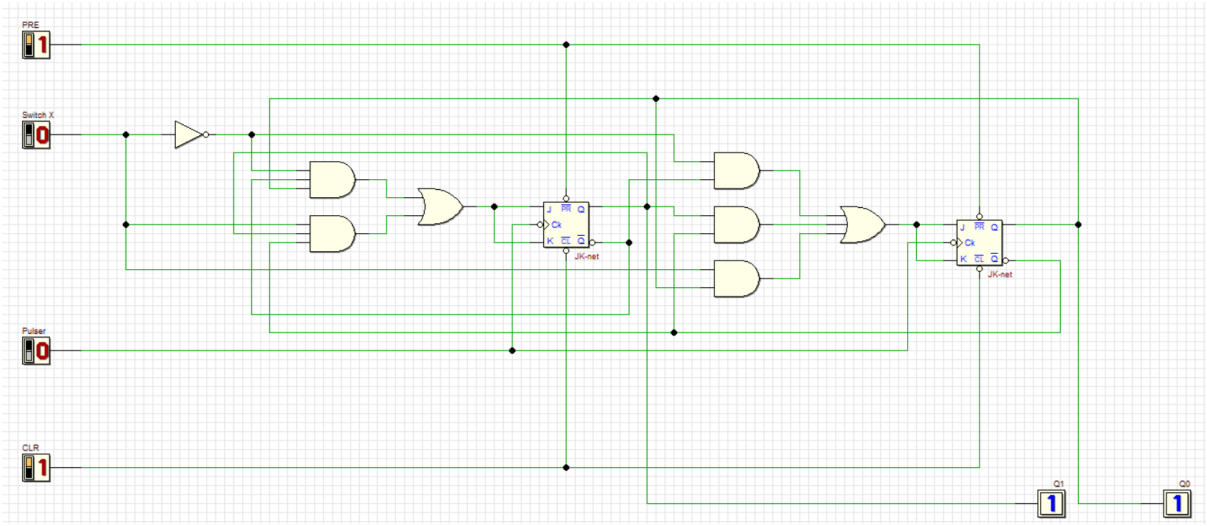
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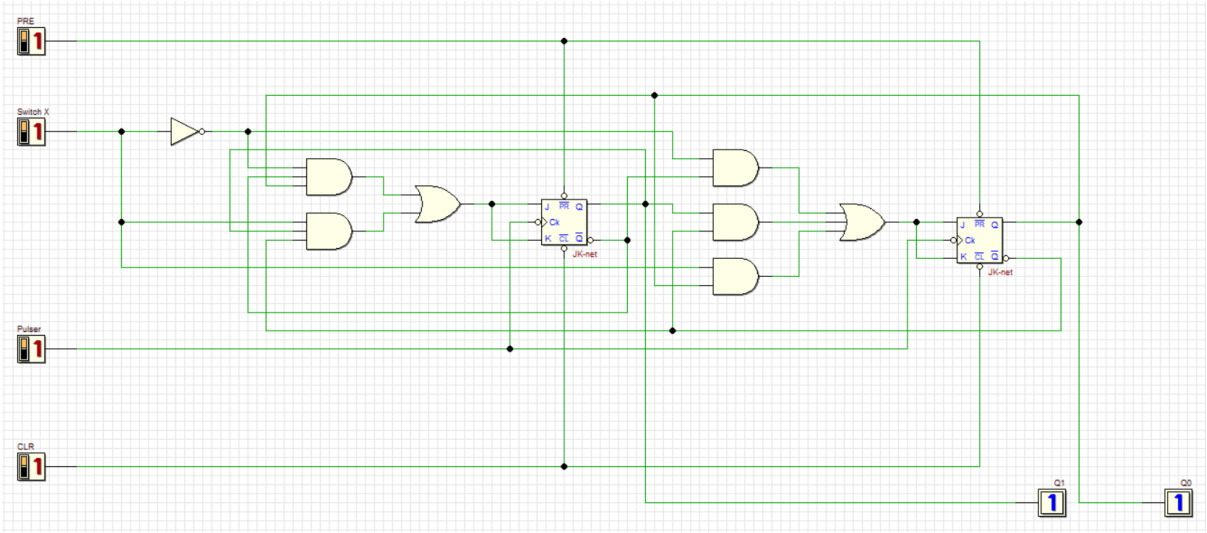
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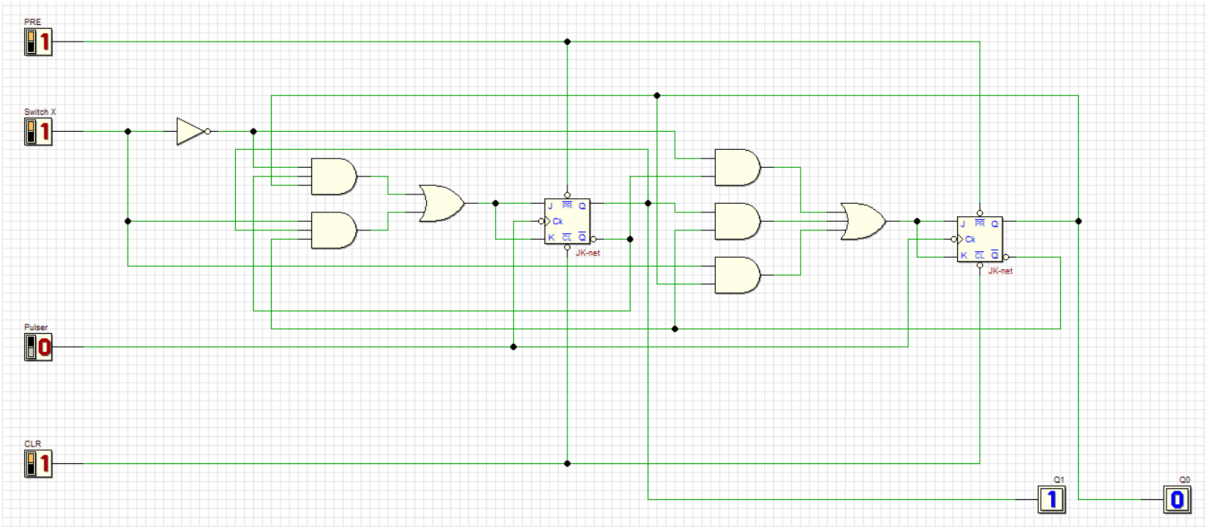
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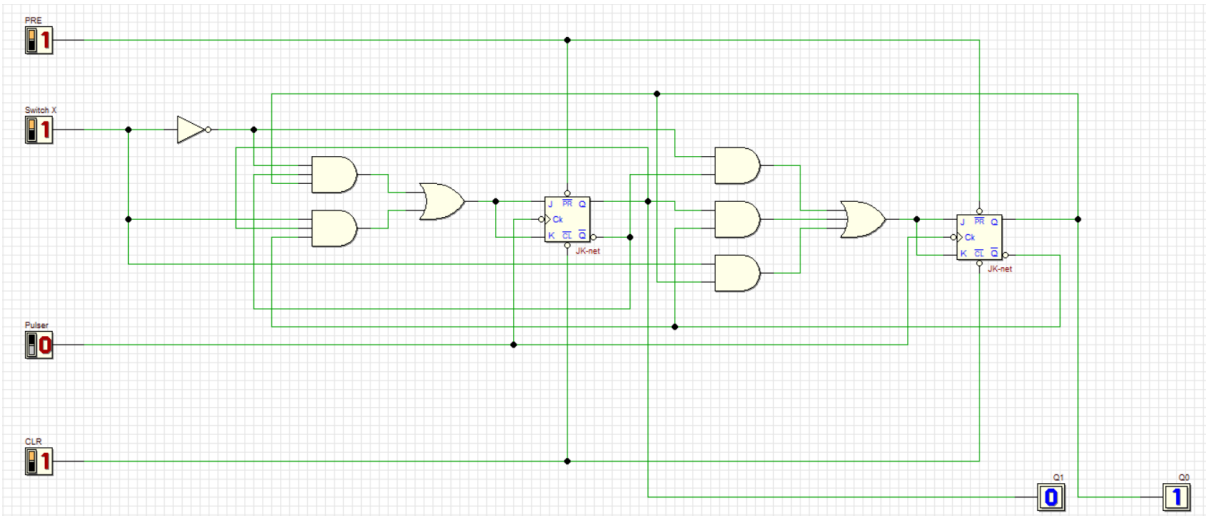
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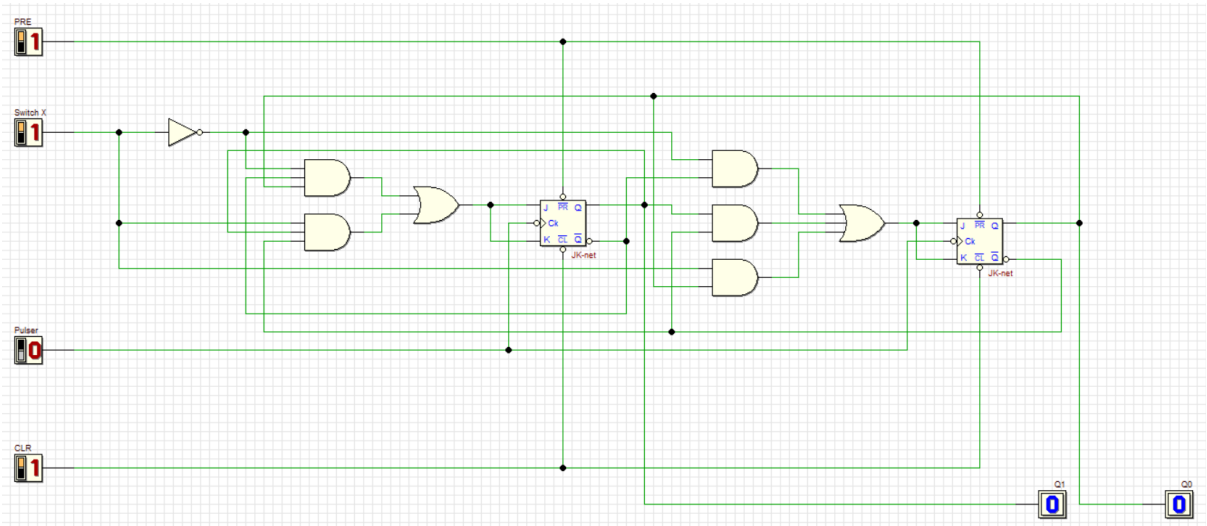
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JK-net
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Q0
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