D. Lab Activities

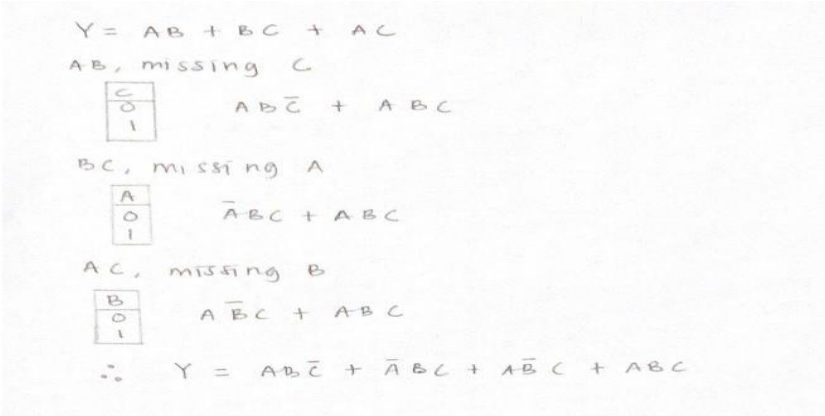
Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

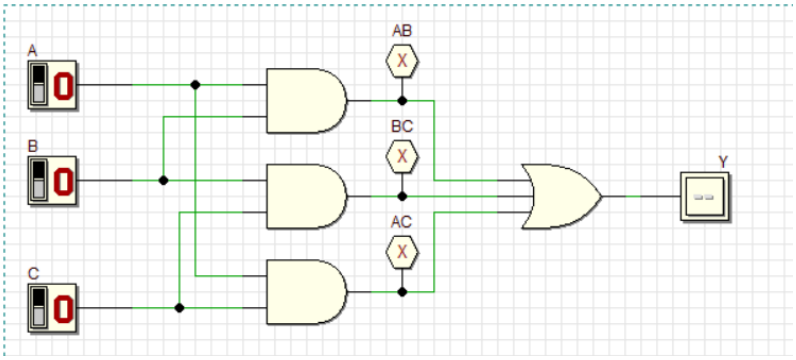
1. Convert the non-standard Boolean expression into standard form.



2. Based on standard form expression, complete the following truth table.

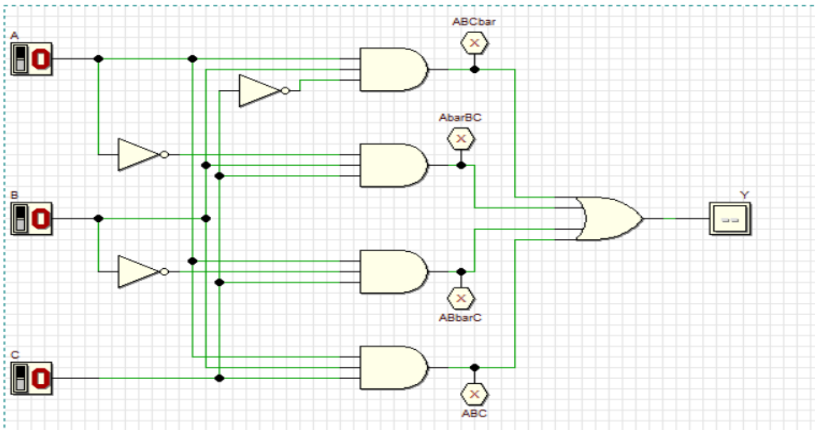
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. Using Deeds Simulator, draw the following circuits:
   a) Circuit (i) for non-standard form (based on given expression).



Circuit (i)

b) Circuit (ii) for standard form (from your answer in question 1).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Circuit (i)

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

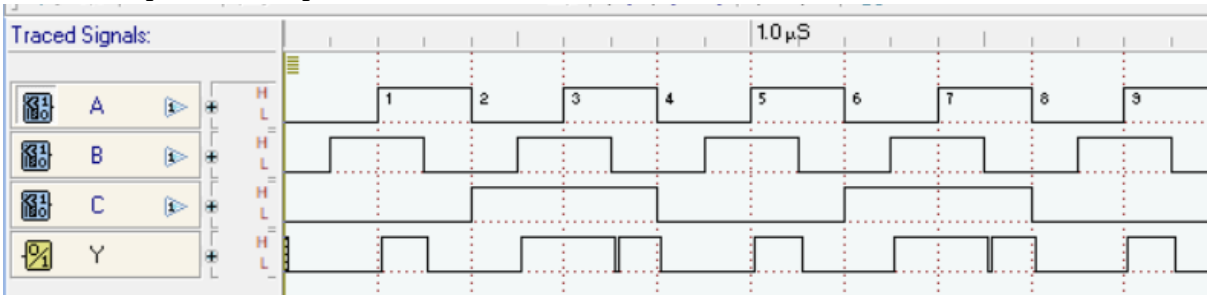
Circuit (ii)

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

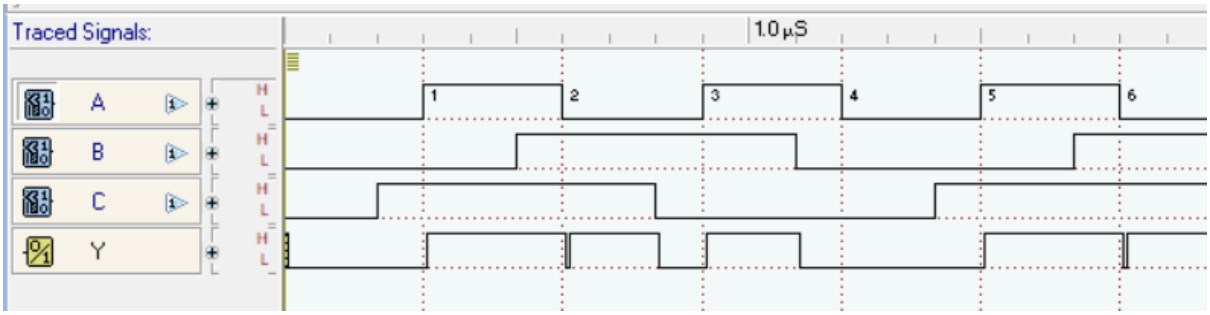
Compare the simulation result for these two truth tables. What is your conclusion?

- Both non-standard and standard forms produce the same outputs. Standardized form of Boolean expression does not change the outputs of the non-standard Boolean expression before.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



Example 1



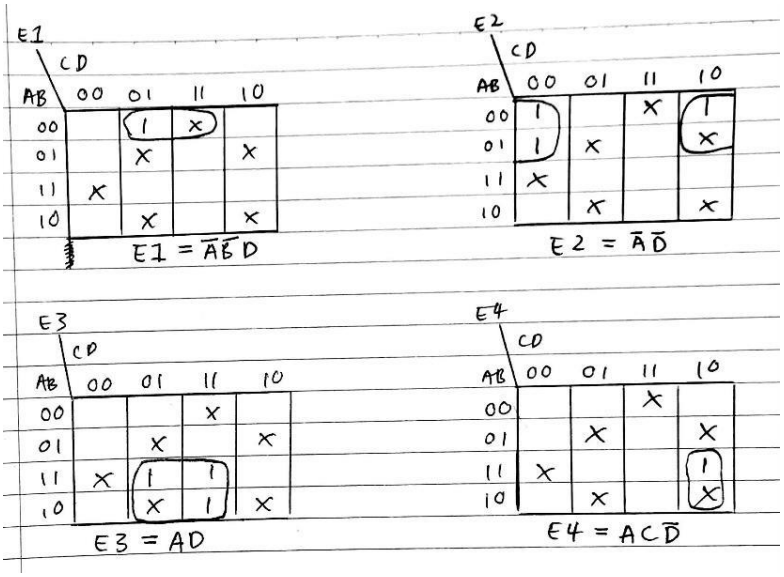
Example 2

Part 2

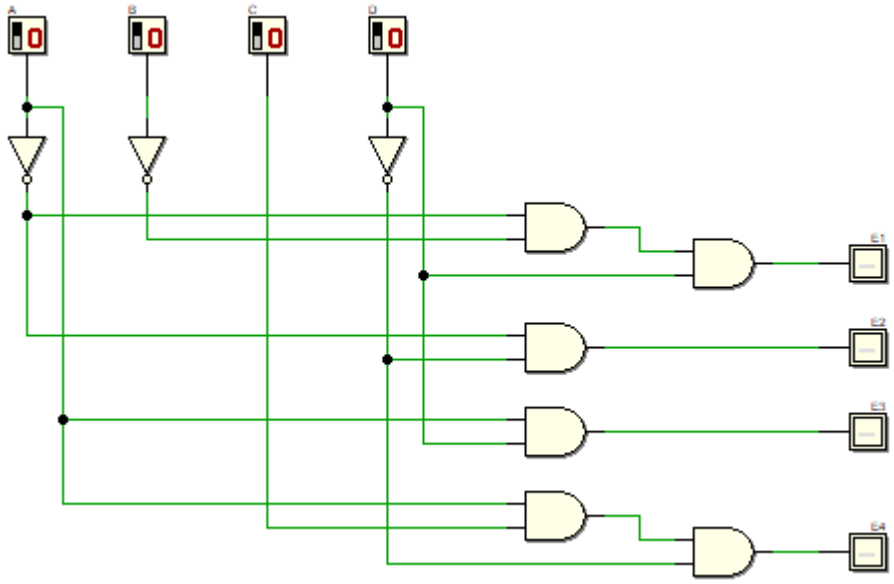
1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

INPUT				OUTPUT			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

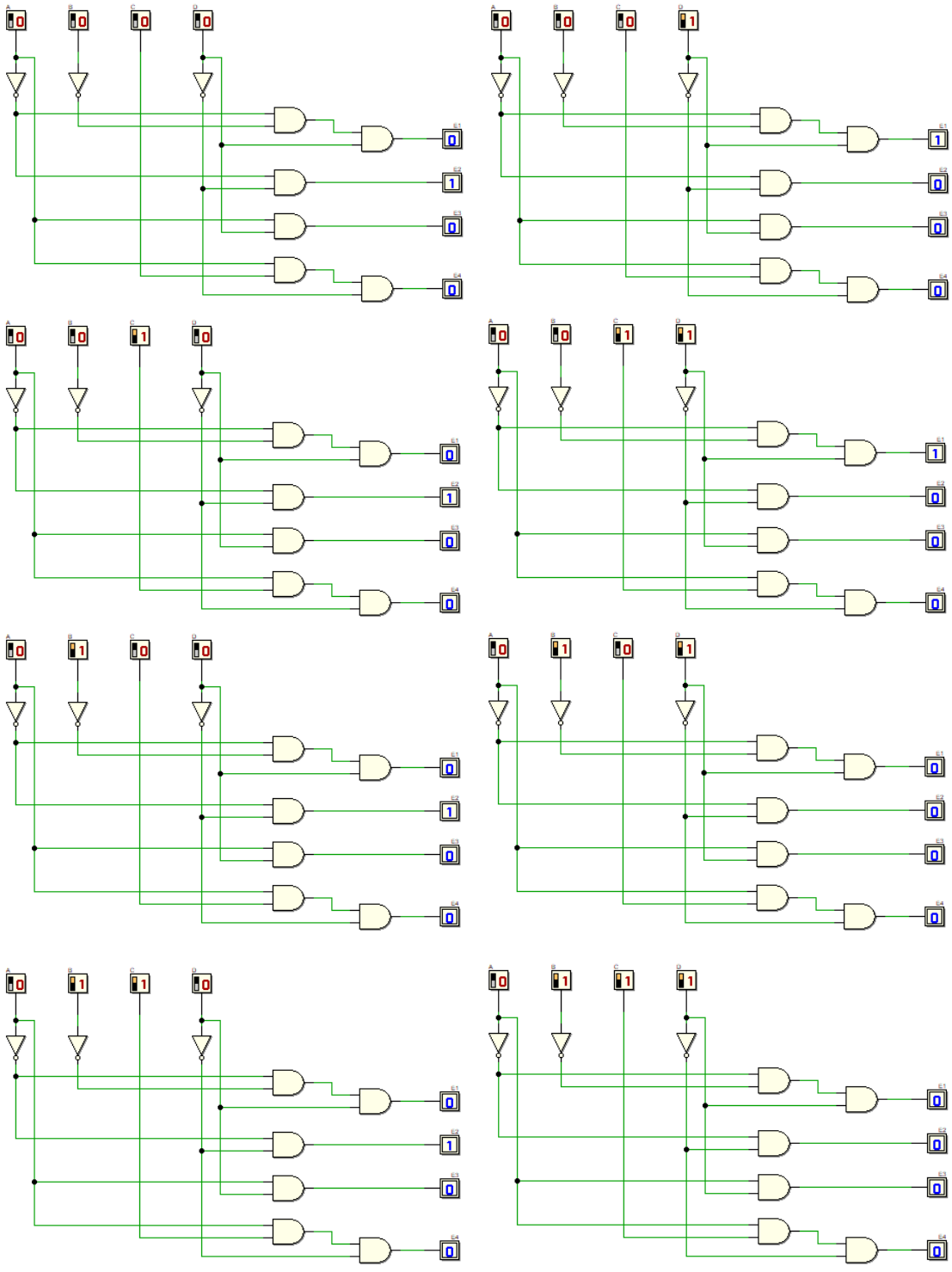
2. Using K-MAP, get minimized SOP Boolean Expressions for E1, E2, E3 and E4 circuits.

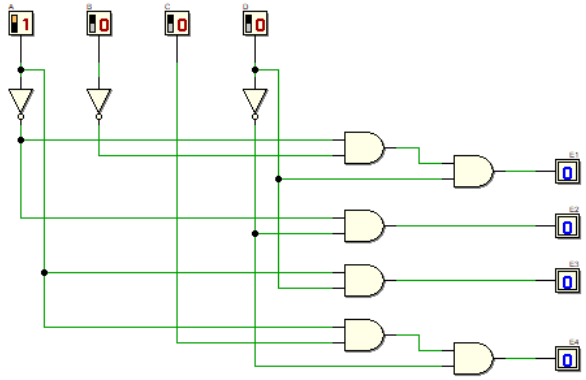
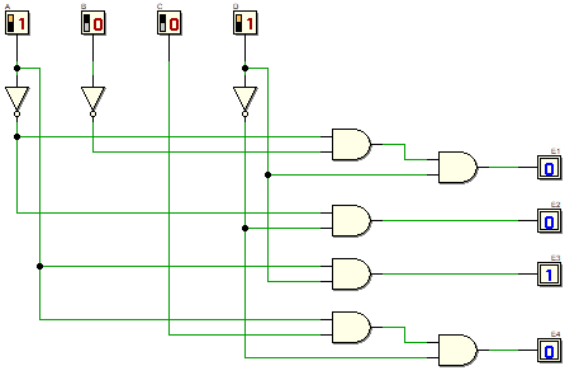
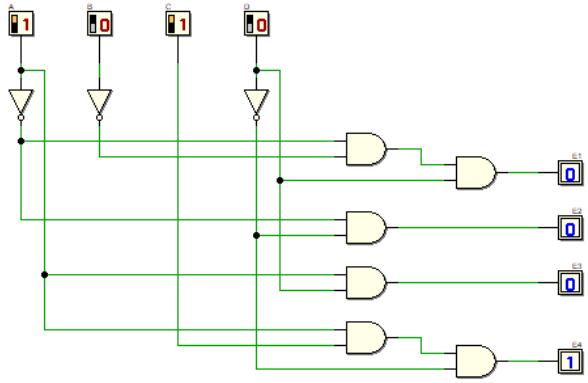
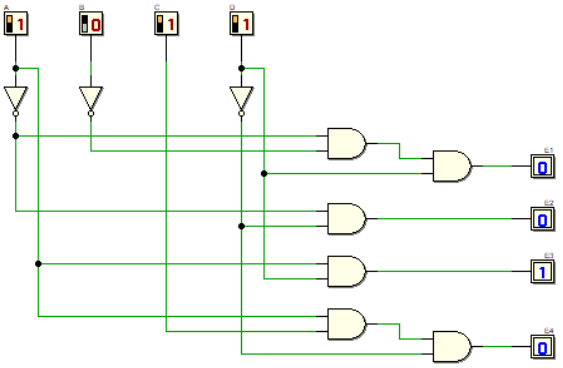
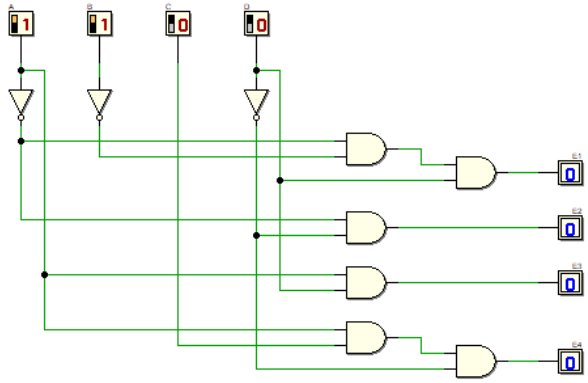
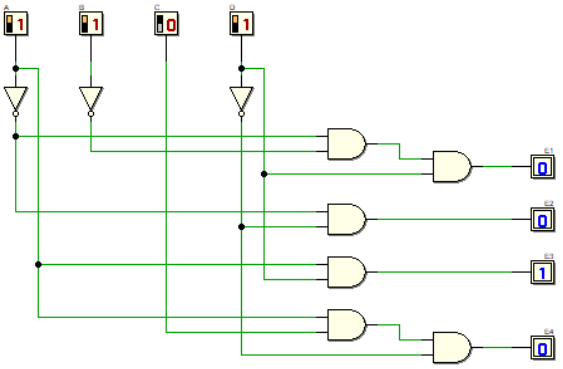
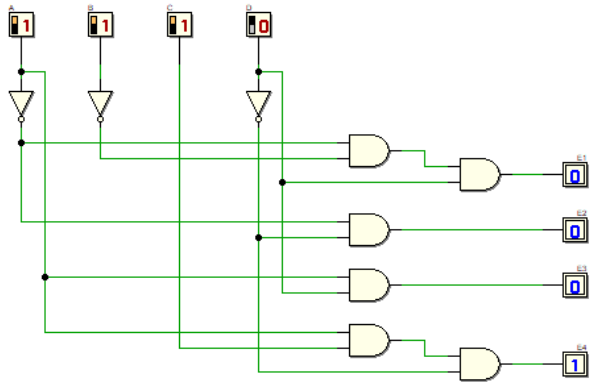
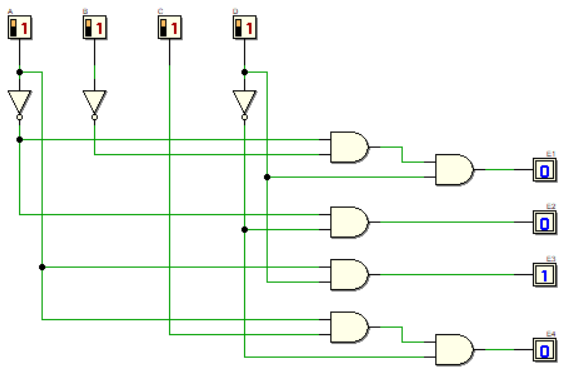


3. From the Boolean expression in step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):
   a) Update Truth Table 2 based on the simulation result.



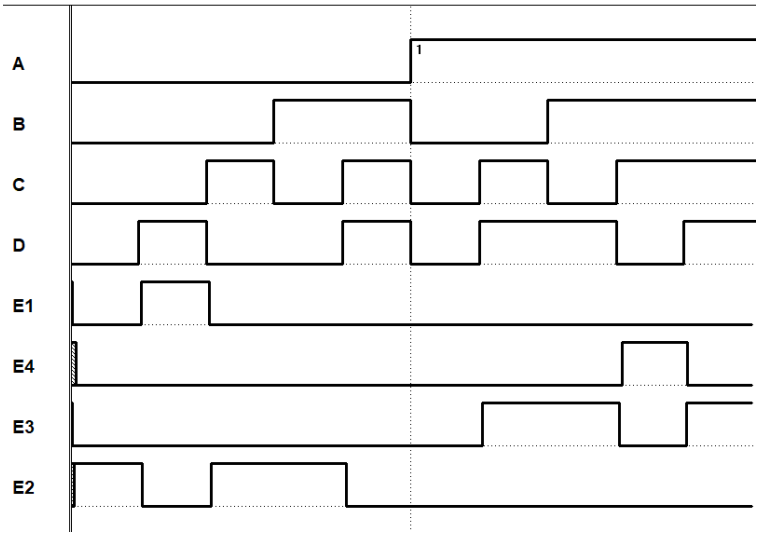









INPUT				OUTPUT			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X(1)	X(0)	X(0)	X(0)
0	1	0	0	0	1	0	0
0	1	0	1	X(0)	X(0)	X(0)	X(0)
0	1	1	0	X(0)	X(1)	X(0)	X(0)
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X(0)	X(0)	X(1)	X(0)
1	0	1	0	X(0)	X(0)	X(0)	X(1)
1	0	1	1	0	0	1	0
1	1	0	0	X(0)	X(0)	X(0)	X(0)
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

- Truth Table 2 and Truth Table 1 have the same value. X is don't care meanwhile the value in the bracket is the output that we got from Deeds simulator.

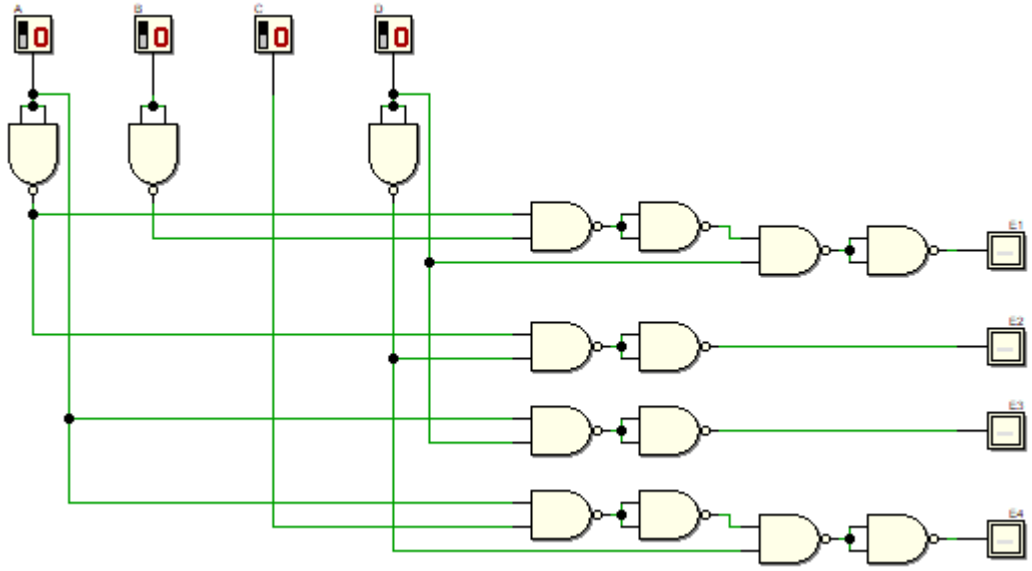
b) Timing Diagram



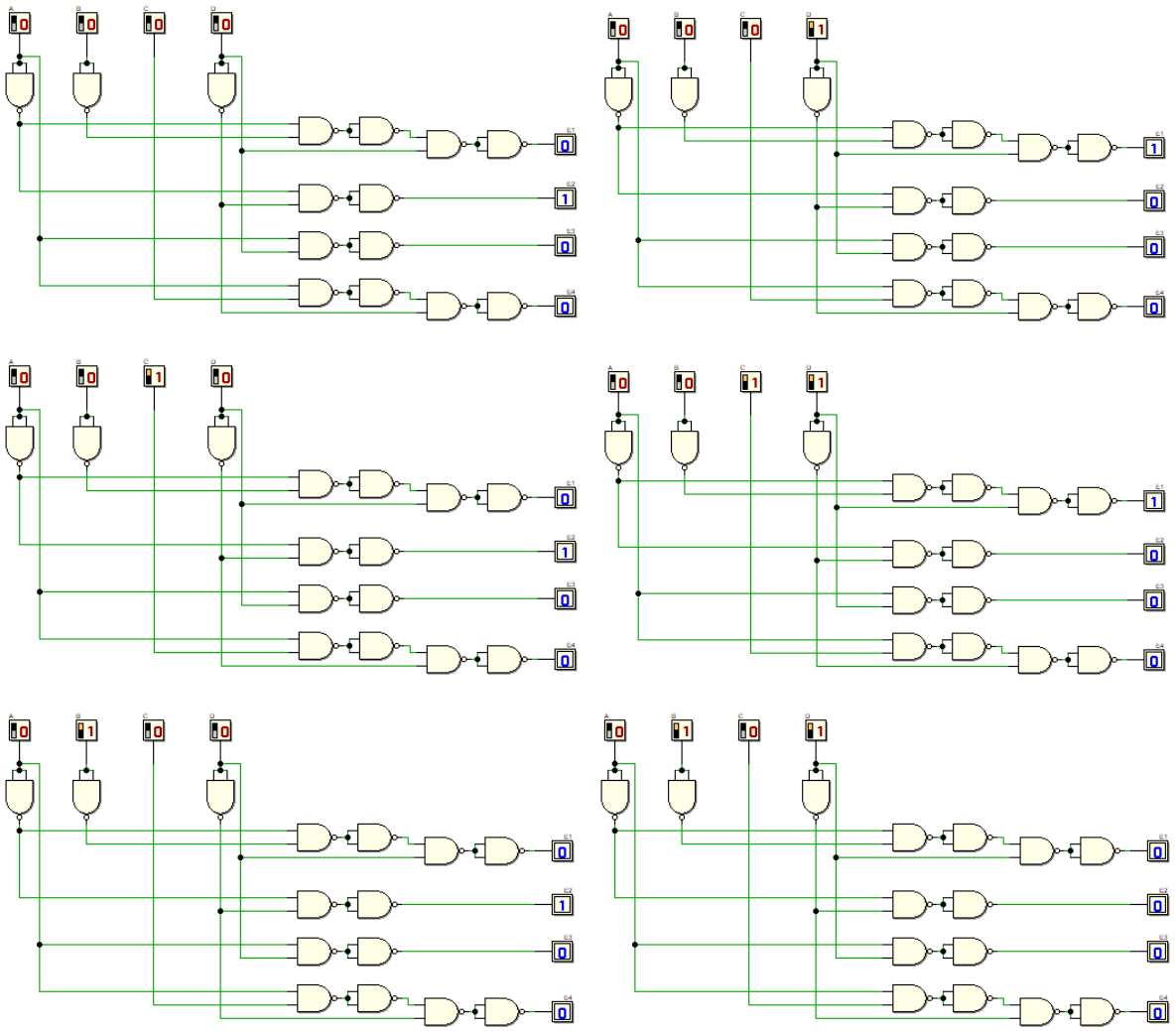
Explain some analysis values based on your timing diagram:

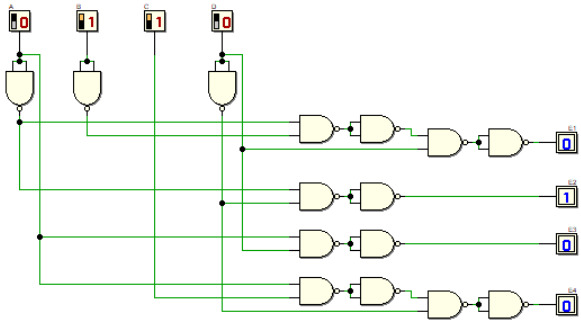
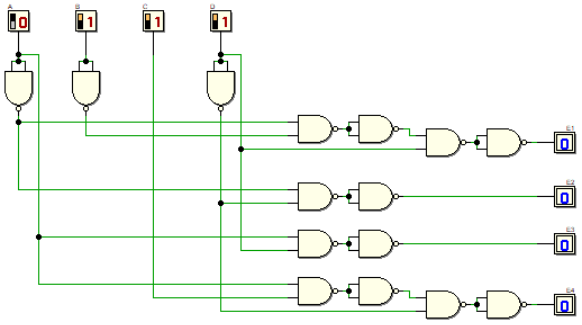
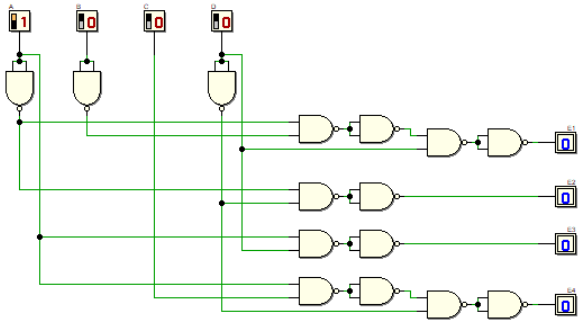
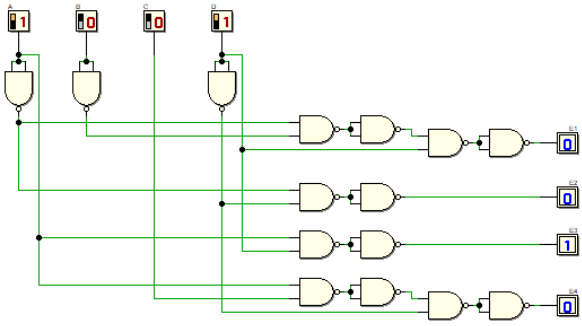
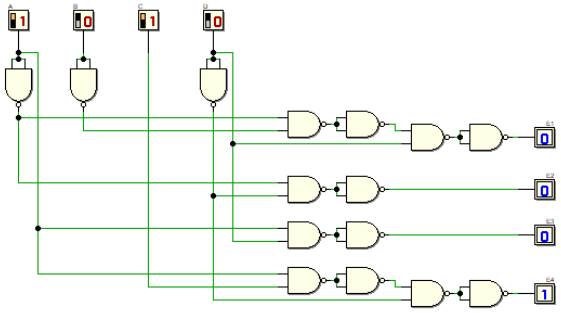
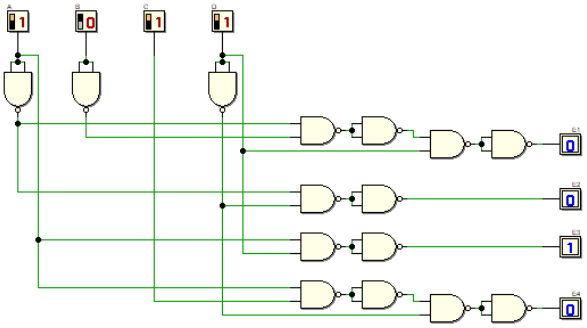
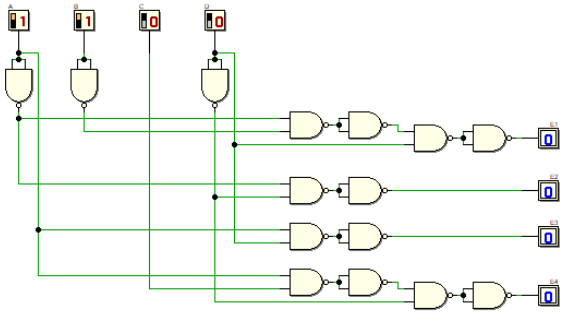
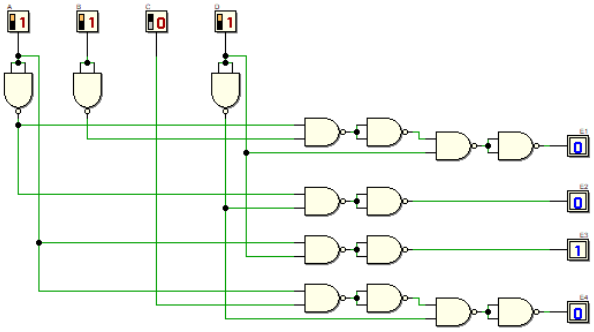
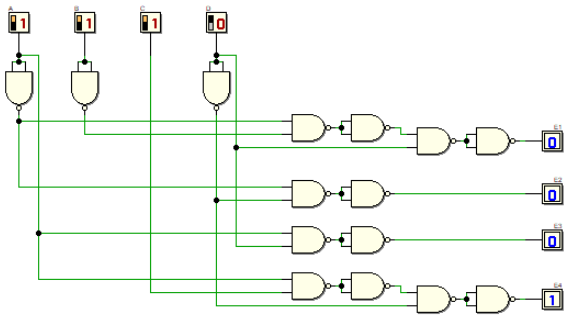
- All input produce only one output.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only, use Deeds Simulator.



6. Simulate the Deeds circuit in step (5):
   a) Update Truth Table 3 based on the simulation result.



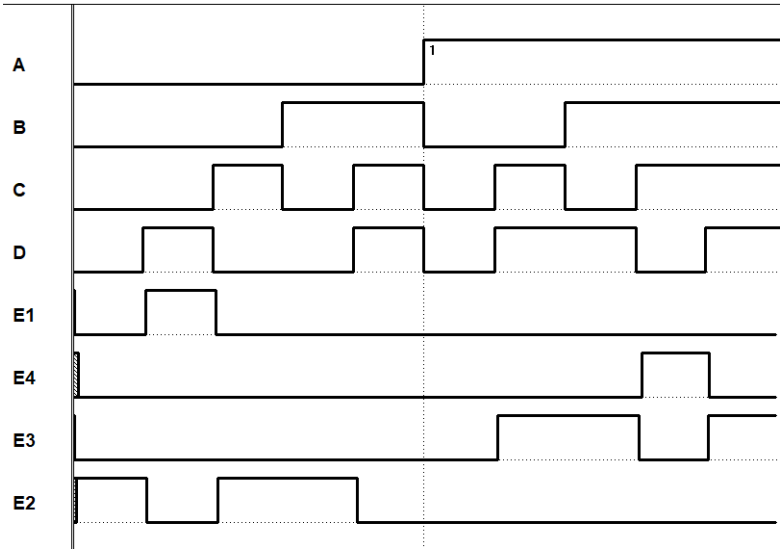










INPUT				OUTPUT			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X(1)	X(0)	X(0)	X(0)
0	1	0	0	0	1	0	0
0	1	0	1	X(0)	X(0)	X(0)	X(0)
0	1	1	0	X(0)	X(1)	X(0)	X(0)
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X(0)	X(0)	X(1)	X(0)
1	0	1	0	X(0)	X(0)	X(0)	X(1)
1	0	1	1	0	0	1	0
1	1	0	0	X(0)	X(0)	X(0)	X(0)
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

- Truth Table 3 and Truth Table 2 have the same value even though circuit in step (2) uses basic gate while circuit in step (3) uses NAND gates only. X is don't care meanwhile the value in the bracket is the output that we got from Deeds simulator.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

- All input produce only one output.