



**School of Computing
Faculty of Engineering
UNIVERSITI TEKNOLOGI MALAYSIA**

SUBJECT : SECR1013 DIGITAL LOGIC

SESSION/SEM : Semester 1
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LAB 3 : SYNCHRONOUS DIGITAL COUNTER

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NAME :

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DATE :

Lab #3

Identifying the Properties of a Synchronous Counter

A. Aims

- 1) Expose the student with experience on constructing synchronous counter circuit using Flip-Flop IC, Basic Gate ICs, Breadboard and ETS-5000 Digital Kit.
- 2) Promote critical thinking among students by analysing the given circuit and identifying the behaviour of the digital circuit.

B. Objectives

The objectives of this lab activity are to:

- 1) Implement a synchronous counter circuit into physical circuit using Breadboard, Flip-Flops, Basic Gates and Switches.
- 2) Completing the next-state table of the counter circuit.
- 3) Sketch the state diagram of the counter circuit.
- 4) Identify the properties of the counter.

C. Materials And Equipment

Materials and equipment required for this lab are as follows:

Item Name	Number of Item
1. Breadboard	1
2. 7408 Quad 2-Input AND	1
3. 7404 Hex Inverter	1
4. 7432 Quad 2-input OR	1
5. 7476 Dual J-K Flip Flop	1
6. ETS-5000 Digital Kit	1

D. Preliminary Works

- 1) Determine the logic level for each input combinations in Table 1 so that the desired result can be realized.

Table 1

Desired Result	<i>PRE</i>	<i>CLR</i>	J	K	CLK	Q
Set initial value Q = 1	0	1	X	X	--	1
Output Q stays the same	1	1	0	0	↓	1
Output Q become 0, no change in asynchronous input	1	1	0	1	↓	0
Output Q is not the previous Q	1	1	1	1	↓	1
RESET Q	1	1	0	1	↓	0
SET Q	1	1	1	0	↓	1

- 2) Answer all questions.

- a) Which state that JK flip-flop has, but not on SR flip-flop.

Input 1 1, Toggle state

- b) Identify whether the JK flip flop in 7476, is a positive-edge triggered or negative-edge triggered flip flop.

Negative-edge triggered flip flop

E. Lab Activities

1) You are given a counter circuit as shown in Figure 4.

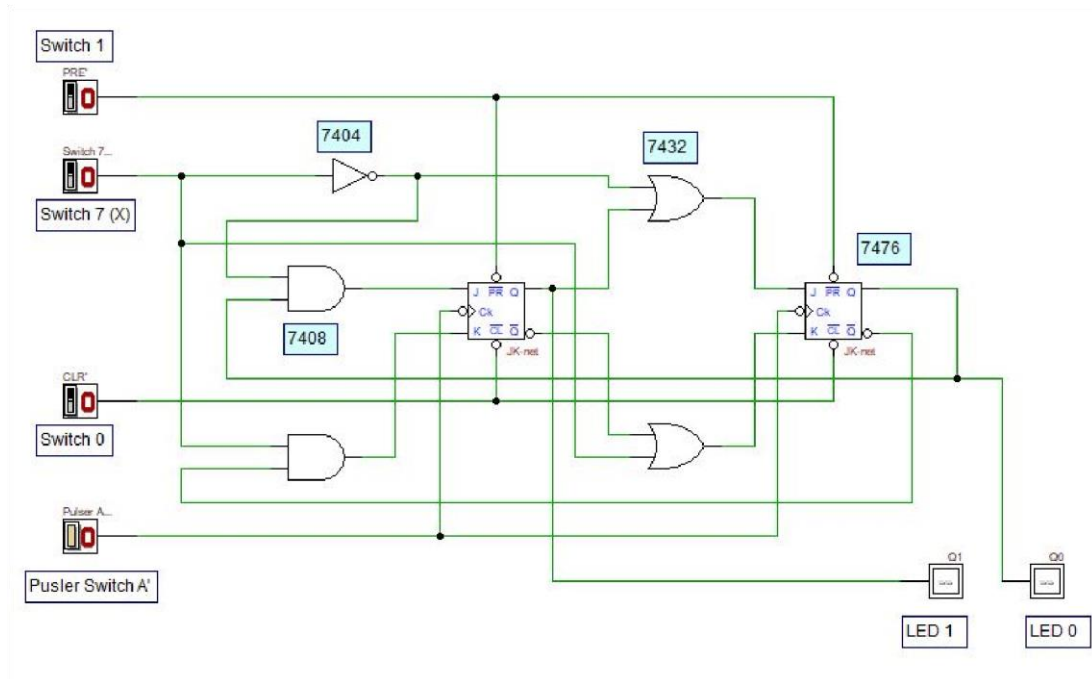


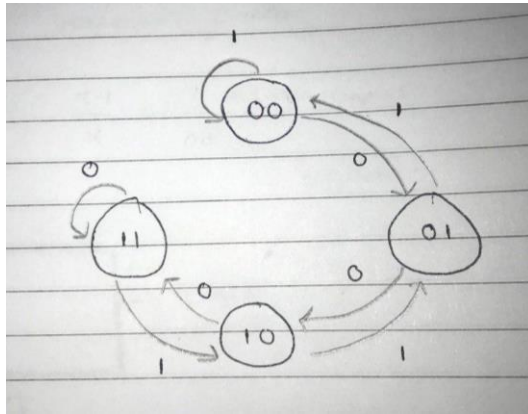
Figure 4: A Synchronous Counter Circuit

- By using all materials and equipment's listed in section C, construct the physical circuit of Figure 4. (Make sure all ICs are connected to V_{cc} and GND).
- Investigate the behaviour of the counter by observing the next state of the counter for all combination of *Present State* and X values. Complete the *Next State* table of the counter in Table 2. Ensure the Switch 0 is in HIGH state. (0=LOW, 1=HIGH)

Table 2

Switch 7	Present State		Next State	
X	Q1 LED 1	Q0 LED 0	Q1 LED 1	Q0 LED 0
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

- 4) By referring to the *Next-State* in Table 2, sketch the state diagram of the counter.



- 5) By referring to the *Next-State* in Table 2 and the state diagram in (4), answer all questions.

- a) What is the main indicator to decide that the counter is a synchronous counter?

The clock to both flip-flops is common.

- b) How many states are available for the counter and what are they?

4 states. 00, 01, 10, 11

- c) What is the function of Switch 7 (X) in the circuit?

The count direction is controlled by an input X, if $X=1$, the counter will count down, if $X=0$, the counter will count up.

- d) What is the function of Switch 0 and Switch 1 in the circuit?

These inputs are called the preset (PRE) and clear (CLR). The preset input drives the flip-flop to a set state while the clear input drives it to a reset state.

- e) Is the counter a saturated counter or recycle counter?

saturated

- 6) Referring to state diagram in 4, draw and built a synchronous counter using D flip-flop.

- a) Built the next state and transition table using the header in Table 3

Input X	Present State		Next State		D FF Transition	
	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

- b) Get the optimized Boolean expression.

Handwritten Karnaugh maps and Boolean expressions for D1 and D0.

D1 Karnaugh Map:

		$Q_1 Q_0$			
$X \backslash$		00	01	11	10
0		0	1	1	1
1		0	0	1	0

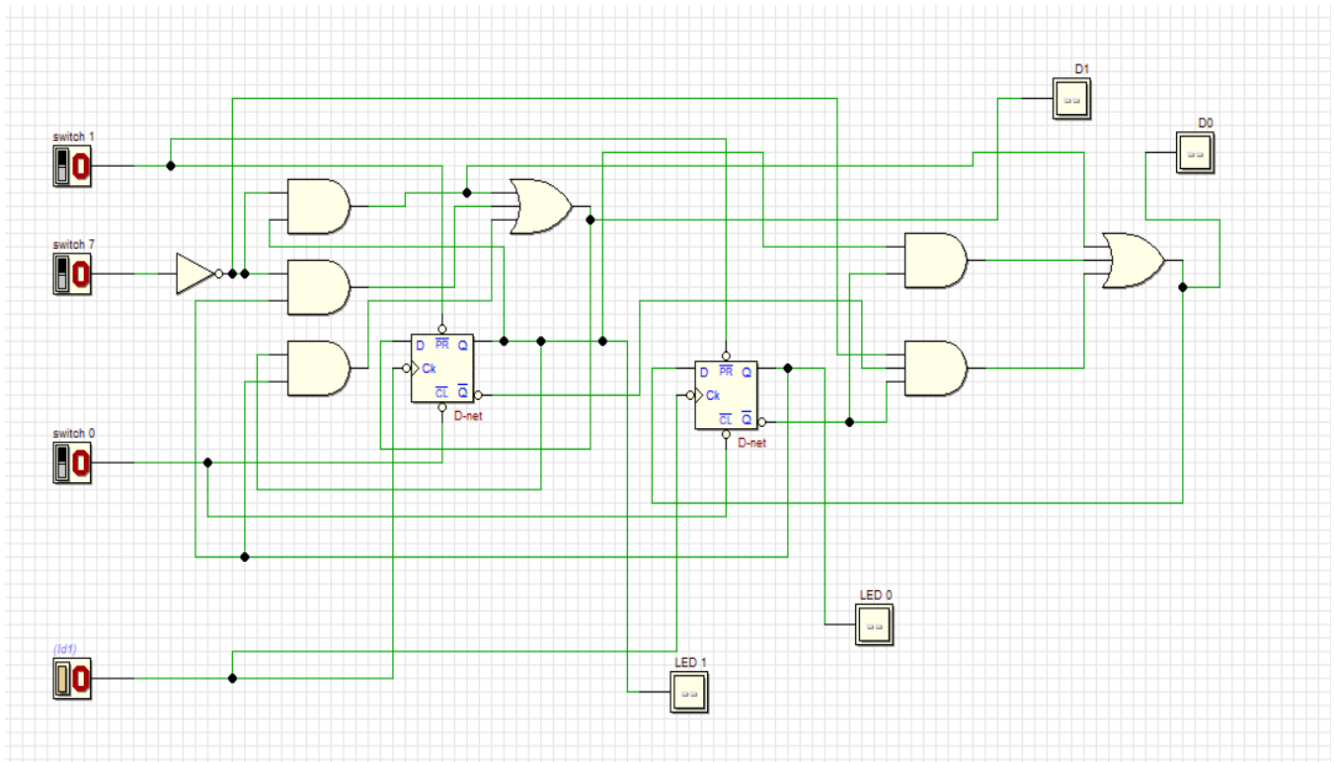
$$D1 = \bar{X}Q_0 + Q_1Q_0 + \bar{X}Q_1$$

D0 Karnaugh Map:

		$Q_1 Q_0$			
$X \backslash$		00	01	11	10
0		1	0	1	1
1		0	0	0	1

$$D_0 = \bar{X}\bar{Q}_1\bar{Q}_0 + \bar{X}Q_1 + Q_1Q_0$$

- c) Draw the complete final circuit design in Deeds.



- d) Simulate the circuit to prove that your Table 3 is correct.

Input X	Present State		Next State		D FF Transition	
	Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

Both outputs are the same.

- 7) Repeat steps in Q (6) using T flip-flop.

- a) Built the next state and transition table

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

- b) Get the optimized Boolean expression.

The image shows handwritten Karnaugh maps for the transition functions T₁ and T₀. For T₁, the map has 1s at (X=0, Q1=0, Q0=1) and (X=1, Q1=1, Q0=0), leading to the expression $T_1 = \bar{X}\bar{Q}_1Q_0 + XQ_1\bar{Q}_0$. For T₀, the map has 1s at (X=0, Q1=0, Q0=0), (X=0, Q1=1, Q0=1), (X=1, Q1=0, Q0=1), and (X=1, Q1=1, Q0=1), leading to the expression $T_0 = \bar{X}\bar{Q}_1 + XQ_0 + Q_1Q_0$.

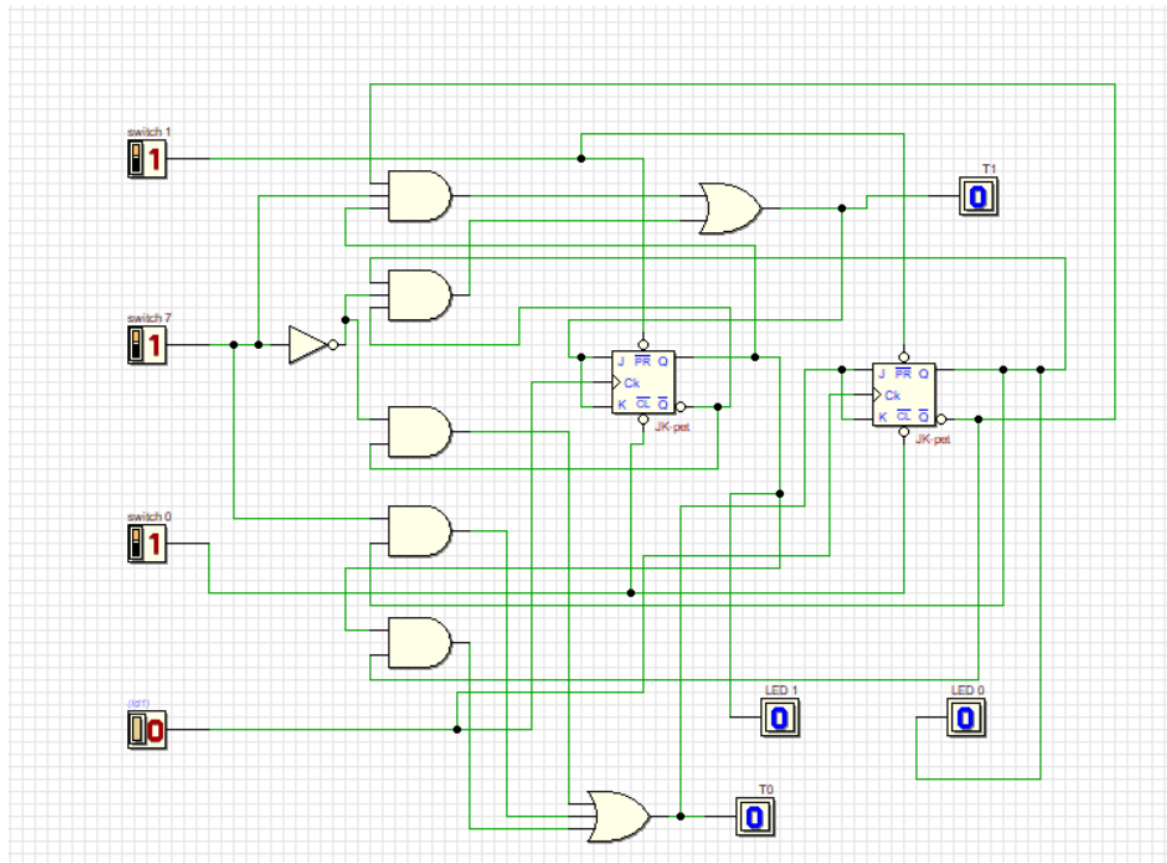
X \ Q ₁ Q ₀	00	01	11	10
0	0	1	0	0
1	0	0	0	1

$$T_1 = \bar{X}\bar{Q}_1Q_0 + XQ_1\bar{Q}_0$$

X \ Q ₁ Q ₀	00	01	11	10
0	1	1	0	1
1	0	1	1	1

$$T_0 = \bar{X}\bar{Q}_1 + XQ_0 + Q_1Q_0$$

- c) Draw the complete final circuit design in Deeds.



d) Simulate the circuit to prove that your Table 3 is correct.

Input X	Present State		Next State		T FF Transition	
	Q1	Q0	Q1+	Q0+	T1	T0
0	0	0	0	1	0	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	0	1
1	1	0	0	1	1	1
1	1	1	1	0	0	1

Both outputs are the same.