**Department of Computer Science**
**Faculty of Computing**
**UNIVERSITI TEKNOLOGI MALAYSIA**

| | | |
|---|---|---|
| SUBJECT | : | SCSR1013 DIGITAL LOGIC |
| SESSION/SEM | : | 1/2020/2021 |
| **LAB 2** | : | **COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION** |
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| DATE | : | 14/1/2021 |

REMARKS :

**MARKS:**

**D. Lab Activities**

**Part 1**

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

| C | A | B |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 1 | 1 |

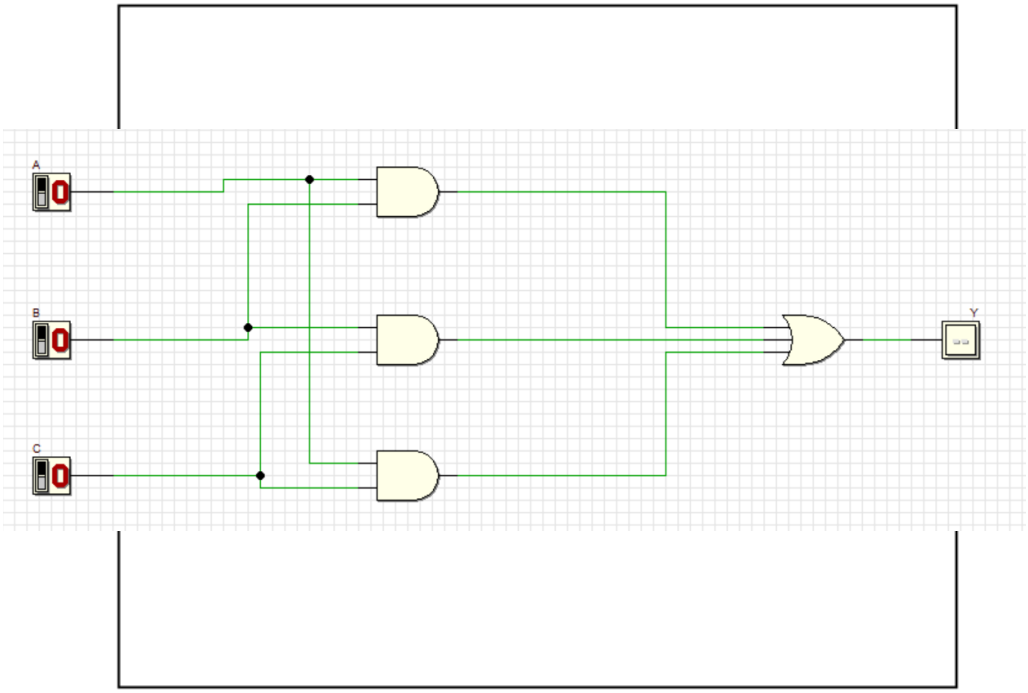
$Y = AB\bar{C} + ABC + \bar{A}BC + A\bar{B}C$

2. Based on standard form expression, complete the following truth table.

| INPUT | | | OUTPUT |
|---|---|---|---|
| **A** | **B** | **C** | **Y** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

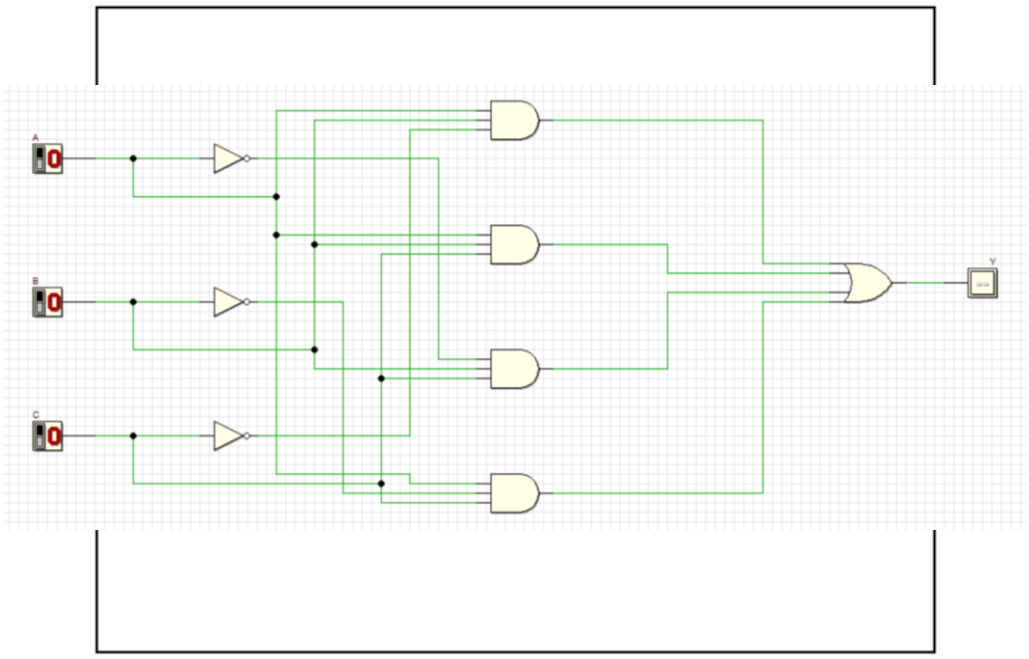
3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



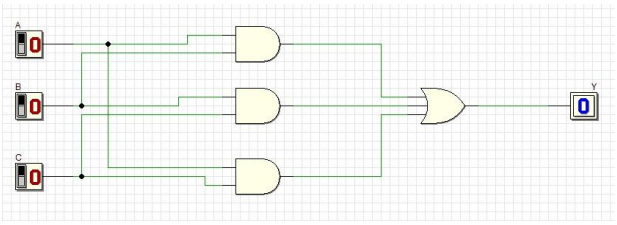

Circuit (i)

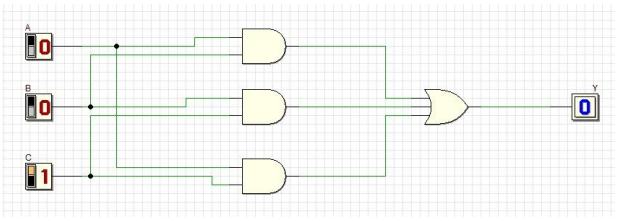
b) Circuit (ii) for standard form (from your answer in question (1)).

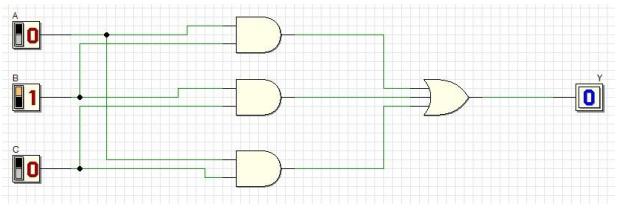


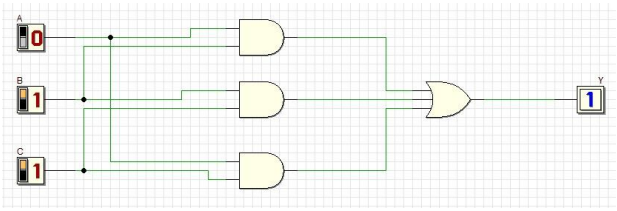

Circuit (ii)

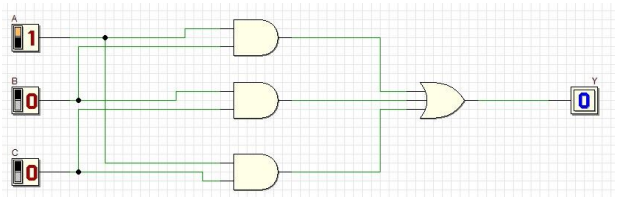
## Non-standard SOP circuit

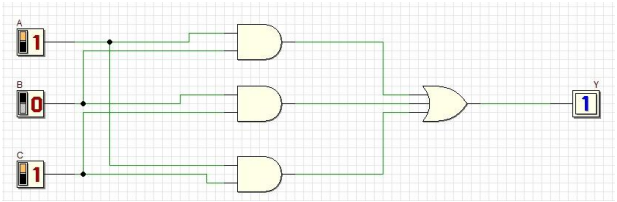


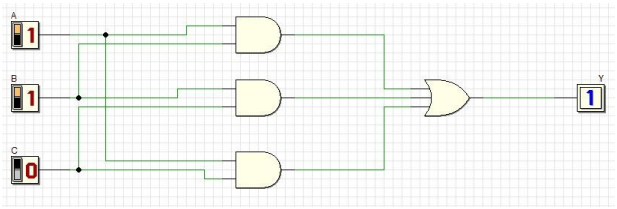



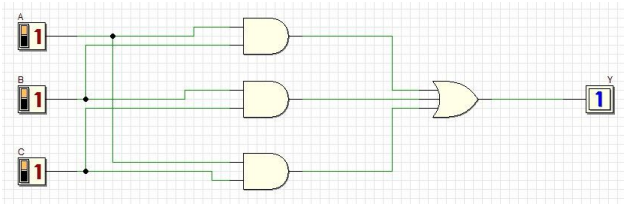



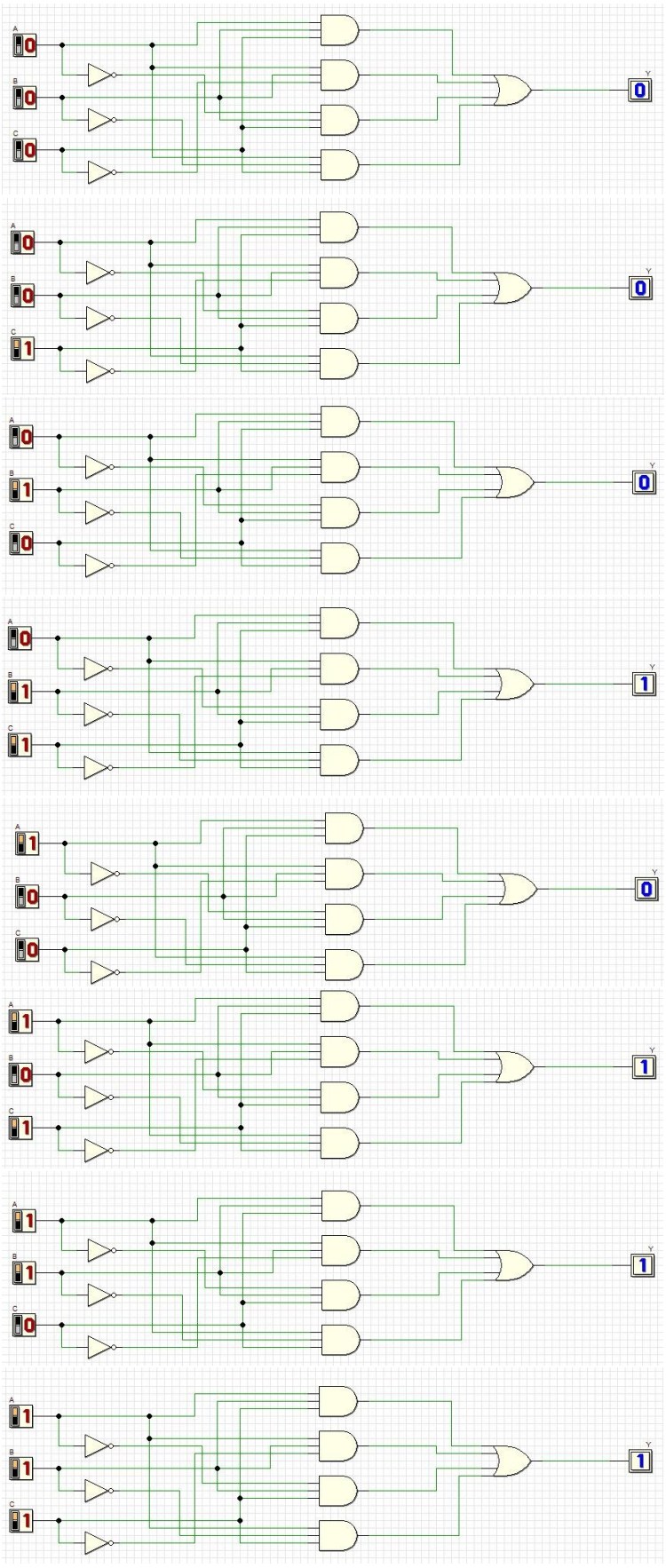



## Standard SOP circuit



4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

| INPUT | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

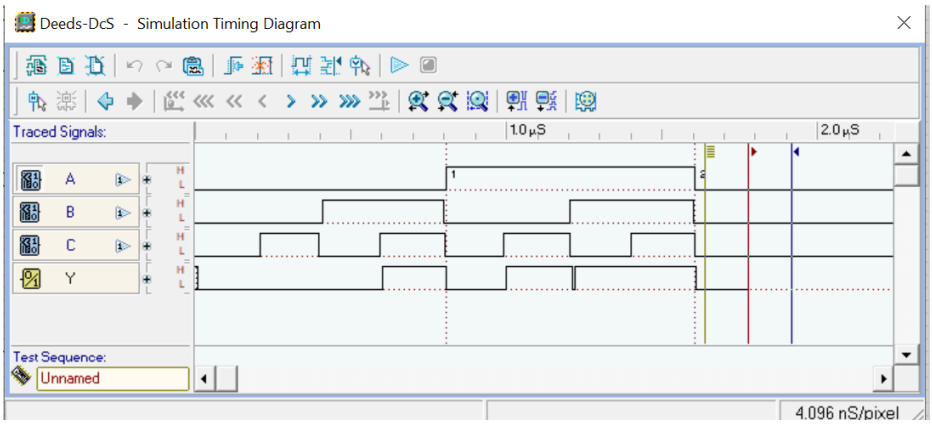
Circuit (ii)

| INPUT | | | OUTPUT |
|---|---|---|---|
| A | B | C | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Conclusion:

Standard SOP form is all variables appear in each product term of expression. It will produce the same output as nonstandard form of SOP. This is because nonstandard form of SOP is the simplification of standard SOP form.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.




Output Y is high when one of the inputs is low or all the input is high. Output Y is low when all the input is low or one of the inputs is high.

**Experimental Steps**

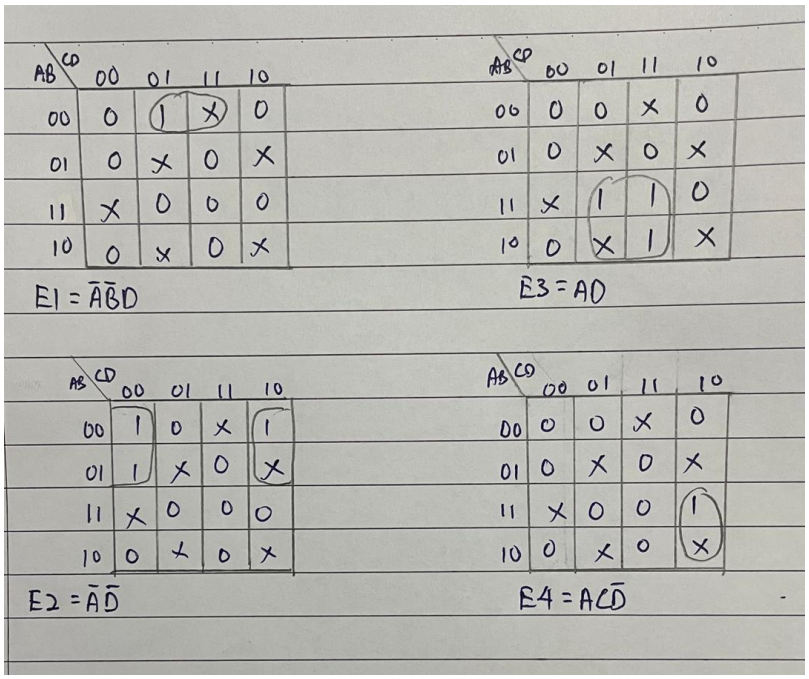
1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

**Truth Table 1**

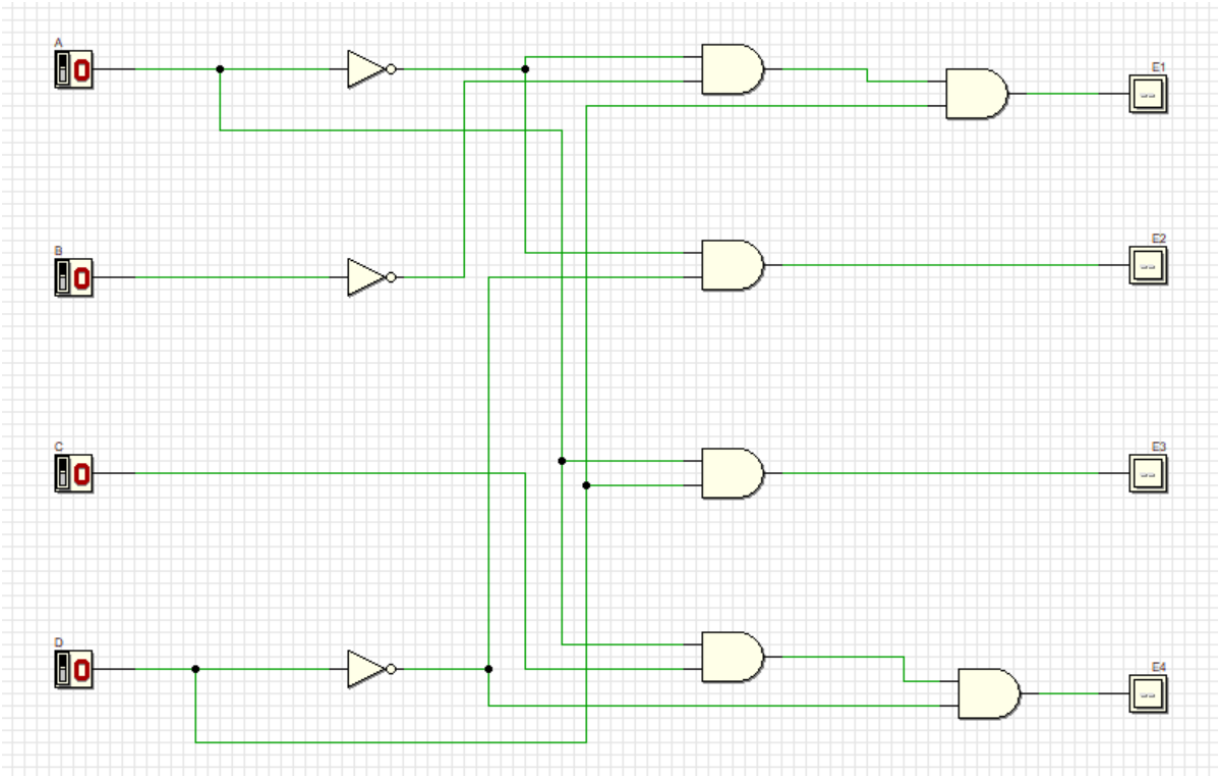
0 is even, A = positive / negative, where 0 = positive, 1 = negative

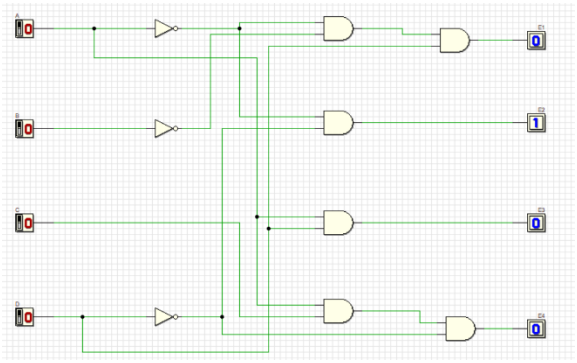
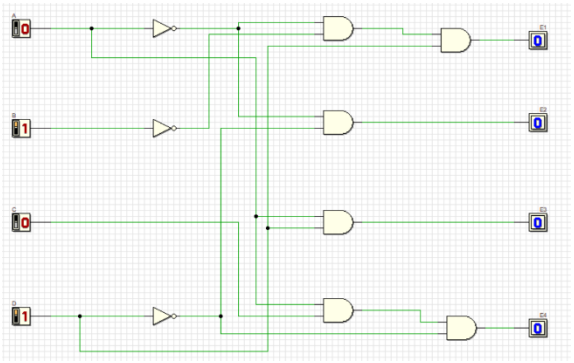
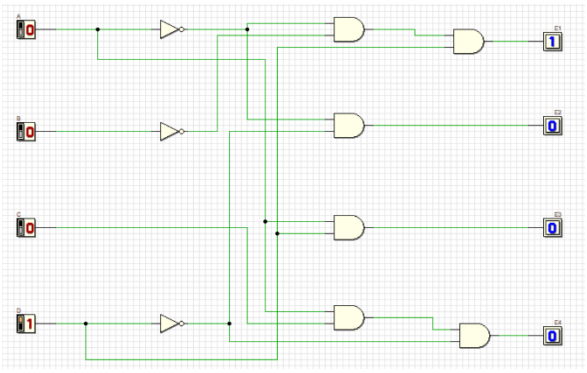
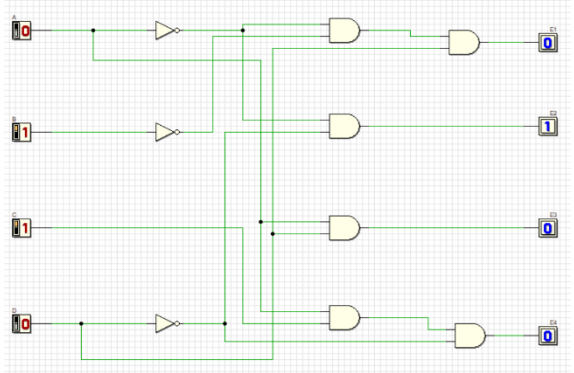
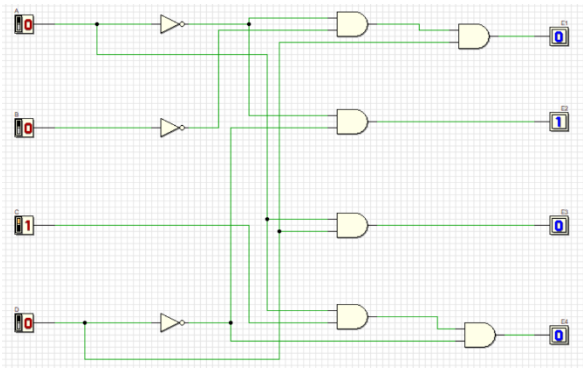
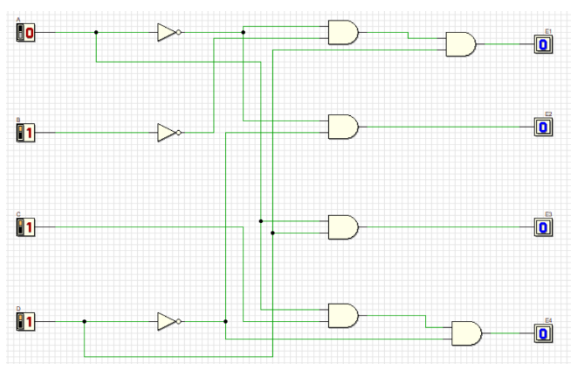
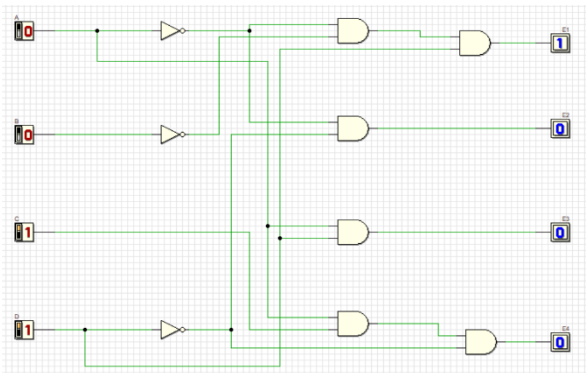
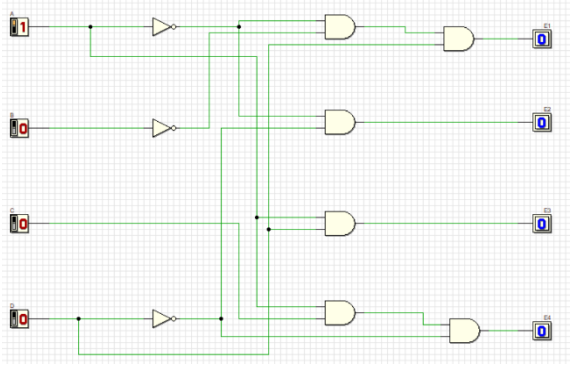
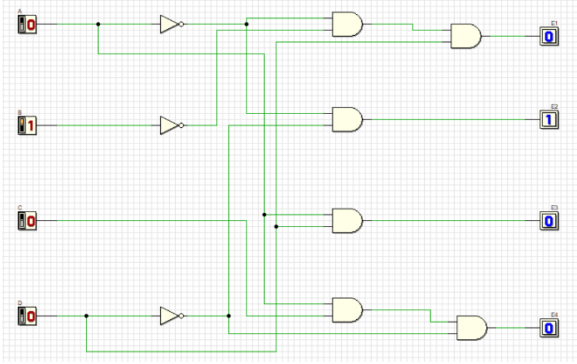
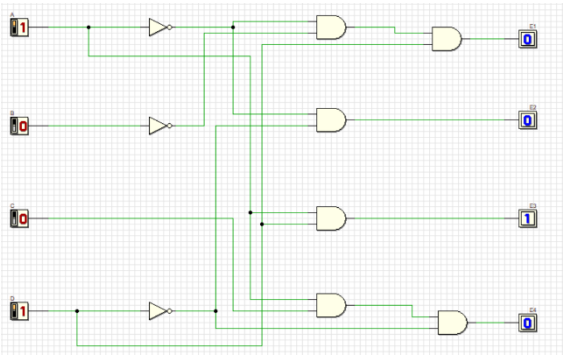
| | Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | E1 | E2 | E3 | E4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | X | X | X | X |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 | X | X | X | X |
| 6 | 0 | 1 | 1 | 0 | X | X | X | X |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| -8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -7 | 1 | 0 | 0 | 1 | X | X | X | X |
| -6 | 1 | 0 | 1 | 0 | X | X | X | X |
| -5 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| -4 | 1 | 1 | 0 | 0 | X | X | X | X |
| -3 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| -2 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| -1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

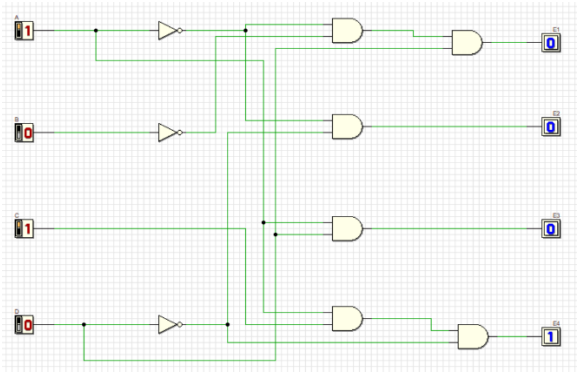
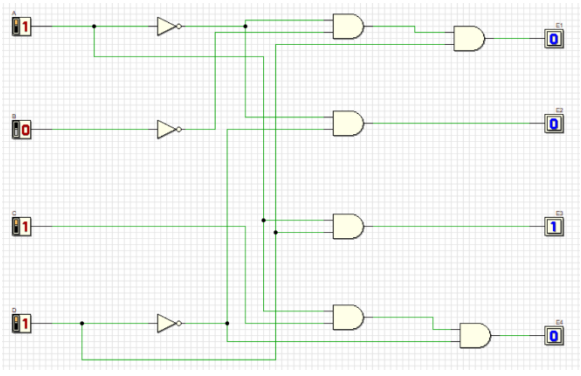
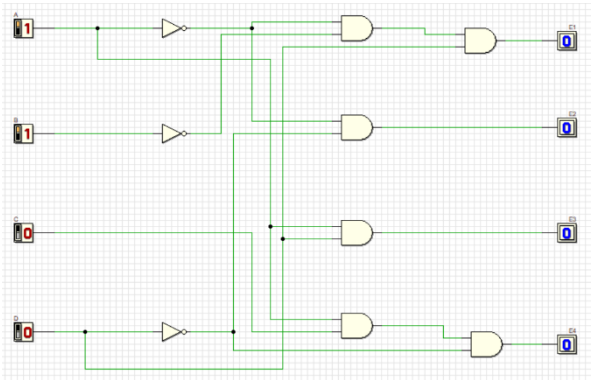
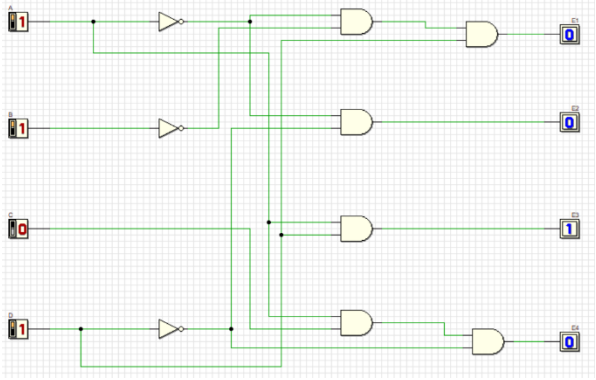
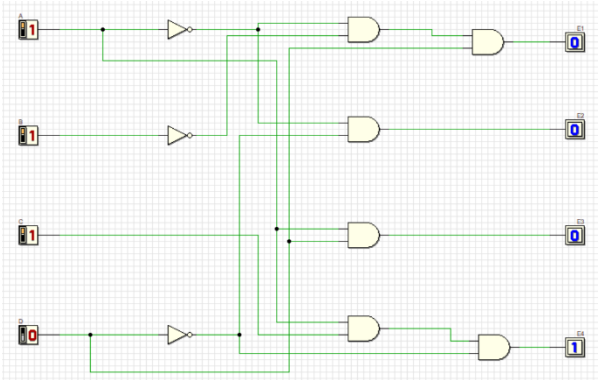
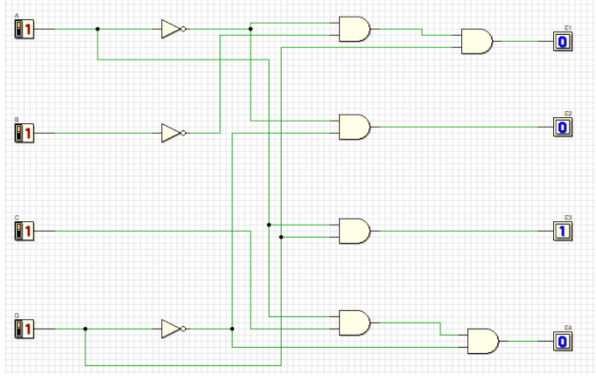
2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.



3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

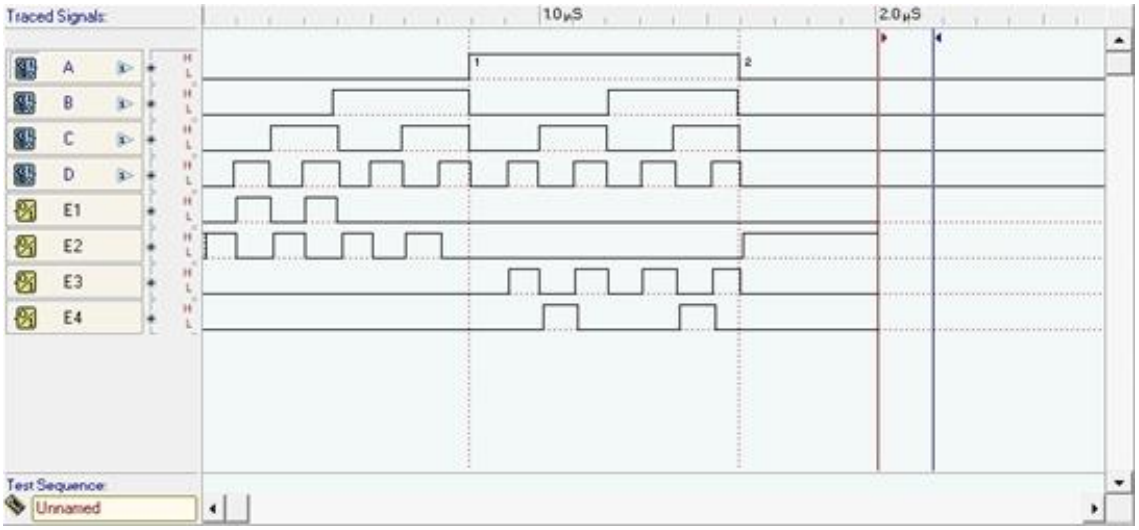
**Truth Table 2**

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **E1** | **E2** | **E3** | **E4** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

The output results in Truth Table 2 with Truth Table 1 is the same. This is because X is don't care which can be value 1 or 0. So in the Truth Table 2 the input same with Truth Table 1 that is don't care condition we also can ignore it.

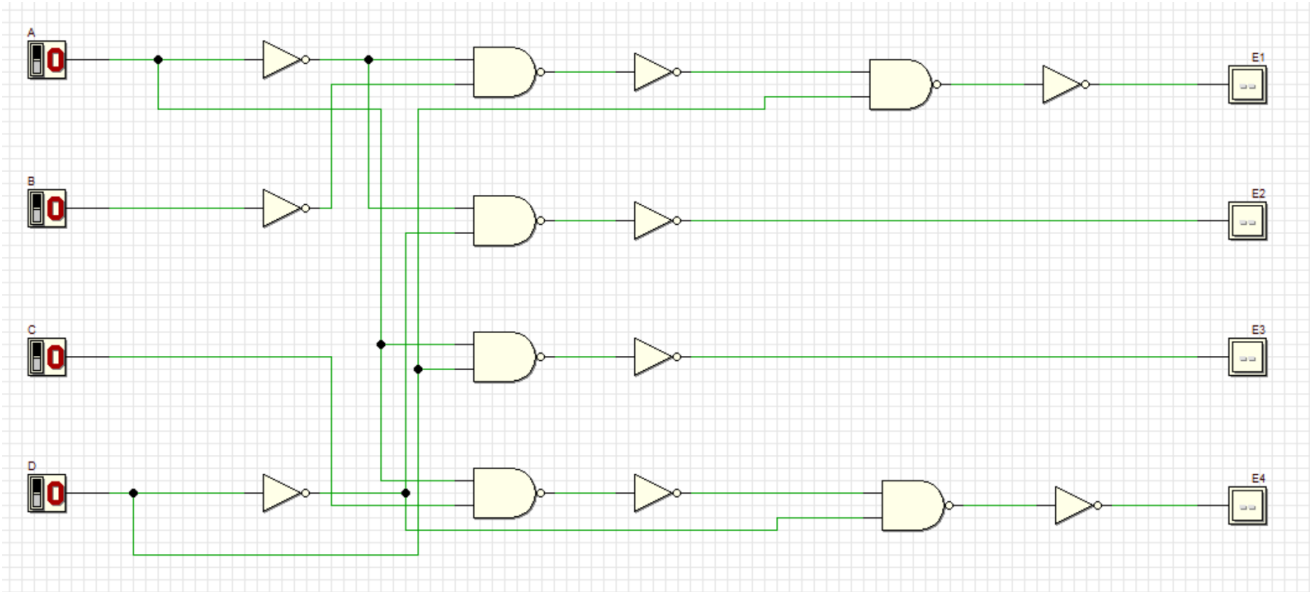
b) Timing Diagram

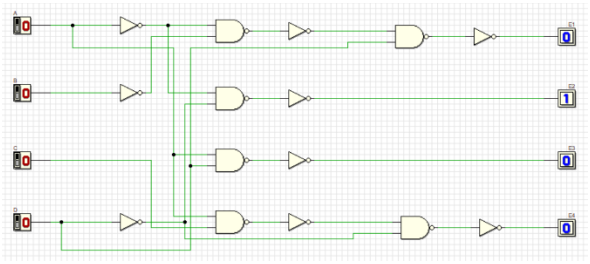
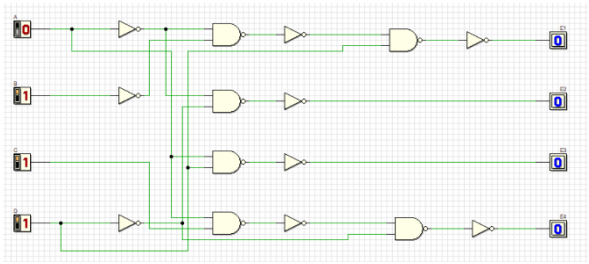
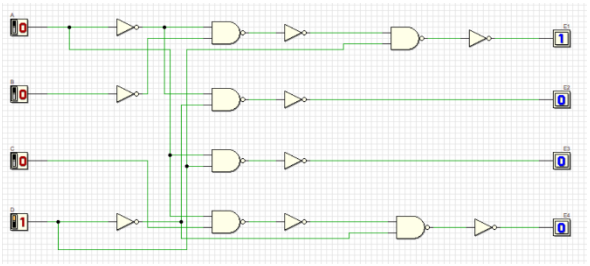
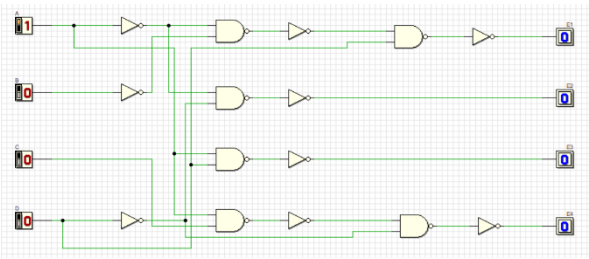
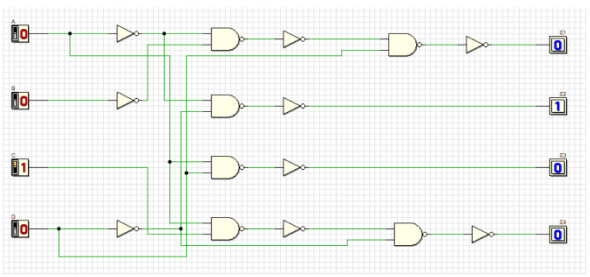
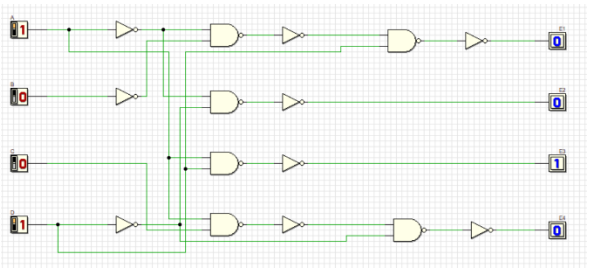
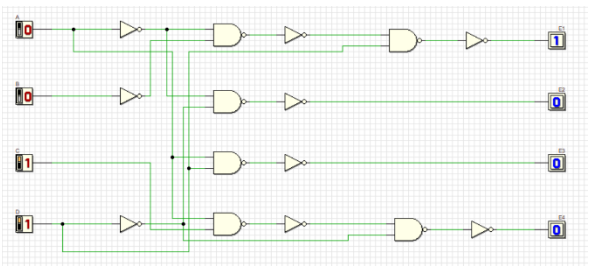
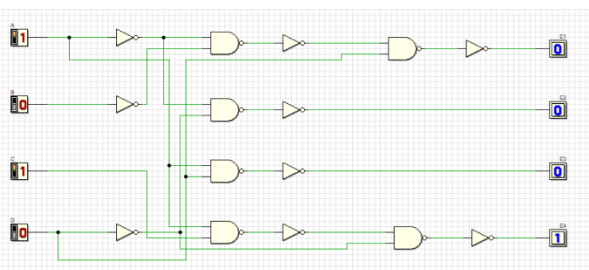
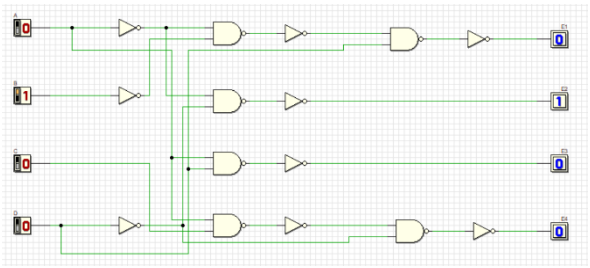
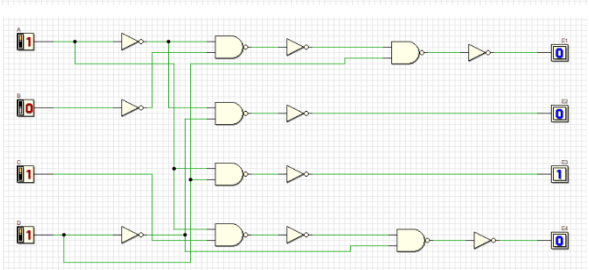
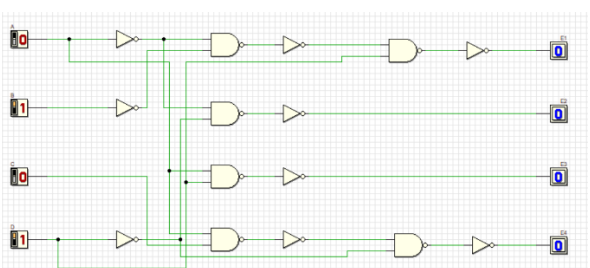
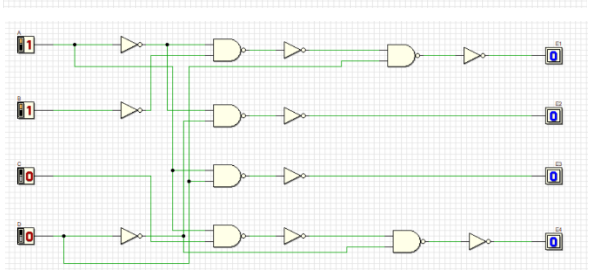
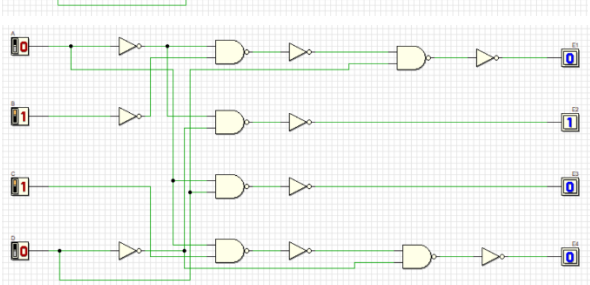
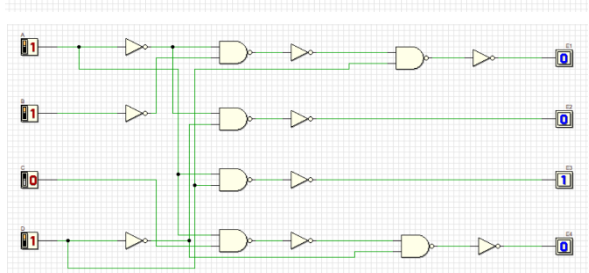


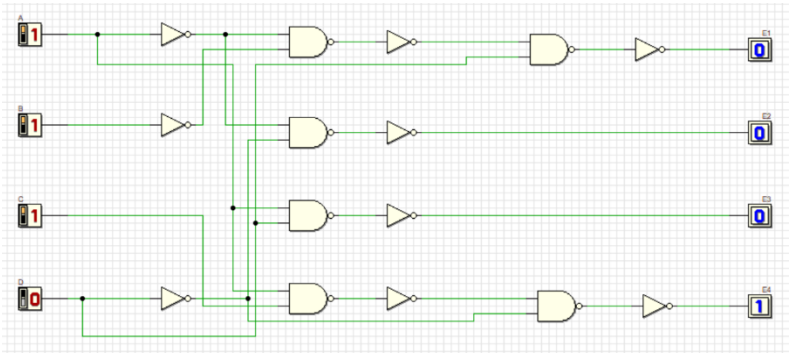

Explain some analysis values based on your timing diagram:

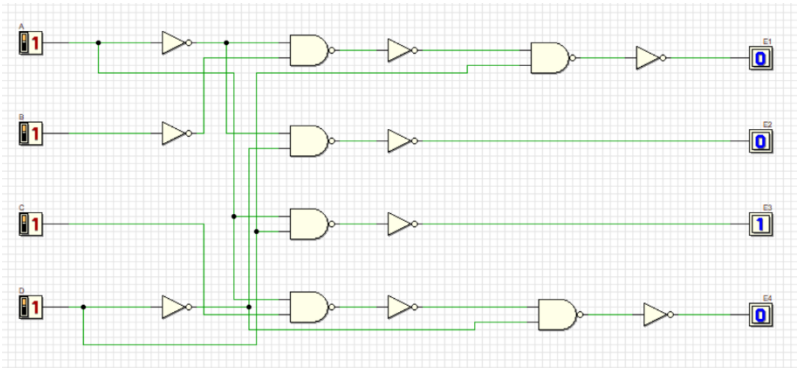
When input D is high and other inputs are low or input C and D is high and other inputs are low, output E1 is high. When all the inputs are low or input B and C is high and the other inputs are low or input B or input C is high and the other inputs are low, output E2 is high. When input A and D is high and the other inputs are low or input A, C and D are high and the input B are low or when input A, B and D are high and input C is low or all the inputs are high, output E3 is high. When inputs A and C are high and the other inputs are low or input A, B and C are high and input D is low, output E4 is high.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.




A
1
B
1
C
1
D
0
E1
0
E2
0
E3
0
E4
1


A
1
B
1
C
1
D
1
E1
0
E2
0
E3
1
E4
0

6. Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

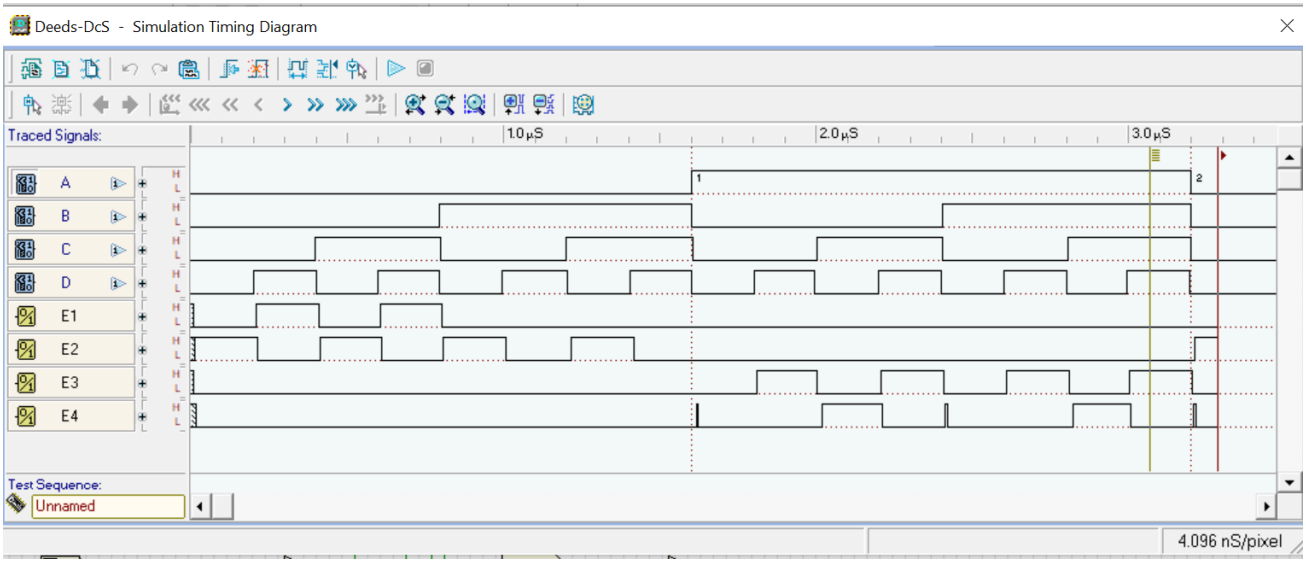
**Truth Table 3**

| INPUTS | | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| **A** | **B** | **C** | **D** | **E1** | **E2** | **E3** | **E4** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

NAND gate is the universal gate which can perform basic gate of AND gate and inverter.

b) Timing Diagram




Explain some analysis values based on your timing diagram:

When input D is high and other inputs are low or input C and D is high and other inputs are low, output E1 is high. When all the inputs are low or input B and C is high and the other inputs are low or input B or input C is high and the other inputs are low, output E2 is high. When input A and D is high and the other inputs are low or input A, C and D are high and the input B are low or when input A, B and D are high and input C is low or all the inputs are high, output E3 is high. When inputs A and C are high and the other inputs are low or input A, B and C are high and input D is low, output E4 is high.

Fully Completed ☐ Partially Completed ☐ Checked by: _____