Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT	:	SECR1013 DIGITAL LOGIC
SESSION/SEM	:	2020/2021 – Semester 1
LAB 2	**:**	**COMBINATIONAL LOGIC CIRCUIT DESIGN SIMULATION**
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DATE	:	12th January 2021

REMARKS :

MARKS:

Lab # 2

Combinational Digital Circuit Design Simulation Using Deeds Simulator

A. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds. Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

Variable = A, B & C (SOP)
There are 3 term from Y = AB + BC + AC

Term	Missing
AB	C or C’
BC	A or A’
AC	B or B’

Boolean Rule 6, A+A’ = 1

Term 1: AB(C+C’) = ABC + ABC’
Term 2: BC(A+A’) = ABC + A’BC
Term 3: AC(B+B’) = ABC + AB’C

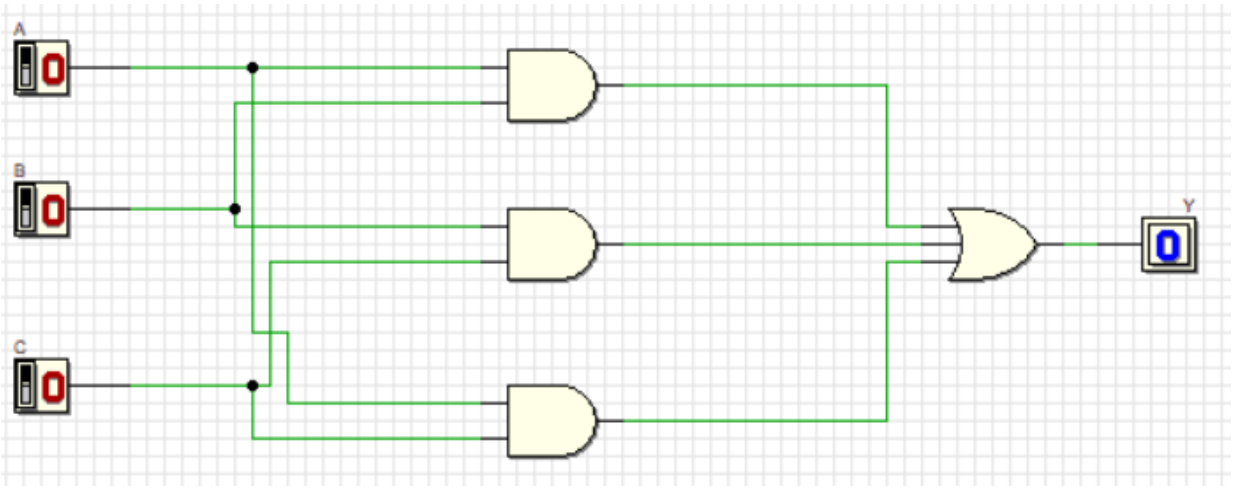
Y = ABC + ABC’ + ABC + A’BC + ABC + AB’C
= ABC + ABC’ + A’BC + AB’C

2. Based on standard form expression, complete the following truth table.

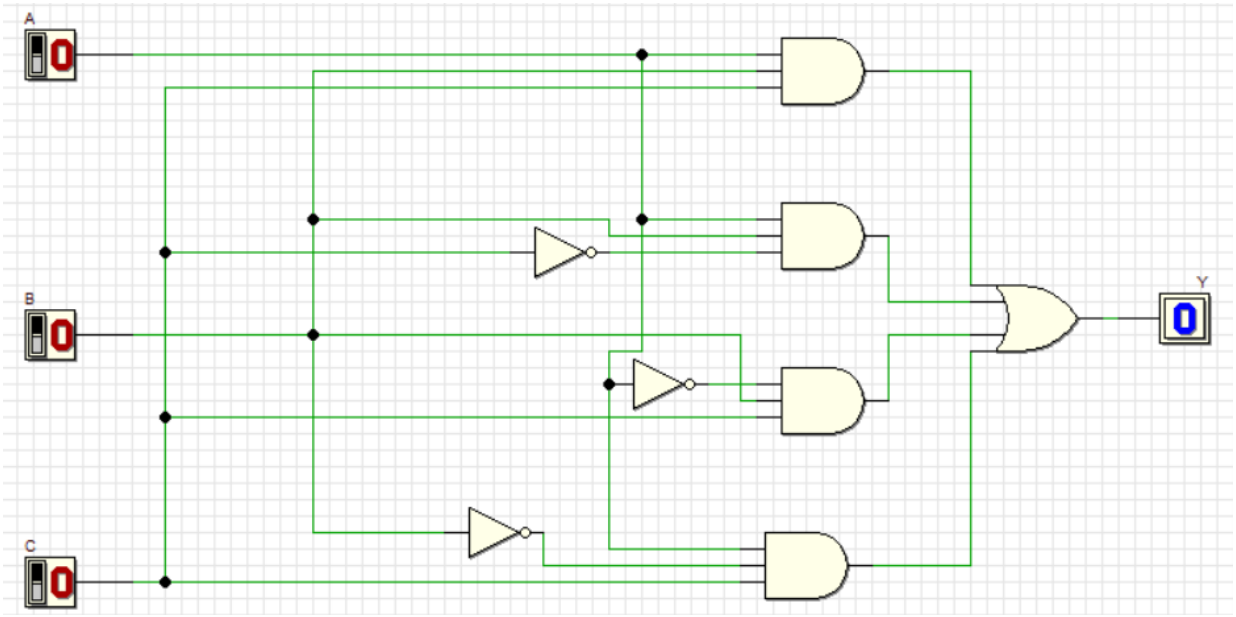
INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

3. Using Deeds Simulator, draw the following circuits and cut & paste your circuit below:

a) Circuit (i) for non-standard form (based on the given expression).



b) Circuit (ii) for standard form (from your answer in question (1)).



4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

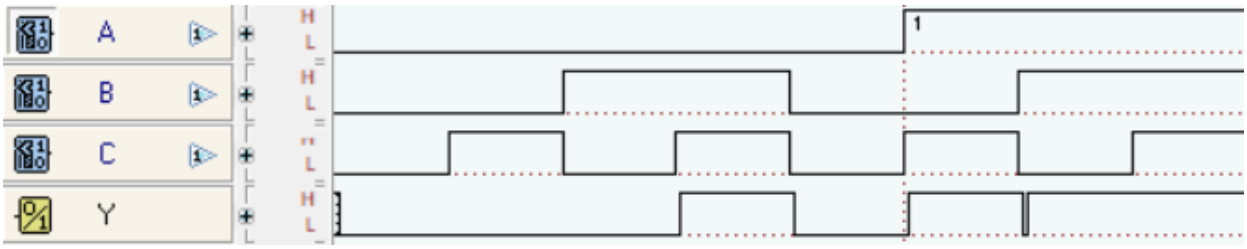
Circuit (ii)

INPUT			OUTPUT
A	**B**	**C**	**Y**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Conclusion:

The truth table of circuit (i) and circuit (ii) show the same result. The input and output for both tables are the same. The result of standard form and non-standard form produce the same result. The only difference between these circuits is the circuit (i) use lesser logic gates and while circuit (ii) use more logic gate. This show that non-standard form can reduce more cost.

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output. Cut & Paste the timing diagram here.



Part 2

Experimental Steps

1. **Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.**

Truth Table 1

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2. **Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.**

E1

CD / AB	00	01	11	10
00	0	1	X	0
01	0	X	0	X
11	X	0	0	0
10	0	X	0	X

E1 = A'B'D

E2

CD / AB	00	01	11	10
00	1	0	X	1
01	1	X	0	X
11	X	0	0	0
10	0	X	0	X

E2 = A'D'

E3

AB \ CD	00	01	11	10
00	0	0	X	0
01	0	X	0	X
11	X	1	1	0
10	0	X	1	X

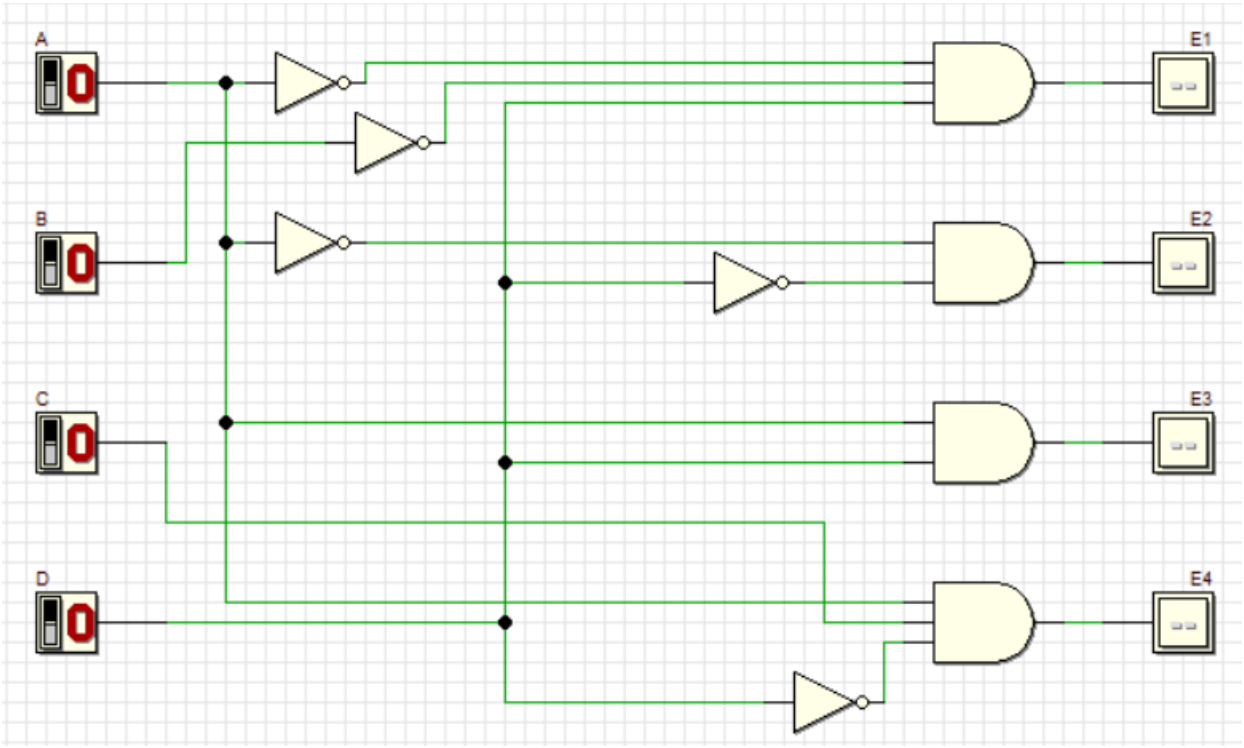
E3 = AD

E4

AB \ CD	00	01	11	10
00	0	0	X	0
01	0	X	0	X
11	X	0	0	1
10	0	X	0	X

E4 = ACD'

3. **From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.**



4. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

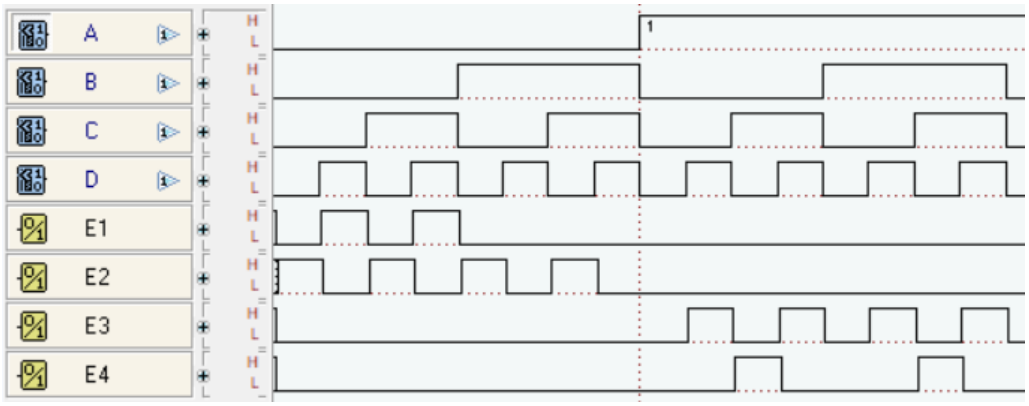
Truth Table 2

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

There is no ‘don’t care terms’ in Truth Table 2 but there is ‘don’t care terms’ in Truth Table 1. We can conclude that Truth Table 1 is the simplest logic circuit that consists of the fewest variables and fewest logic gates that matter only comparing with Truth Table 2. The purpose of using ‘don’t care terms’ is to create a simplest circuit results which reduce cost.

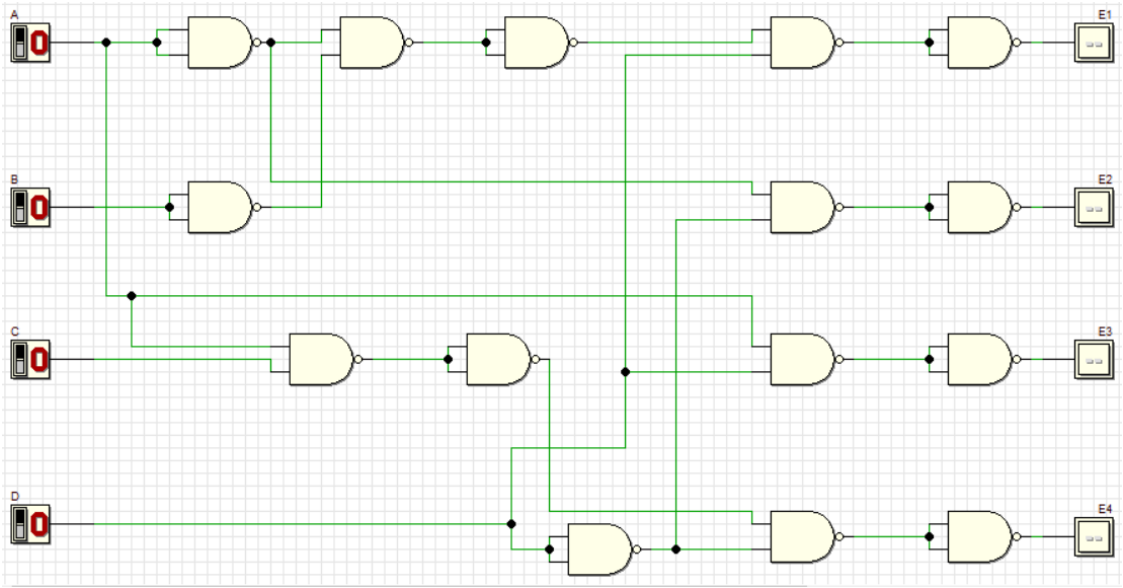
b) Timing Diagram



Explain some analysis values based on your timing diagram:

From the timing diagram above, E1 shows that the value '1' when A=0, B=0, D=1. For E2, it shows the value '1' when A=0, D=0. For E3, it shows the value '1' when A=1, D=1. For E4, it shows the value '1' when A=1, C=1, D=0.

5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.



6. **Simulate the Deeds circuit in step (5):**

a) Update Truth Table 3 based on the simulation result.

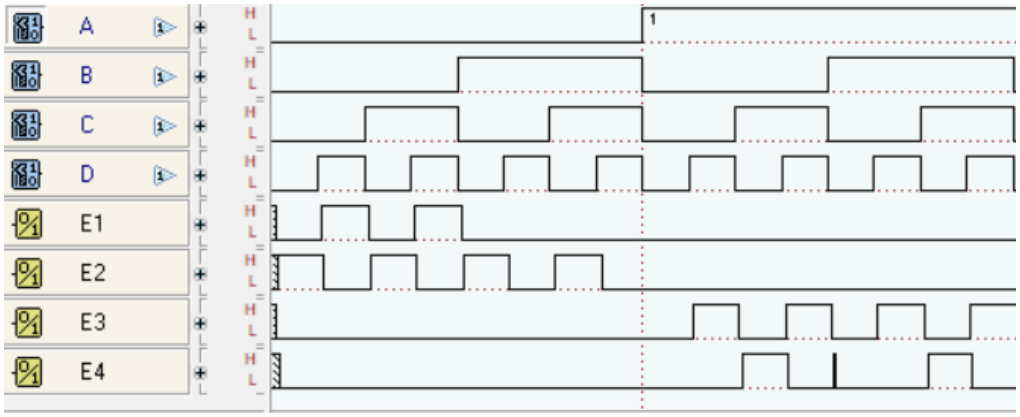
Truth Table 3

INPUTS				OUTPUTS			
A	**B**	**C**	**D**	**E1**	**E2**	**E3**	**E4**
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

The output results in Truth Table 3 is same as Truth Table 2. The SOP circuit if converted to NAND gates only. We can conclude that NAND gate is a universal gate that can perform as AND gate and NOT gate which are used in the circuit of Truth Table 2.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

The input state for this timing diagram is active-high. E1 shows the value ‘1’ when A=0, B=0, D=1. While E2 shows the value ‘1’ when A=0, D=0. And for E3, it shows the value ‘1’ when A=1, D=1. E4 shows the value ‘1’ when A=1, C=1, D=0.

Fully Completed ☐ Partially Completed ☐ Checked by: _____