**Department of Computer**

**Science**

**Faculty of Comput**

**ing**

**UNIVERSITI TEKNOLOGI MALAYSIA**



**MARKS:**

|  |
| --- |
|  SUBJECT : SCSR1013 DIGITAL LOGIC SESSION/SEM : ………………………………………………………………….  |
| **LAB 2 : OMBINATIONAL LOGIC CIRCUIT DESIGN** **SIMULATION**  |
|  NAME 1 ：Singthai Srisoi  DATE : 9.1.2021  |

 REMARKS :

**D. Lab Activities**

# Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

*Y*=*AB*+*BC*+*AC*

1. Convert the non-standard Boolean expression into standard form.

1. Based on standard form expression, complete the following truth table.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **INPUT**  |  | **OUTPUT**  |
| **A**  | **B**  | **C**  | **Y**  |
|  0 |  0 |  0 |  0 |
|  0 | 0  | 1  |  0 |
|  0 |  1 | 0  | 0  |
|  0 |  1 |  1 | 1  |
|  1 |  0 |  0 |  0 |
|  1 | 0  |  1 | 1  |
|  1 |  1 |  0 | 1  |
|  1 |  1 | 1  | 1  |

1. Using Deeds Simulator, draw the following circuits:

1. Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

1. Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

1. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

 Circuit (i)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **INPUT**  |  | **OUTPUT**  |
| **A**  | **B**  | **C**  | **Y**  |
|  0 |  0 |  0 |  0 |
|  0 | 0  | 1  |  0 |
|  0 |  1 | 0  | 0  |
|  0 |  1 |  1 | 1  |
|  1 |  0 |  0 |  0 |
|  1 | 0  |  1 | 1  |
|  1 |  1 |  0 | 1  |
|  1 |  1 | 1  | 1  |

 Circuit (ii)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **INPUT**  |  | **OUTPUT**  |
| **A**  | **B**  | **C**  | **Y**  |
|  0 |  0 |  0 |  0 |
|  0 | 0  | 1  |  0 |
|  0 |  1 | 0  | 0  |
|  0 |  1 |  1 | 1  |
|  1 |  0 |  0 |  0 |
|  1 | 0  |  1 | 1  |
|  1 |  1 |  0 | 1  |
|  1 |  1 | 1  | 1  |

 Conclusion:

The truth table of circuit 1 and circuit 2 are the same. Hence circuit 1 is the simpler version of circuit 2.

1. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.

# Part 2

Combinational circuit design process and simulate with Deeds Simulator.

## Design Process

1. Determine Parameter Input / Output and their relations.
2. Construct Truth Table. iii) Using K-Map, get the SOP optimized form of all Boolean equation outputs.
3. Draw the circuit and use duality symbol; convert AND-OR circuit to NAND gates ONLY.
4. Simulate the design using Deeds Simulator. Check the results according to Truth Table and Timing Diagram Operation.

## Problem Situation

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2’s complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 5, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.



## Figure 5

The following rules are used to activate the error’s signal type:

|  |  |
| --- | --- |
| **RULE 1**:  | E1 is activated if the input number is positive ODD and the majority of the bits is ‘0’.  |
| **RULE 2**:  | E2 is activated if the input number is positive EVEN and the majority of the bits is ‘0’.  |
| **RULE 3**:  | E3 is activated if the input number is negative ODD and the majority of the bits is ‘1’.  |
| **RULE 4**:  | E4 is activated if the input number is negative EVEN and the majority of the bits is ‘1’.  |
| **RULE 5**:  | The output of error signal is invalid if the input has equal bit ‘0’  |

and bit ‘1’.

 (**NOTE:** Positive ODD is positive numbers that are odd and negative

 EVEN is negative numbers that are even).

## Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

## Truth Table 1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **INPUTS**  |  |  | **OUTPUTS**  |  |
| **A**  | **B**  | **C**  | **D**  | **E1**  | **E2**  | **E3**  | **E4**  |
|  0 |  0 |  0 |  0  | 0 |  1 |  0 |  0 |
|  0 |  0 |  0 |  1  |  1 |  0 |  0 |  0 |
|  0 |  0 |  1 |  0  |  0 |  1 |  0 |  0 |
|  0 |  0 |  1 |  1  |  x |  x |  x |  x |
|  0 |  1 |  0 |  0  |  0 |  1 |  0 |  0 |
|  0 |  1 |  0 |  1  |  x |  x |  x |  x |
|  0 |  1 |  1 |  0  |  x |  x |  x |  x |
|  0 |  1 |  1 |  1  |  1 |  0 |  0 |  0 |
|  1 |  0 |  0 |  0  |  0 |  0 |  0 |  1 |
|  1 |  0 |  0 |  1  |  x |  x |  x |  x |
|  1 |  0 |  1 |  0  |  x |  x |  x |  x |
|  1 |  0 |  1 |  1 |  0 |  0 |  1 |  0 |
|  1 |  1 |  0 |  0  |  x |  x |  x |  x |
|  1 |  1 |  0 |  1  |  0 |  0 |  1 |  0 |
|  1 |  1 |  1 |  0  |  0 |  0 |  0 |  1 |
|  1 |  1 |  1 |  1  |  0 |  0 |  1 |  0 |

1. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.



1. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



1. Simulate the Deeds circuit in step (3):

a) Update Truth Table 2 based on the simulation result.

## Truth Table 2

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **INPUTS**  |  |  | **OUTPUTS**  |  |
| **A**  | **B**  | **C**  | **D**  | **E1**  | **E2**  | **E3**  | **E4**  |
|  0 |  0 |  0 |  0 |  0 |  1 |  0 |  0 |
|  0 | 0  |  0 | 1  |  1 |  0 |  0 |  0 |
|  0 |  0 |  1 |  0 |  0 |  1 |  0 |  0 |
|  0 |  0 |  1 |  1 |  1 |  0 |  0 |  0 |
|  0 |  1 |  0 |  0 |  0 |  1 |  0 |  0 |
|  0 |  1 |  0 |  1 |  1 |  0 |  0 |  0 |
|  0 |  1 |  1 |  0 |  0 |  1 |  0 |  0 |
|  0 |  1 |  1 |  1 |  1 |  0 |  0 |  0 |
|  1 |  0 |  0 |  0 |  0 |  0 |  0 |  1 |
|  1 |  0 |  0 |  1 |  0 |  0 |  1 |  0 |
|  1 |  0 |  1 |  0 |  0 |  0 |  0 |  1 |
|  1 |  0 |  1 |  1 |  0 |  0 |  1 |  0 |
|  1 |  1 |  0 |  0 |  0 |  0 |  0 |  1 |
|  1 |  1 |  0 |  1 |  0 |  0 |  1 |  0 |
|  1 |  1 |  1 |  0 |  0 |  0 |  0 |  1 |
|  1 |  1 | 1  |  1 |  0 |  0 |  1 | 0  |

Compare the output results in Truth Table 2 with Truth Table 1. What is your conclusion?

Truth table 2 did not include the don’t care condition

b) Timing Diagram

Explain some analysis values based on your timing diagram:

E1 is the inverse of E2 for the first eight output

E3 is the inverse of E4 for the last eight output

1. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator.

1. Simulate the Deeds circuit in step (5):

a) Update Truth Table 3 based on the simulation result.

## Truth Table 3

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **INPUTS**  |  |  | **OUTPUTS**  |  |
| **A**  | **B**  | **C**  | **D**  | **E1**  | **E2**  | **E3**  | **E4**  |
|  0 |  0 |  0 |  0 |  0 |  1 |  0 |  0 |
|  0 | 0  |  0 | 1  |  1 |  0 |  0 |  0 |
|  0 |  0 |  1 |  0 |  0 |  1 |  0 |  0 |
|  0 |  0 |  1 |  1 |  1 |  0 |  0 |  0 |
|  0 |  1 |  0 |  0 |  0 |  1 |  0 |  0 |
|  0 |  1 |  0 |  1 |  1 |  0 |  0 |  0 |
|  0 |  1 |  1 |  0 |  0 |  1 |  0 |  0 |
|  0 |  1 |  1 |  1 |  1 |  0 |  0 |  0 |
|  1 |  0 |  0 |  0 |  0 |  0 |  0 |  1 |
|  1 |  0 |  0 |  1 |  0 |  0 |  1 |  0 |
|  1 |  0 |  1 |  0 |  0 |  0 |  0 |  1 |
|  1 |  0 |  1 |  1 |  0 |  0 |  1 |  0 |
|  1 |  1 |  0 |  0 |  0 |  0 |  0 |  1 |
|  1 |  1 |  0 |  1 |  0 |  0 |  1 |  0 |
|  1 |  1 |  1 |  0 |  0 |  0 |  0 |  1 |
|  1 |  1 | 1  |  1 |  0 |  0 |  1 | 0  |

##

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?

Table 3 and table 2 are the same. Hence the circuit is the same.

b) Timing Diagram

Explain some analysis values based on your timing diagram:

E1 is the inverse of E2

E3 is the inverse of E4

|  |  |  |
| --- | --- | --- |
|   | Partially Completed  |   |

Fully

 Completed Checked by: \_\_\_\_\_\_\_\_\_\_