UTM

UNIVERSITI TEKNOLOGI MALAYSIA

DIGITAL LOGIC

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SECR1013-05

LAB 2

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D. Lab Activities

Part 1

Simulating logic circuit, construct truth table and timing diagram with Deeds.

Given Boolean expression as follow:

$$Y = AB + BC + AC$$

1. Convert the non-standard Boolean expression into standard form.

$Y = AB + BC + AC$
$T_1 \quad T_2 \quad T_3$

T_1 : C missing
T_2 : A missing
T_3 : B missing

$T_1 : AB = AB(C + \bar{C})$
$= ABC + AB\bar{C}$

$T_2 : BC = BC(A + \bar{A})$
$= ABC + \bar{A}BC$

$T_3 : AC = AC(B + \bar{B})$
$= ABC + A\bar{B}C$

$\therefore Y = ABC + AB\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C$

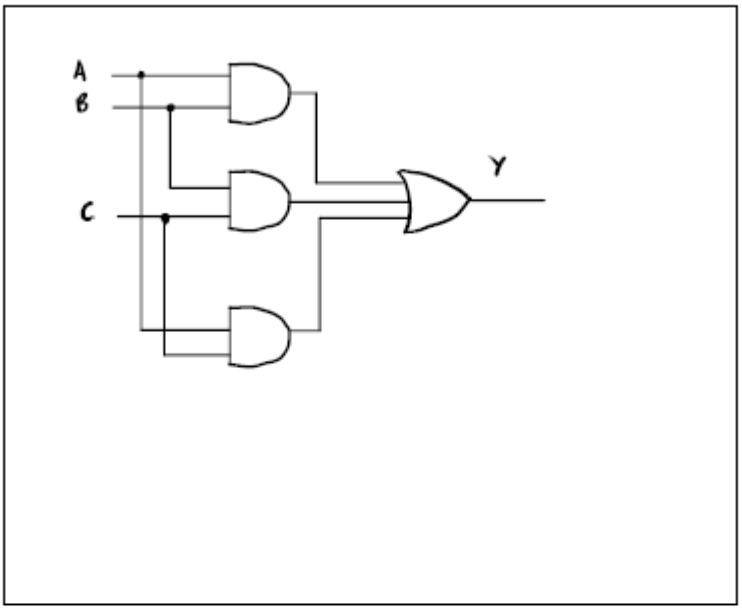
$Y = ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$ (standard form)

2. Based on standard form expression, complete the following truth table.

INPUT			OUTPUT
A	B	C	Y
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

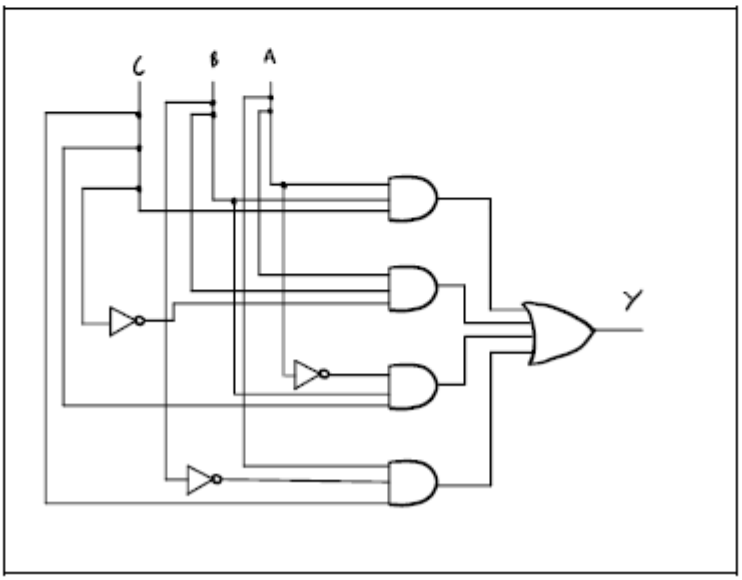
3. Using Deeds Simulator, draw the following circuits:

a) Circuit (i) for non-standard form (based on the given expression).



Circuit (i)

b) Circuit (ii) for standard form (from your answer in question (1)).



Circuit (ii)

4. Simulate these two circuits in step (3) and complete their truth table.

Compare the simulation result for these two truth tables. What is your conclusion?

Circuit (i)

INPUT			OUTPUT
A	B	C	Y
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

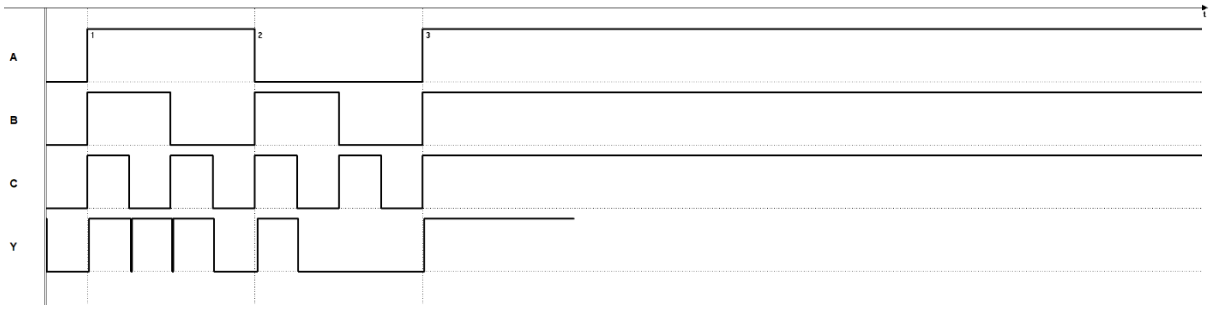
Circuit (ii)

INPUT			OUTPUT
A	B	C	Y
1	1	1	1
1	1	0	1
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

Conclusion:

The outputs of both circuits are the same. This is because both expressions are the same and the difference is that the expression in circuit (i) is simpler than in circuit (ii).

5. Simulate output of circuit (ii) with Timing Diagram. Illustrate some examples of different inputs and output.



Experimental Steps

1. Complete Truth Table 1 for Digital Fault Diagnose Circuit. Use variables A, B, C and D as inputs; E1, E2, E3 and E4 as outputs.

Truth Table 1

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	X	X	X	X
0	1	0	0	0	1	0	0
0	1	0	1	X	X	X	X
0	1	1	0	X	X	X	X
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	X	X	X	X
1	0	1	0	X	X	X	X
1	0	1	1	0	0	1	0
1	1	0	0	X	X	X	X
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

2. Using K-MAP, get minimized SOP Boolean expressions for E1, E2, E3 and E4 circuits.

E1

cd / ab	00	01	11	10
00	0	1	x	0
01	0	x	0	x
11	x	0	0	0
10	0	x	0	x

E1 = $\bar{A}\bar{B}D$

E2

cd / ab	00	01	11	10
00	1	0	x	1
01	1	x	0	x
11	x	0	0	0
10	0	x	0	x

E2 = $\bar{A}\bar{D}$

E3

ab \ cd	00	01	11	10
00	0	0	x	0
01	0	x	0	x
11	x	1	1	0
10	0	x	1	x

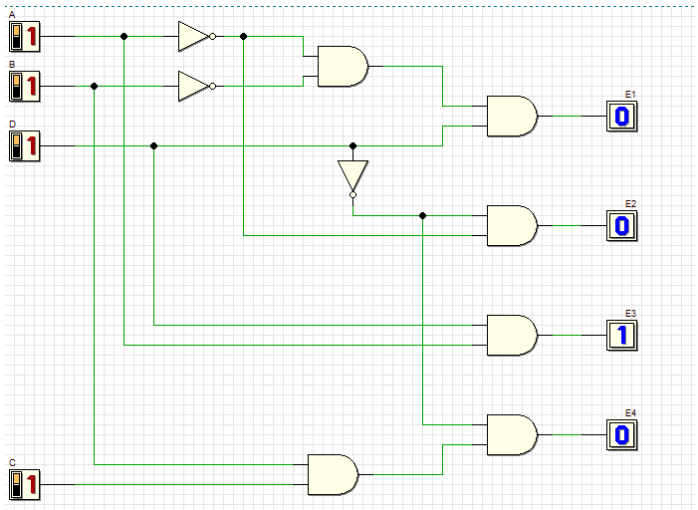
E3 = AD

E4

ab \ cd	00	01	11	10
00	0	0	x	0
01	0	x	0	x
11	x	0	0	1
10	0	x	0	x

E4 = BCD̄

3. From the Boolean expression in the step (2), draw your final E1, E2, E3 and E4 circuits using 2 input basic gates (AND, OR, NOT). Use Deeds Simulator.



4. Simulate the Deeds circuit in step (3):

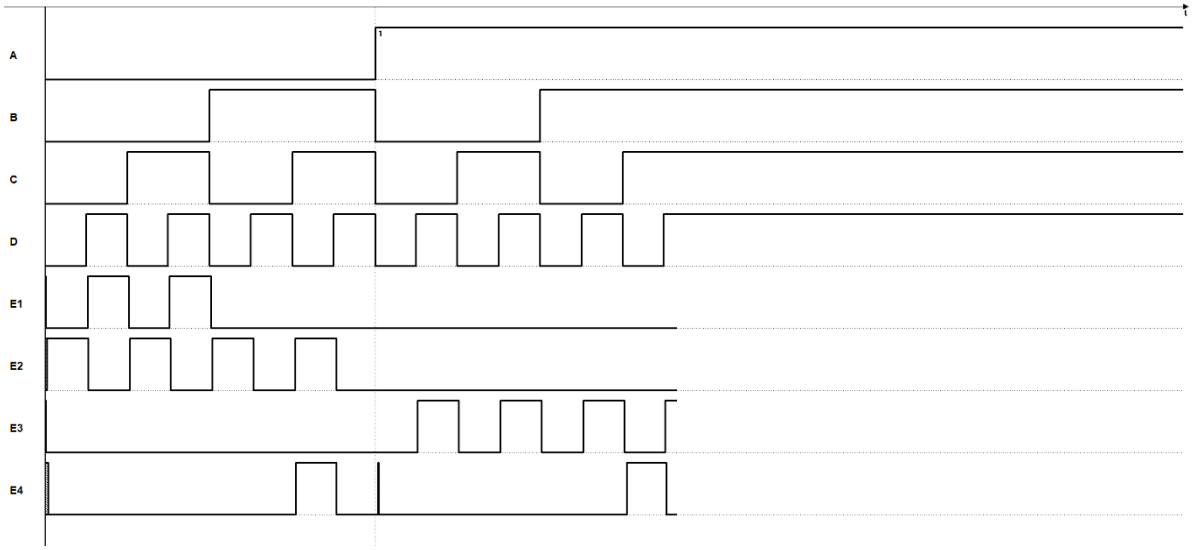
a) Update Truth Table 2 based on the simulation result.

Truth Table 2

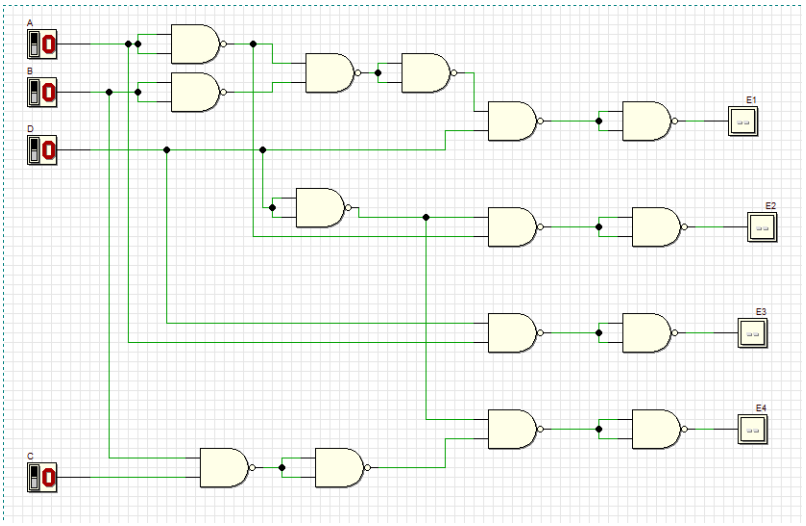
INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in truth table 2 with truth table 1. What is your conclusion?
It is the same output

B) Timing diagram



5. Using dual symbol concept, convert your circuit in step (3) to NAND gates only. Use Deeds Simulator



6) Simulate the Deeds circuit in step (5)

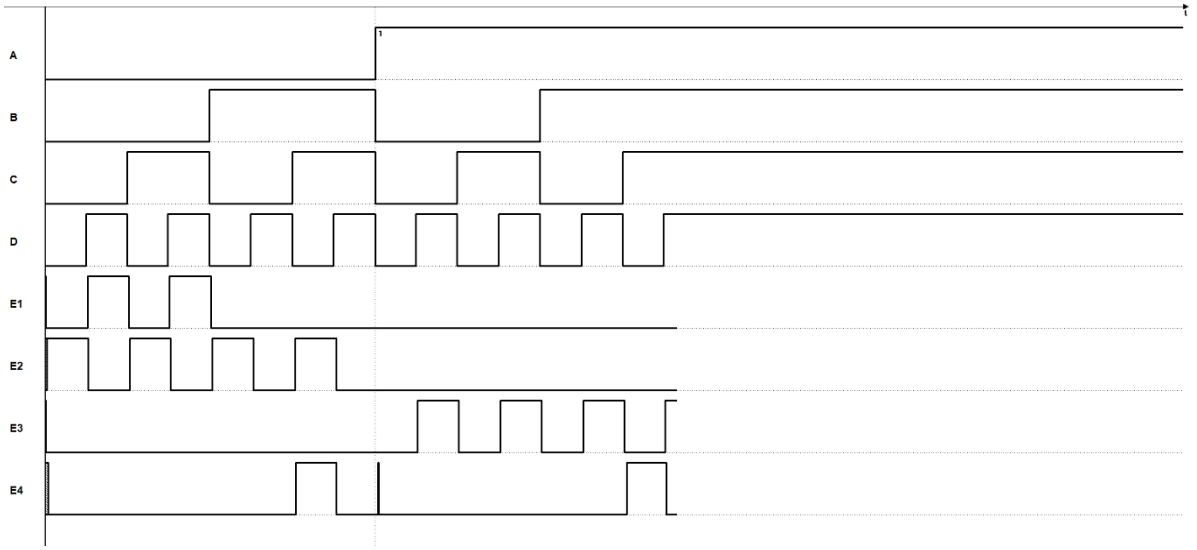
a) Update Truth table 3 based on the simulation result

Truth table 3

INPUTS				OUTPUTS			
A	B	C	D	E1	E2	E3	E4
0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	1	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	0	1	1	0	0	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	1	0

Compare the output results in Truth Table 3 with Truth Table 2. What is your conclusion?
It gives the same output with truth table 2.

b) Timing Diagram



Explain some analysis values based on your timing diagram:

The outcome is similar due to how the NAND gates work thus the timing diagram is similar to the ones before