UNIVERSITI TEKNOLOGI MALAYSIA

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SCSR1013 DIGITAL LOGIC

MODULE 8b: COUNTERS (SYNC)

2016/2017-1

FACULTY OF COMPUTING

Synchronous Counters:

Synchronous Counter Design

- Step 1
  Describe a general sequential circuit in terms of its basic parts and its input and outputs.
- Step 2
  Develop state diagram
- Step 3
  Create next state table
- Step 4
  Create flip-flop transition table.

  excitation table
- Step 5
  Use K-maps to derive the logic equations.
- Step 6
  Implement counter implementation

FF Excitation Table

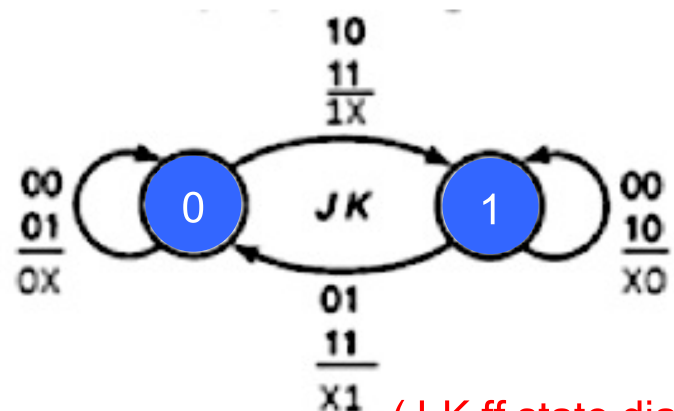
About creating Next State table

- JK Flip-Flop

	FF State J	FF State K		
NO CHANGE	0	0	0	0
RESET	0	1	0	0
SET	1	0	0	1
TOGGLE	1	1	0	1

(Refer to JK FF truth table in module 7: page 228)

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



(J-K ff state diagram)

Exercise 8b.1:

Construct the excitation table for **D flip-flop**

(using its state diagram)

Exercise 8b.2:

Construct the excitation table for **T flip-flop**

(using its state diagram)

Note:
These excitation tables will be used while filling in the flip-flop transition table in STEP 4 of designing synchronous counter.

Summary

Excitation tables of flip-flops:

	Present State	Next State	FF State	
	Q_n	Q_{n+1}	J	K
NO CHANGE / RESET	0	0	0	X
SET / TOGGLE	0	1	1	X
RESET / TOGGLE	1	0	X	1
NO CHANGE / SET	1	1	X	0

J-K flip-flop

Q_{n+1}	D
0	0
1	1

D flip-flop

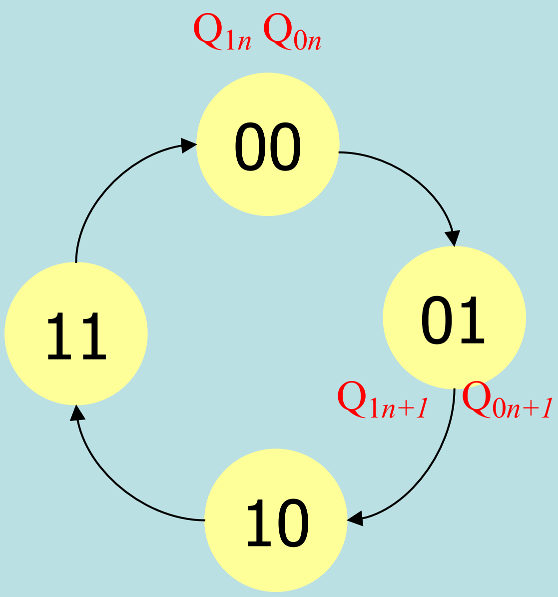
Q_{n+1}	T
Q_n	0
$\overline{Q_n}$	1

T flip-flop

Design 2-bit Synchronous Counter: J-K Flip-flop

- Step 1:
  To design 2-bit synchronous counter using JK FF. There is no input or output element in this design.

- Step 2: Draw state diagram



- Step 3: Create next state table

Present State		Next State	
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Step 4:

  Construct the flip-flop transition table

FF1 FF0

Present State		Next State		JK Transition			
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}	J_1	K_1	J_0	K_0
0	0	0	1				
0	1	1	0				
1	0	1	1				
1	1	0	0				

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Step 4:

  Construct the flip-flop transition table

FF1 FF0

Present State		Next State		JK Transition			
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}	J_1	K_1	J_0	K_0
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1

FF1 FF0

Present State		Next State		JK Transition			
Q_{1n}	Q_{0n}	Q_{1n+1}	Q_{0n+1}	J_1	K_1	J_0	K_0
0	0			0	X	1	X
0	1			1	X	X	1
1	0			X	0	1	X
1	1			X	1	X	1

- Step 5:
  Use K-maps to derive the logic equations

  (for present state only).

J_1

$Q_1 \backslash Q_0$	0	1
0	0	1
1	X	X

$J_1 = Q_0$

J_0

$Q_1 \backslash Q_0$	0	1
0	1	X
1	1	X

$J_0 = 1$

K_1

$Q_1 \backslash Q_0$	0	1
0	X	X
1	0	1

$K_1 = Q_0$

K_0

$Q_1 \backslash Q_0$	0	1
0	X	1
1	X	1

$K_0 = 1$

- Step 6: Implement counter implementation by drawing the logic symbol connection / counter circuit.

FF0

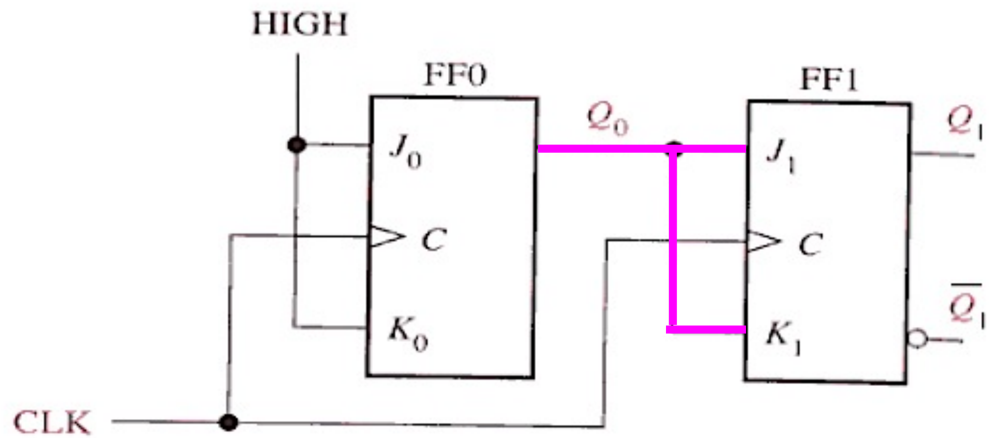
$J_0 = 1$

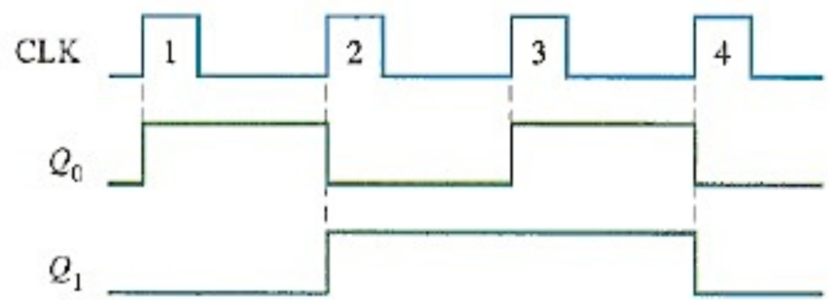
$K_0 = 1$

FF1

$J_1 = Q_0$

$K_1 = Q_0$





Q_1 toggle when $Q_0=1$

- Q_0 toggle at positive edge (CLK1, CLK2, CLK3, CLK4)
- Q_1 toggle when $Q_0=1$ at positive edge (CLK2, CLK4)

Extra

Exercise 8b.3: Design 2-bit synchronous counter that using D flip-flop. Show all steps clearly.

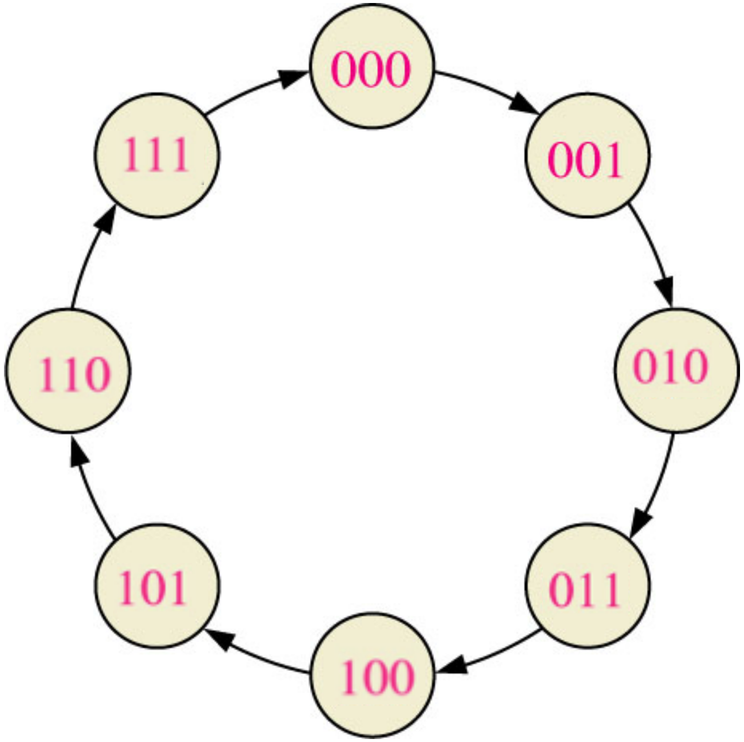
Extra

Exercise 8b.4: Design 2-bit synchronous counter that using T flip-flop. Show all steps clearly.

Design 3-bit Synchronous Counter:

J-K Flip-flop

- Step 2: State diagram



- Step 3: Next State table

Present State			Next State		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Note:
While filling in the flip-flop transition table, refer to the excitation table.

Present State	Next State	FF State	
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

- Step 4:

  FF transition table

FF2 FF1 FF0

Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

(Module page: 259)

- **Step 5**:

Create K-map to determine the Boolean expression

Present State			Next State			JK Transition Table					
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0				0	X	0	X	1	X
0	0	1				0	X	1	X	X	1
0	1	0				0	X	X	0	1	X
0	1	1				1	X	X	1	X	1
1	0	0				X	0	0	X	1	X
1	0	1				X	0	1	X	X	1
1	1	0				X	0	X	0	1	X
1	1	1				X	1	X	1	X	1

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$$J_2 = Q_1Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$$J_1 =$$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$$J_0 =$$

Q_2 \ Q_1Q_0	00	01	11	10
0				
1				

$$K_2 =$$

Q_2 \ Q_1Q_0	00	01	11	10
0				
1				

$$K_1 =$$

Q_2 \ Q_1Q_0	00	01	11	10
0				
1				

$$K_0 =$$

**Fill in the K-maps

- **Step 5**:

Create K-map to determine the Boolean expression

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	1	0
1	X	X	X	X

$$J_2 = Q_1Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$$J_1 = Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$$J_0 = 1$$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	X	X
1	0	0	1	0

$$K_2 = Q_1Q_0$$

Q_2 \ Q_1Q_0	00	01	11	10
0	X	X	1	0
1	X	X	1	0

$$K_1 = Q_0$$

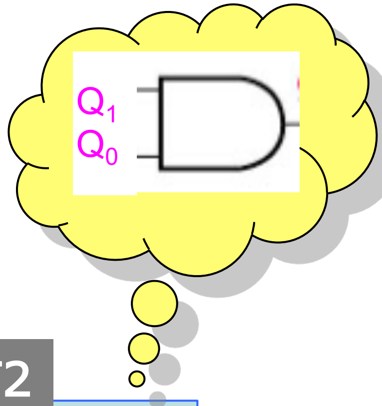
Q_2 \ Q_1Q_0	00	01	11	10
0	X	1	1	X
1	X	1	1	X

$$K_0 = 1$$

**Fill in the K-maps

- Step 6:

  The implementation of 3-bit synchronous counter



FF0

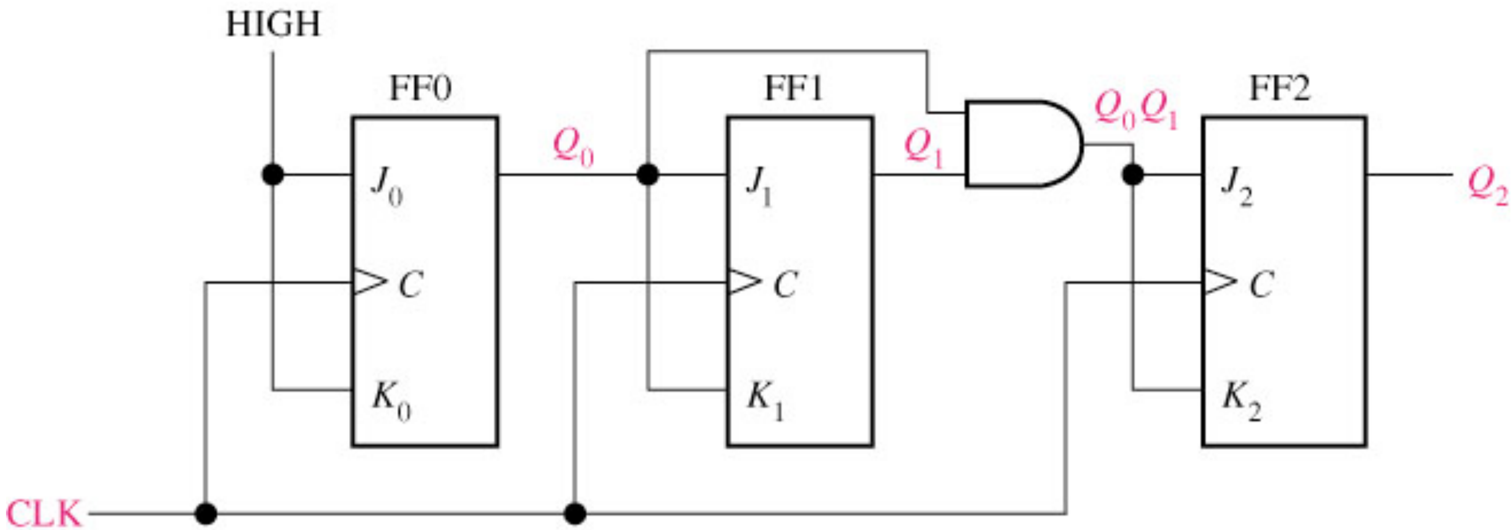
$$J_0 = 1$$
$$K_0 = 1$$

FF1

$$J_1 = Q_0$$
$$K_1 = Q_0$$

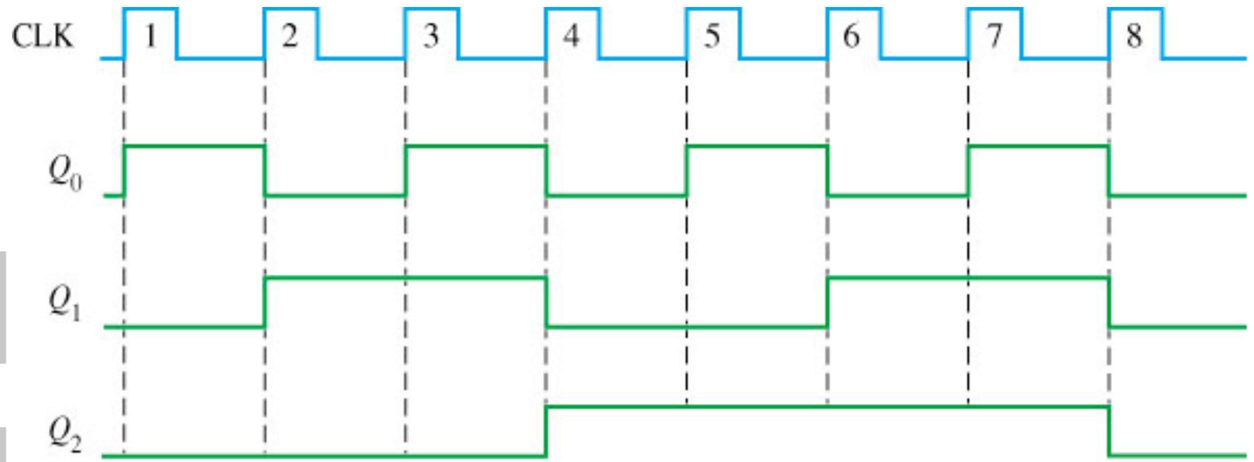
FF2

$$J_2 = Q_1 Q_0$$
$$K_2 = Q_1 Q_0$$



Q_1 toggle when $Q_0=1$

Q_2 toggle when $Q_0=Q_1=1$



Note:

Actually we can design a synchronous counter by observing its timing diagram, based on the above timing diagram:

Q_0 always toggle. To achieve this, we have to operate FF0 in toggle mode by connecting J_0 and K_0 to HIGH

Q_1 goes to opposite state every time Q_0 is HIGH (at the positive edge of clock CLK2, CLK4,CLK6 and CLK8).

From the observation we can achieve this by connecting Q_0 to the J_1 and K_1 inputs of FF1

Q_2 changes state when both Q_0 and Q_1 is HIGH. (at the positive edge of clock CLK4 and CLK8).

From the observation we can achieve this by 'AND'ing Q_0 and $Q_1$to the J_2 and K_2 inputs of FF2

Extra

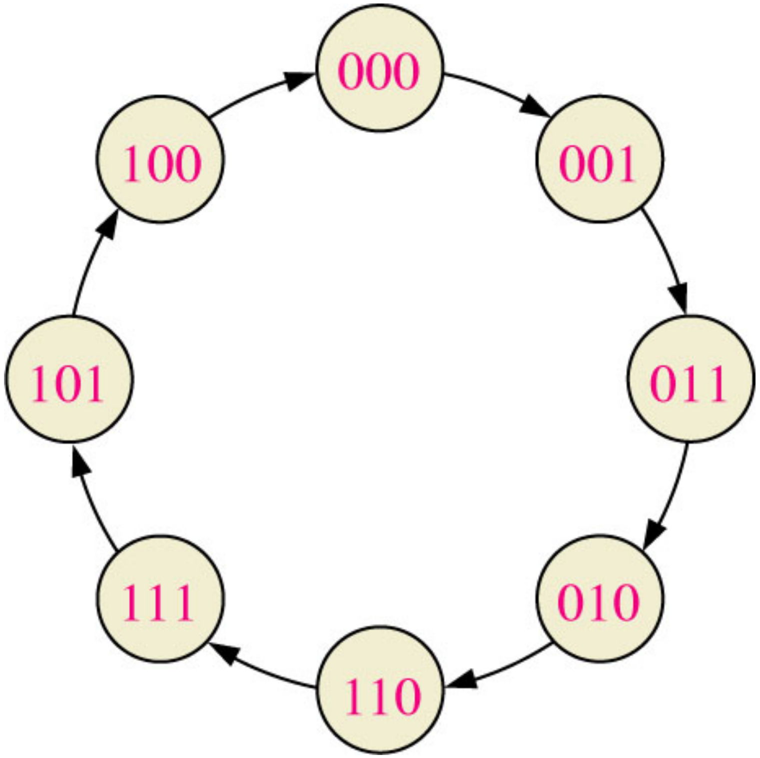
Exercise 8b.5: Design 3-bit synchronous counter that using T flip-flop. Show all steps clearly.

Extra

Exercise 8b.6: Design 4-bit synchronous counter that using J-K flip-flop with negative edge triggered. Show all steps clearly.

Extra

Exercise 8b.7: Design 3-bit synchronous counter that using J-K flip-flop based on the state diagram below. Show all steps clearly.



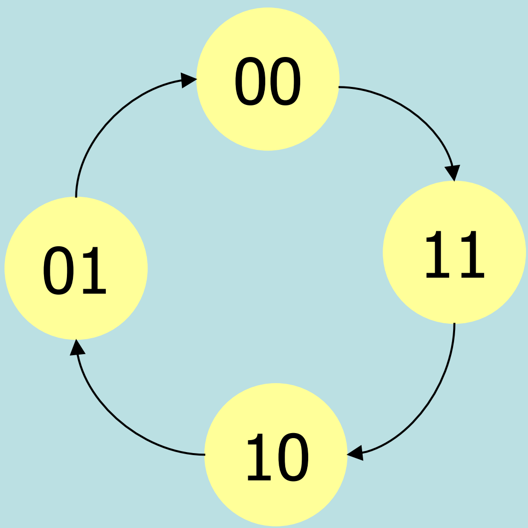
Extra

Exercise 8b.7b: Continue exercise 8b.7 by drawing the counter design.

2-bit Down Synchronous Counter: D Flip-flop

- Step 1:
  To design 2-bit down synchronous counter using D FF. There is no input or output element in this design.

- Step 2: Draw state diagram



- Step 3: Create next state table

Present State		Next State	
Q_1	Q_0	Q_{1+}	Q_{0+}
0	0	1	1
0	1	0	0
1	0	0	1
1	1	1	0

- **Step 4:**

  Draw flip-flop transition table. For D FF, D input is the same as the next state values.

Q_{n+1}	D
0	0
1	1

Present State		Next State		D Transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
0	0	1	1	1	1
0	1	0	0	0	0
1	0	0	1	0	1
1	1	1	0	1	0

- **Step 5:** K-Map.

Q_1 \ Q_0	0	1
0	1	0
1	1	0

$$D_0 = Q_0$$

Q_1 \ Q_0	0	1
0	1	0
1	0	1

$$D_1 = \overline{Q}_1\overline{Q}_0 + Q_1Q_0$$

$$D_1 = Q_0 \odot Q_1$$

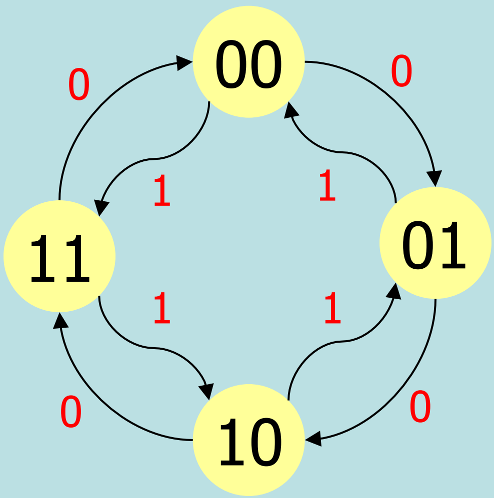
Exercise 8b.8: Draw the circuit for of 2-bit down synchronous counter using D FF with $D1 = Q0 \odot Q1$ and $D0 = \overline{Q0}$

(Refer previous example: module page 262)

2-bit UP/DOWN Synchronous Counter: D Flip-flop

- Step 1:
  To design 2-bit up down synchronous counter using D FF based on input X. When X=0 → Counter UP and X=1 → Counter DOWN

- Step 2:
  Given the state diagram.



- Step 3: Create next state table

	Input, X	Present State $Q1_n$	Present State $Q0_n$	Next State $Q1_{n+1}$	Next State $Q0_{n+1}$
Count up	0	0	0	0	1
	0	0	1	1	0
	0	1	0	1	1
	0	1	1	0	0
Count down	1	0	0	1	1
	1	0	1	0	0
	1	1	0	0	1
	1	1	1	1	0

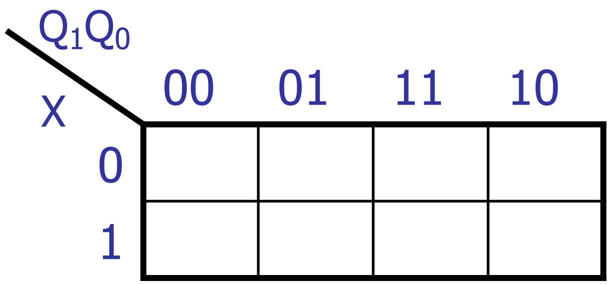
- Step 4:

  D FF transition table and determine Boolean expression.

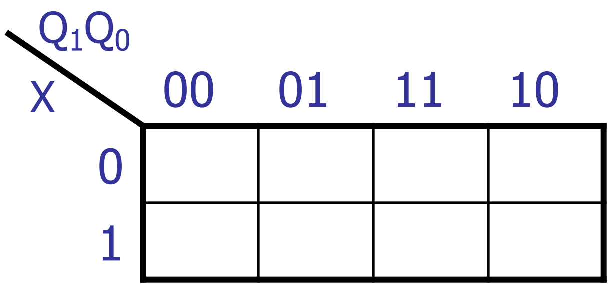
Input, X	Present State		Next State		D FF	
	$Q1_n$	$Q0_n$	$Q1_{n+1}$	$Q0_{n+1}$	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

- Step 5:

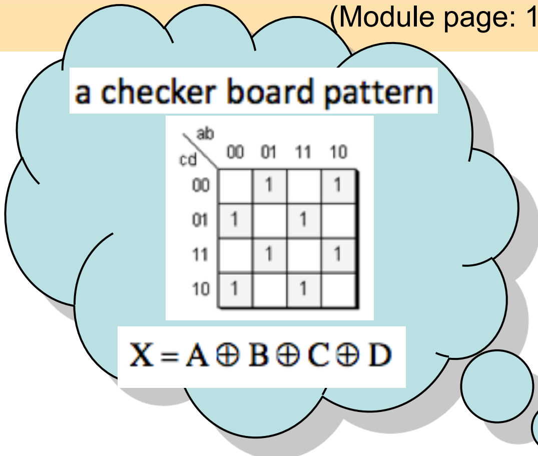
  Implement the circuit.



$D_1 =$



$D_0 =$



- **Step 4:**
  D FF transition table.

Input, X	Present State		Next State		D FF	
	$Q1_n$	$Q0_n$	$Q1_{n+1}$	$Q0_{n+1}$	D1	D0
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	1	1	1
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	1	0	0	1	0	1
1	1	1	1	0	1	0

- **Step 5:**
  Define logic equation.

X \ Q_1Q_0	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$D_1 = X \oplus Q_1 \oplus Q_0$$

X \ Q_1Q_0	00	01	11	10
0	1	0	0	1
1	1	0	0	1

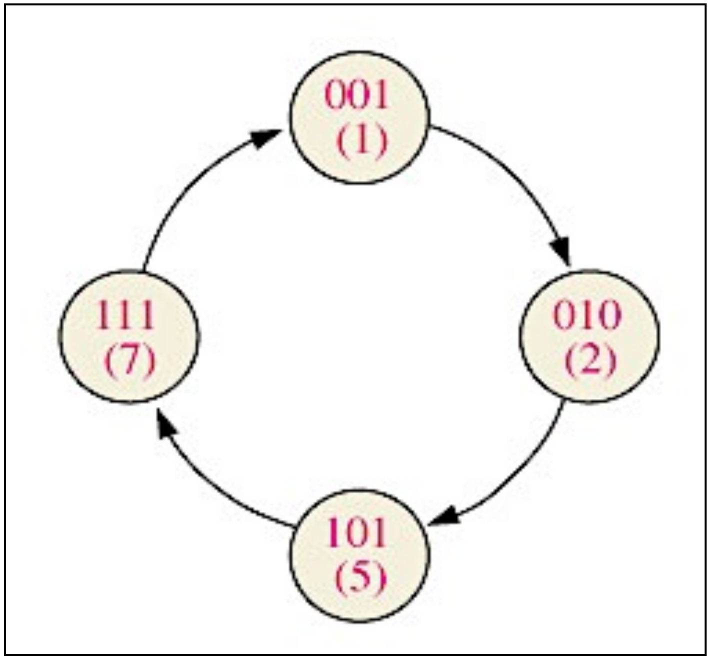
$$D_0 = \overline{Q}_0$$

Exercise 8b.9: Draw the circuit for of 2-bit up-down synchronous counter using D FF with $D_1 = X \oplus Q_1 \oplus Q_0$ and $D_0 = \overline{Q}_0$

(Refer previous example: module page 261)

Counter for Arbitrary Sequences

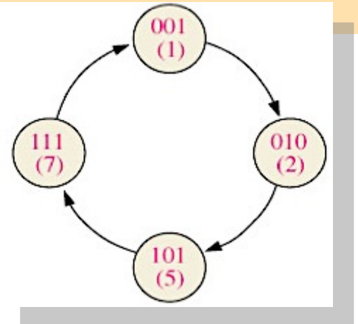
- Design the counter base on the given state diagram using T FF.



•The counter is 3-bit counter
•The total number state = $2^3 = 8$

•Only 4 state (1, 2, 5, 7)
→ **Valid State**

•Other states (0, 3, 4, 6)
→ **Invalid State**
(never occur /don't care)



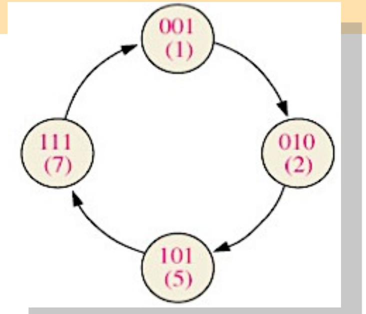
- State table and T FF transition table.

Present State			Next State			T FF		
$Q2_n$	$Q1_n$	$Q0_n$	$Q2_{n+1}$	$Q1_{n+1}$	$Q0_{n+1}$	T2	T1	T0
0	0	0	X	X	X	X	X	X
0	0	1	0	1	0	0	1	1
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

- Derive the Boolean expression and draw the circuit diagram.

**Fill in the next state and T FF transition column

Q_{n+1}	T
Q_n	0
$\overline{Q_n}$	1



- State table and T FF transition table.

FF2 FF1 FF0

Present State			Next State			T FF		
$Q2_n$	$Q1_n$	$Q0_n$	$Q2_{n+1}$	$Q1_{n+1}$	$Q0_{n+1}$	T2	T1	T0
0	0	0	X	X	X	X	X	X
0	0	1	0	1	0	0	1	1
0	1	0	1	0	1	1	1	1
0	1	1	X	X	X	X	X	X
1	0	0	X	X	X	X	X	X
1	0	1	1	1	1	0	1	0
1	1	0	X	X	X	X	X	X
1	1	1	0	0	1	1	1	0

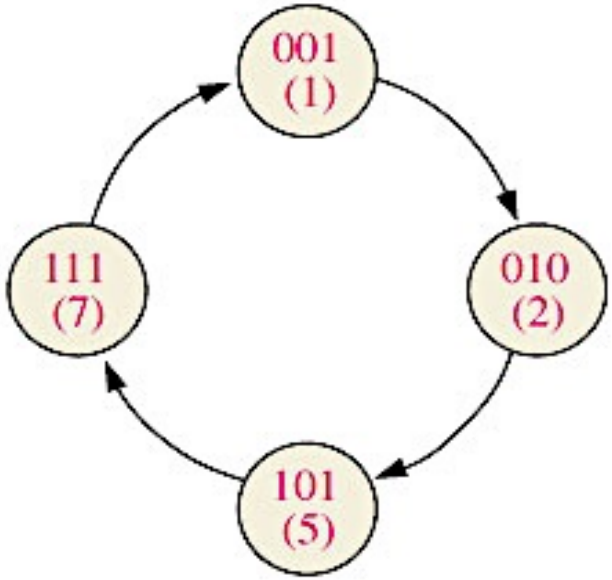
- Derive the Boolean expression and draw the circuit diagram.

**Fill in the next state and T FF transition column

Exercise 8b.10: Derive the Boolean expression and draw the circuit diagram from the previous example.

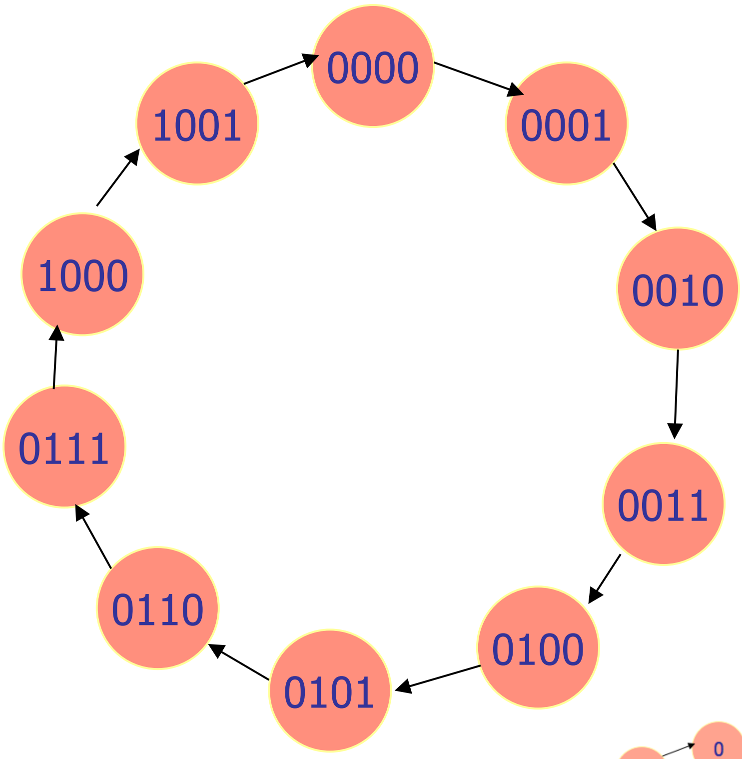
Extra

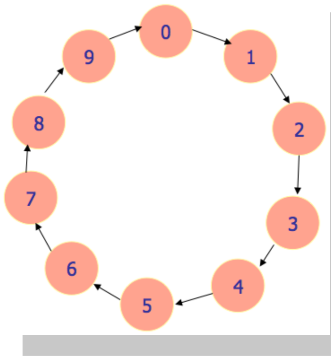
Exercise 8b.11: Design a counter with the irregular binary count sequence shown in the state diagram below using JK FF.



Synchronous BCD Decade Counter

- Synchronous decade counter counts from 0 to 9 and then recycles to 0 again.
- 4 FF is required and the unused states ie 10 to 15 are taken as don’t care terms.





**Fill in the T0 column

Present State				Next State				T FF Transition			
Q3	Q2	Q1	Q0	$Q3_+$	$Q2_+$	$Q1_+$	$Q0_+$	T3	T2	T1	T0
0	0	0	0	0	0	0	1	0	0	0	**1**
0	0	0	1	0	0	1	0	0	0	1	**1**
0	0	1	0	0	0	1	1	0	0	0	**1**
0	0	1	1	0	1	0	0	0	1	1	**1**
0	1	0	0	0	1	0	1	0	0	0	**1**
0	1	0	1	0	1	1	0	0	0	1	**1**
0	1	1	0	0	1	1	1	0	0	0	**1**
0	1	1	1	1	0	0	0	1	1	1	**1**
1	0	0	0	1	0	0	1	0	0	0	**1**
1	0	0	1	0	0	0	0	1	0	0	**1**
1	0	1	0	X	X	X	X	X	X	X	**X**
1	0	1	1	X	X	X	X	X	X	X	**X**
1	1	0	0	X	X	X	X	X	X	X	**X**
1	1	0	1	X	X	X	X	X	X	X	**X**
1	1	1	0	X	X	X	X	X	X	X	**X**
1	1	1	1	X	X	X	X	X	X	X	**X**

**Fill in the K-maps

Self-Test:

Fill in the k-map to simplify the equations.

Q3Q2 \ Q1Q0	00	01	11	10
00				
01				
11				
10				

T3 =

Q3Q2 \ Q1Q0	00	01	11	10
00				
01				
11				
10				

T2 =

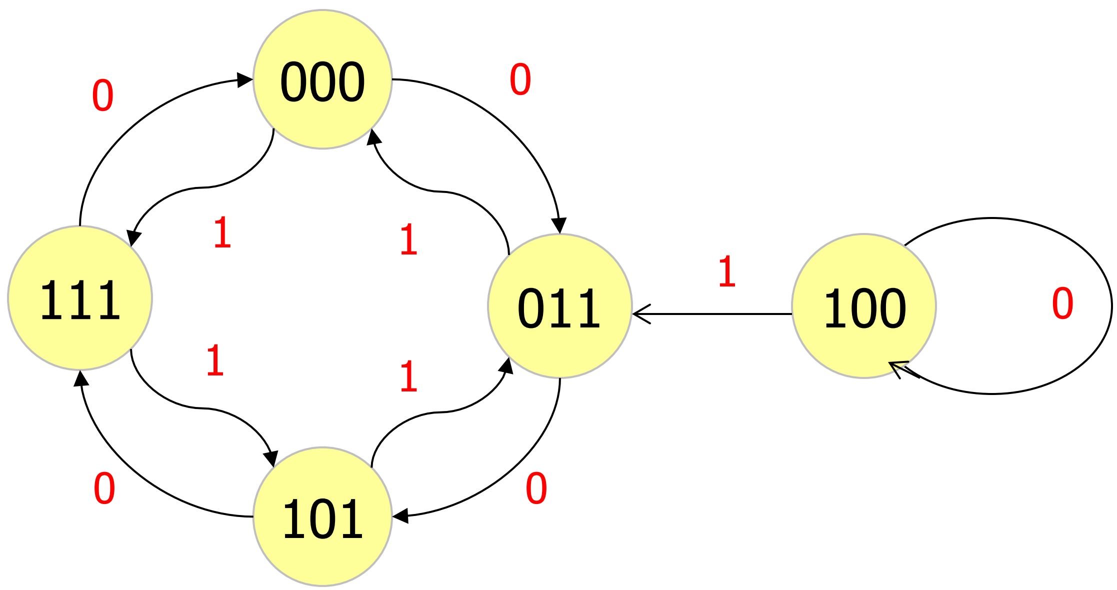
Q3Q2 \ Q1Q0	00	01	11	10
00				
01				
11				
10				

T1 =

Q3Q2 \ Q1Q0	00	01	11	10
00				
01				
11				
10				

T0 =

Exercise 8b.12: Design a synchronous counter with the irregular binary count sequence shown in the state diagram below using J-K FF.



Cascaded Counter

Recap: Modulus

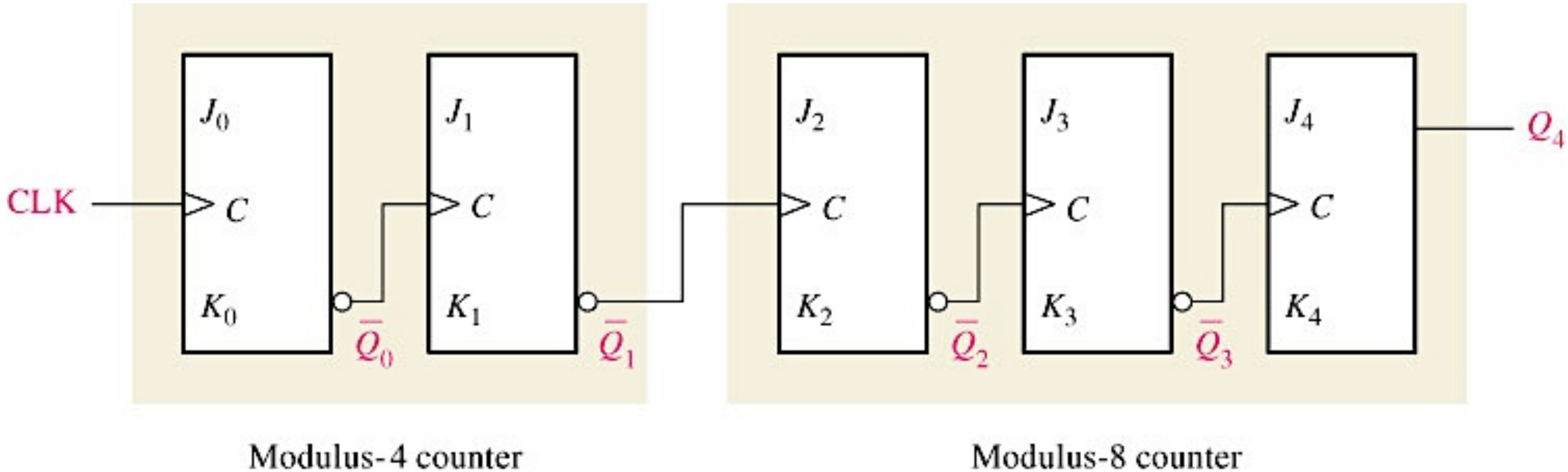
- The modulus → number of unique states through which the counter will sequence.
- Maximum possible number of states = 2^N, N is the number of flip-flops in the counter.
  - Example : Modulus 8 = 2^3 (Need 3 flip flops)
- Counter can be designed to have less number of states in their sequence → Truncated sequence.
  - One common modulus for counters → ten (Modulus 10).
  - It called BCD decade counters (as explained in previous slides).

Cascaded Counter

- Counter can be connected to achieve higher modulus operation.
- Cascading means that the last-stage output of one counter drives the input of the next counter.

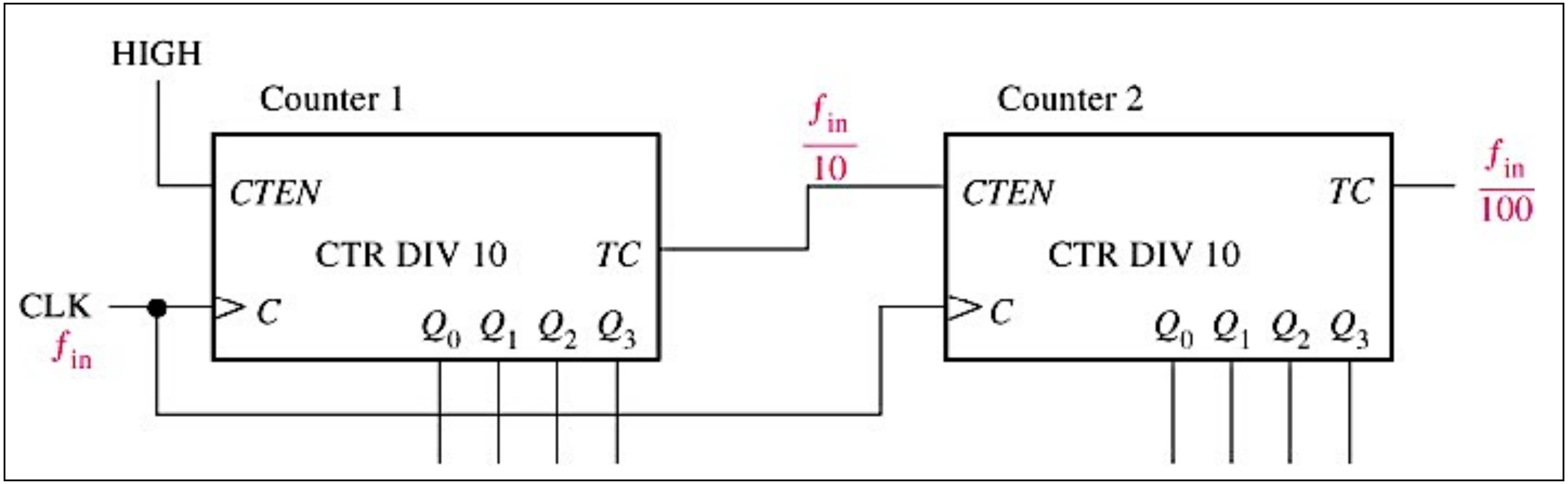
Example:

- Two counters, modulus-4 and modulus-8 connected in cascade, can achieve count until 32 CLK (modulus-32). (i.e 4 x 8)



Cascaded Counter:
Modulus-100 Counter

- Modulus-100 counter using 2 cascaded decade counters.
- This counter can be viewed as a frequency divider.
- It divides the input clock frequency by 100.

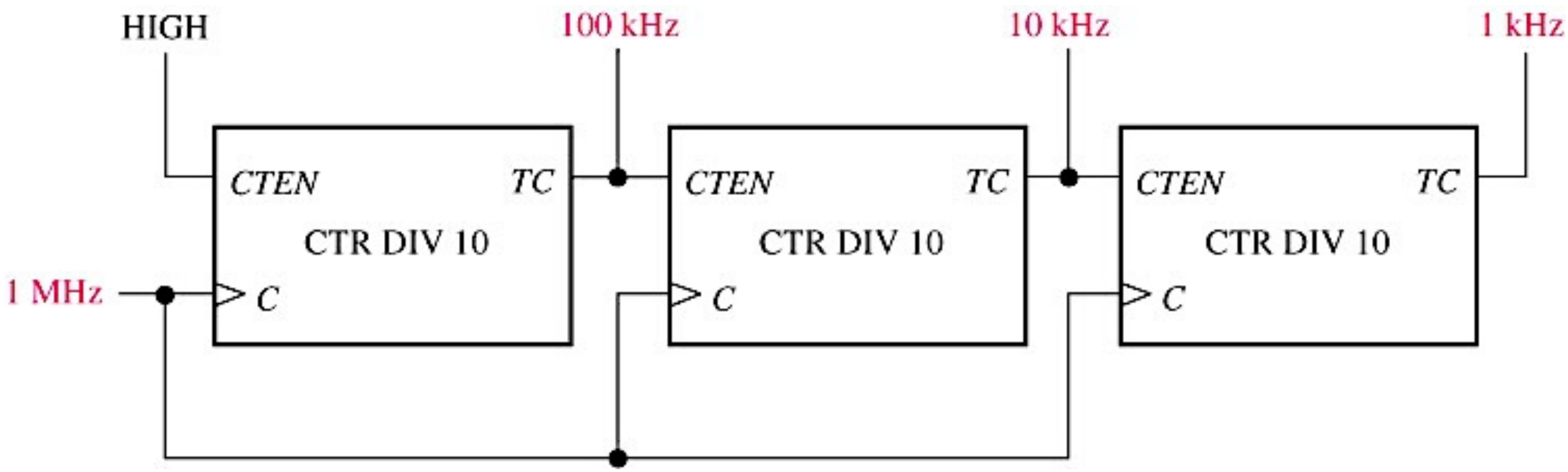


(Total MOD = 10 x 10 = 100)

Cascaded Counter:

Modulus-1000 Counter

- Three cascaded decade counters forming a divide-by-1000 frequency divider.



Basis clock frequency of 1 MHz and you wish to obtain 100kHz, 10Hz, and 1kHz, a series of cascaded decade counters can be used. If 1 MHz signal is divided by 10, the output is 100kHz. Then if the 100 kHz signal is divided by 10, the output is 10kHz. Further division by 10 gives the 1 kHz frequency.

Total MOD = 10 x 10 x 10
= 1000

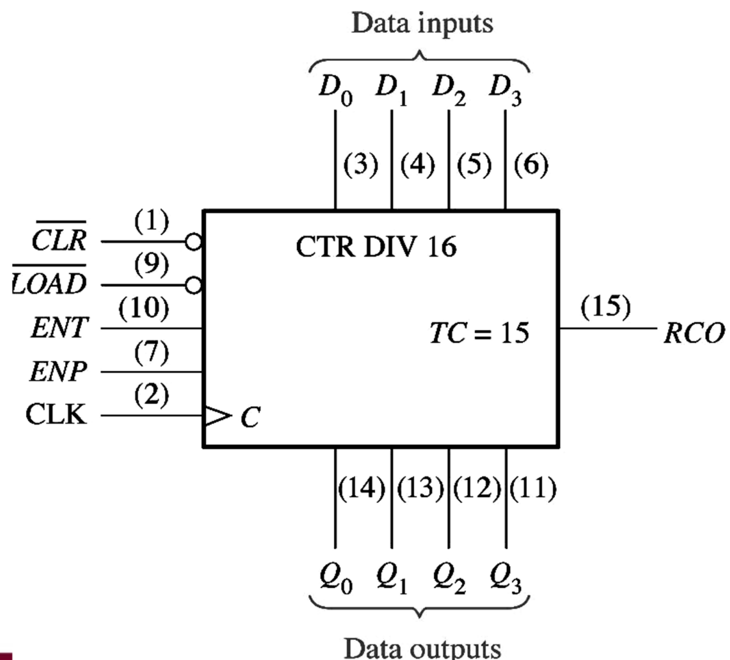
Extra

Exercise 8b.13: Two type of counters, modulus-4 and modulus-8 need to be used to achieve count up to modulus-*n* (*n* CLK).

a) How to cascade the counters to achieve count until 32 CLK (modulus-32)?
b) What is the frequency produced by each counter given an initial frequency as 800MHz?

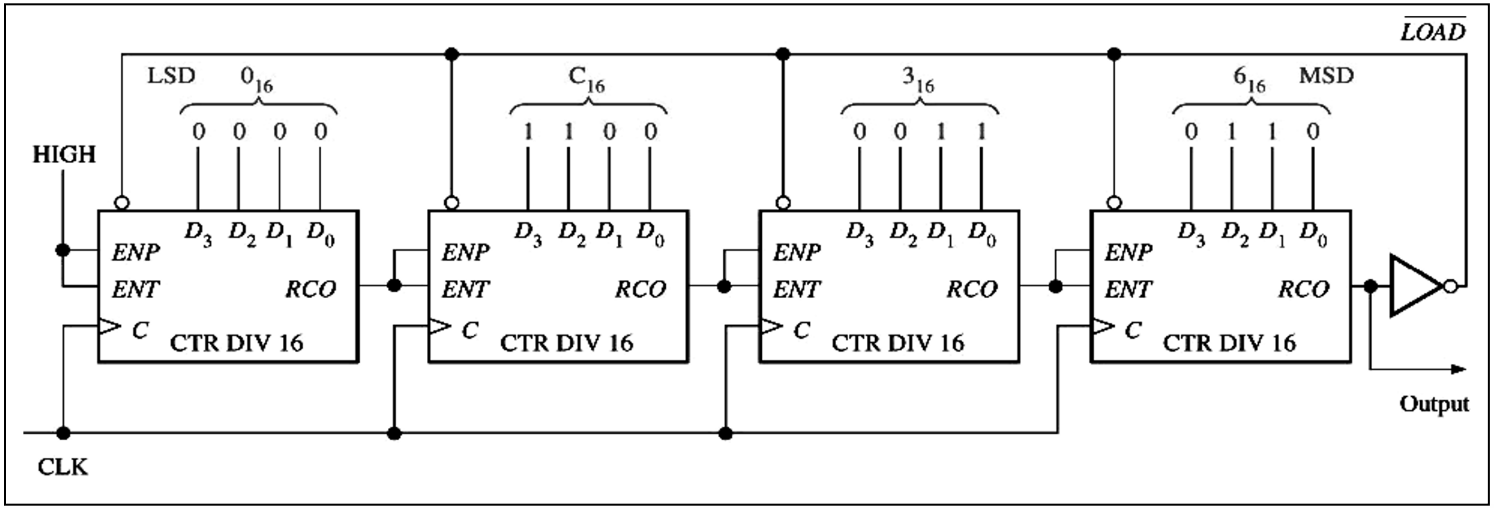
74HC163: 4-Bit Synchronous Binary Counter

- There is a dedicated counter IC, e.g 74HC163 which is a MOD 16 counter IC
- The starting counting sequence can be change by setting the initial value at $D_3D_2D_1D_0$
  - To load the initial value, LOAD' must be 0



Cascaded Counter with Truncated Sequence

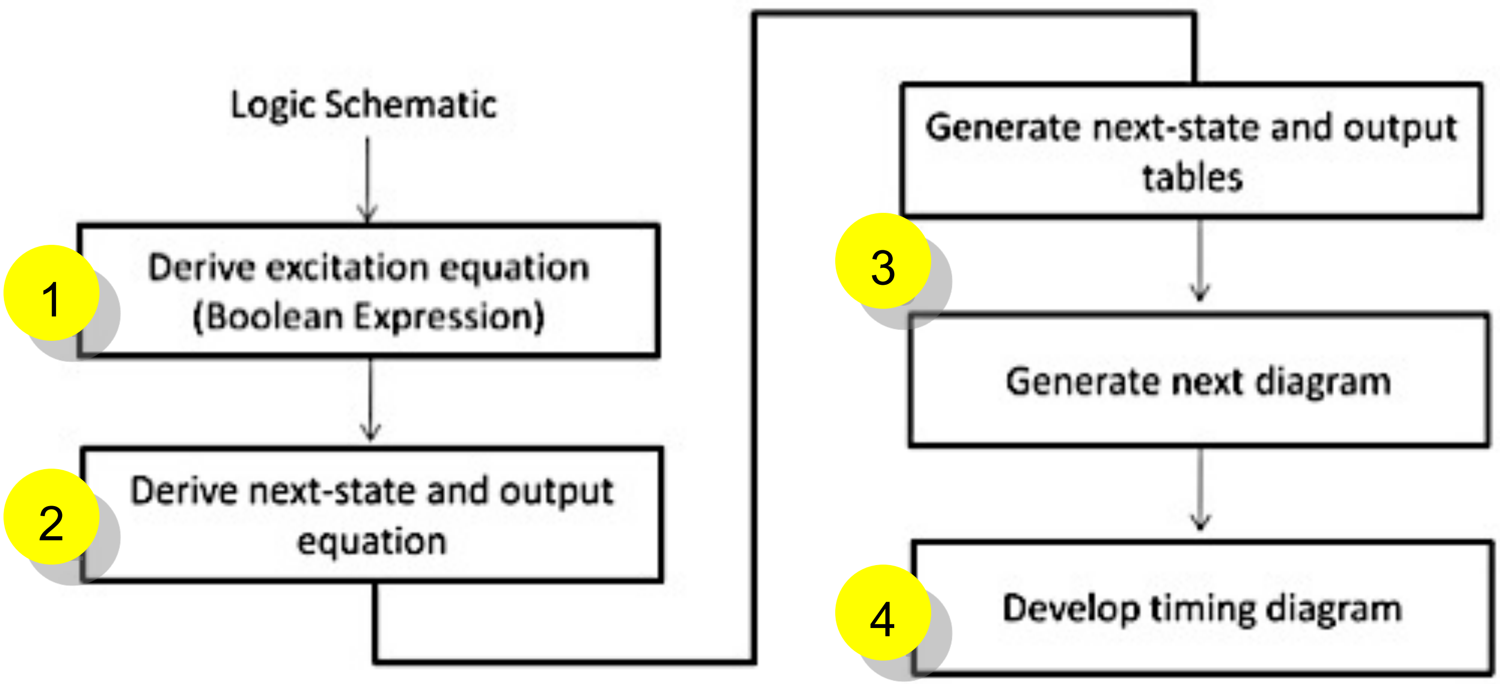
- The cascaded counter below has 16^4 = 65,536 states (full modulus for four cascaded CTR DIV 16).
- If we need a modulus 40,000 counter only. So, how?
  1. Determine the initial value : 65536-40000 = 25536 ($63C0_{16}$) make the counter starts at this count.
  2. Therefore preset the cascaded counter to $63C0_{16}$ by setting the value of $D_3D_2D_1D_0$ as shown below.



Analysis of Sequential Circuits

Analysis of Sequential Circuits

- Behavior of a sequential circuit is determined from the inputs, the outputs and the states of its flip-flops.
- Both the output and the next state are a function of the inputs and the present state.



- Step 1:
  Start with the logic schematic from which we can derive **excitation equations** for each flip-flop input.

- Step 2:
  To obtain **next-state equations**, we insert the excitation equations into the characteristic equations. The **output equations** can be derived from the schematic:

Flip-flop characteristic equation:

$$\text{active HIGH SR}: Q_{next} = S + \overline{R}Q,\ SR = 0$$
$$JK: Q_{next} = J\overline{Q} + \overline{K}Q$$
$$D: Q_{next} = D$$
$$T: Q_{next} = T\overline{Q} + \overline{T}Q$$

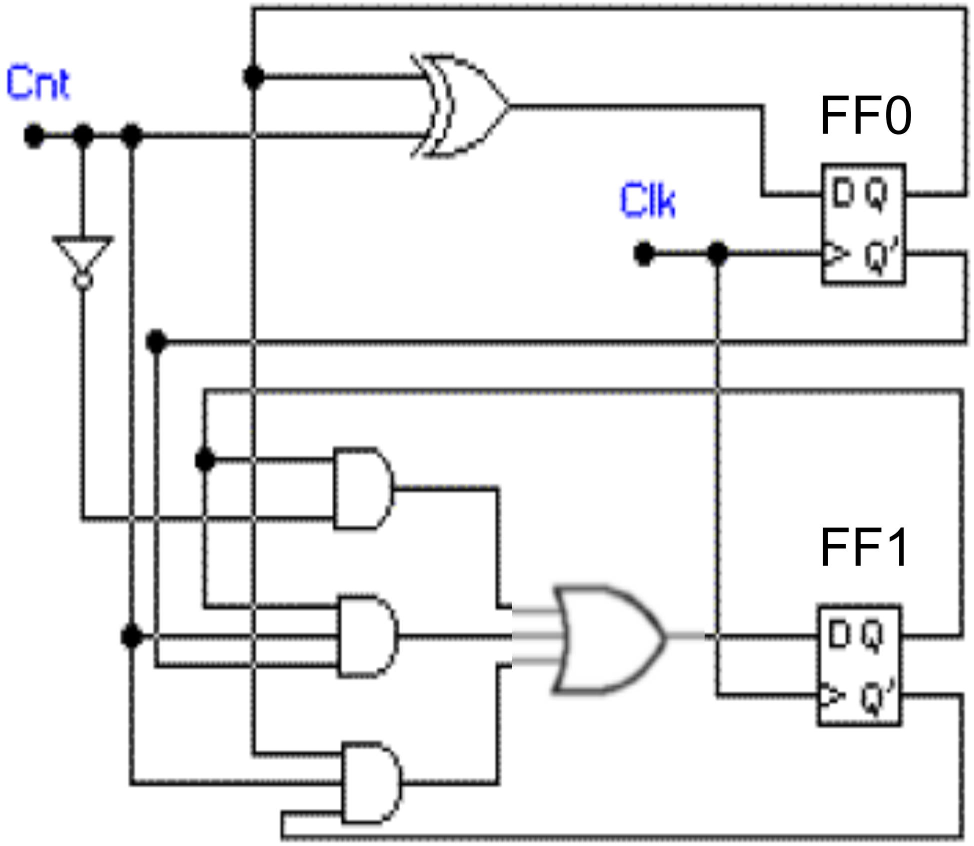
- Step 3:
  Once we have our output and next-state equations, we can generate the **next-state and output tables** as well as **state diagrams**.

- Step 4:
  When we reach this stage, we use either the table or the state diagram to develop a **timing diagram** which can be verified through simulation.

Method 1: Modulo-4 Counter

Example:

Derive the state table and state diagram for the sequential circuit below. Use Method 1



$$\begin{aligned} \text{active HIGH SR}: Q_{next} &= S + \overline{R}Q,\ SR = 0 \\ JK: Q_{next} &= J\overline{Q} + \overline{K}Q \\ D: Q_{next} &= D \\ T: Q_{next} &= T\overline{Q} + \overline{T}Q \end{aligned}$$

- Step 1: **Boolean expressions** for the inputs of each flip-flops in the schematic.

$$D_0 = Cnt \oplus Q_0 = \overline{Cnt} \bullet Q_0 + Cnt \bullet \overline{Q}_0$$

$$D_1 = \overline{Cnt} \bullet Q_1 + Cnt \bullet \overline{Q}_1 \bullet Q_0 + Cnt \bullet Q_1 \bullet Q_0$$

- Step 2: Derive the **next-state equations** by converting these excitation equations into flip-flop characteristic equations. In the case of D flip-flops, $Q_+ = D$.

$$Q_{0+} = D_0 = Cnt \oplus Q_0 = \overline{Cnt} \bullet Q_0 + Cnt \bullet \overline{Q}_0$$

$$Q_{1+} = D_1 = \overline{Cnt} \bullet Q_1 + Cnt \bullet \overline{Q}_1 \bullet Q_0 + Cnt \bullet Q_1 \bullet Q_0$$

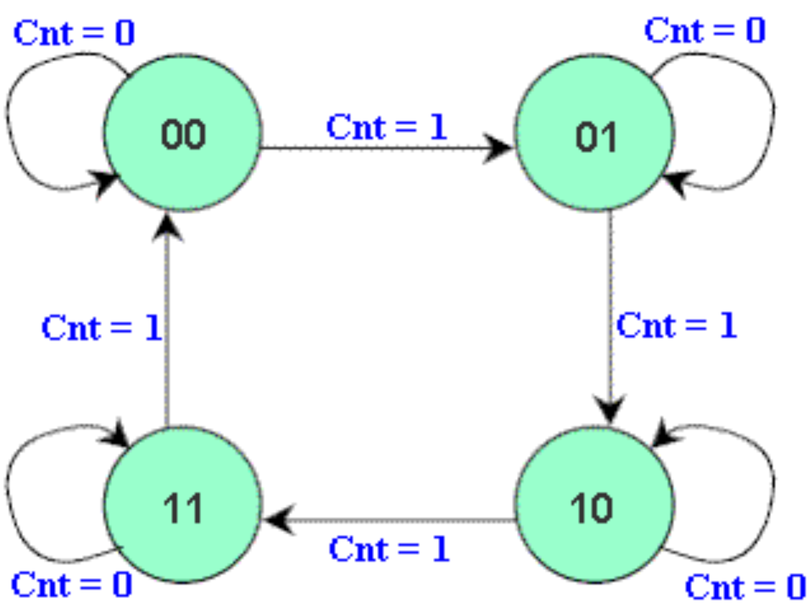
$$Q_{0+} = D_0 = Cnt \oplus Q_0 = \overline{Cnt} \bullet Q_0 + Cnt \bullet \overline{Q}_0$$

$$Q_{1+} = D_1 = \overline{Cnt} \bullet Q_1 + Cnt \bullet \overline{Q}_1 \bullet Q_0 + Cnt \bullet Q_1 \bullet Q_0$$

- Step 3:
  Construct the **next-state table**.

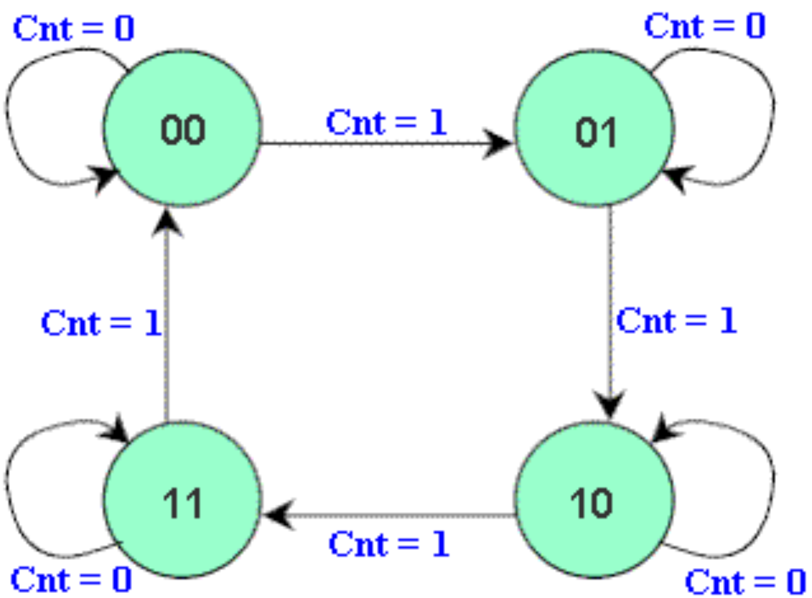
Input, Cnt	Present State		Next State	
	Q_1	Q_0	$Q_{1+} = D_1$	$Q_{0+} = D_0$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

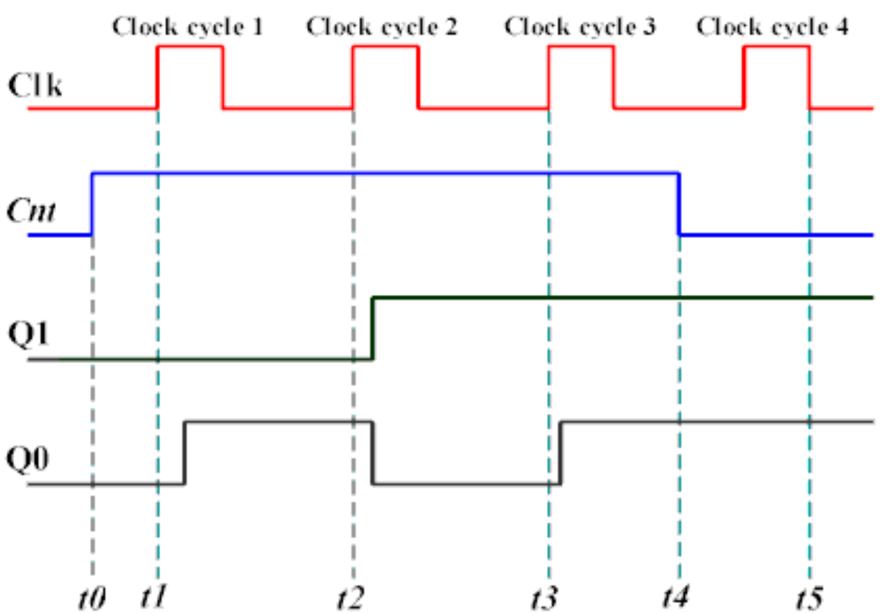
- Step 4:
- The **state diagram** is generated directly from the next-state table.

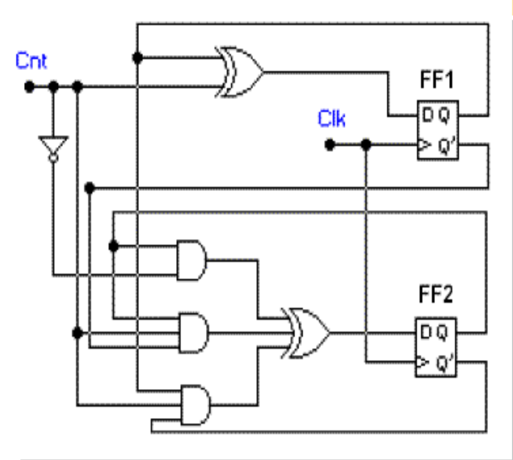


Input, Cnt	Present State		Next State	
	Q_1	Q_0	$Q_{1+} = D_1$	$Q_{0+} = D_0$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

- Step 4:
- The **state diagram** is generated directly from the next-state table.
- Next get the **timing diagram**







We can conclude:

a) From the counter circuit:

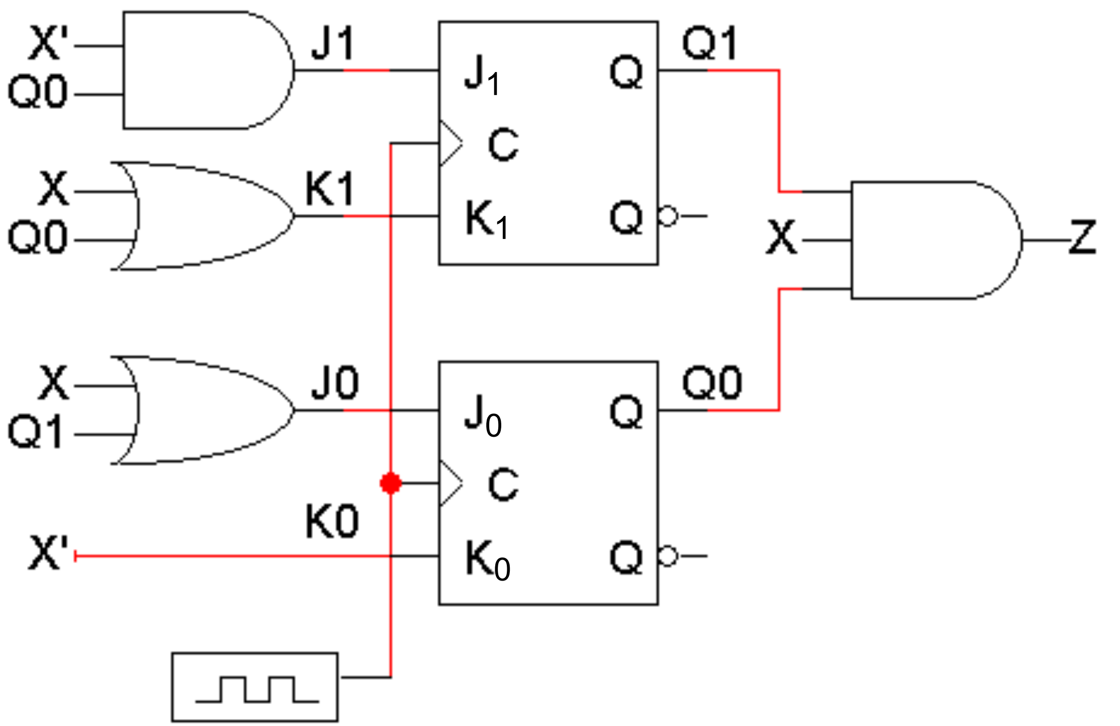
- 2- bit counter because there are 2 FFs in the design.
- Sycnhronous counter because the FFs have a common clock.

b) From the counter state diagram:

- MOD 4 because has 4 state (i.e. $2^2=4$), not a truncated counter.
- Count Up counter when Cnt=1, and stay in the previous state when Cnt=0.

Method 2: JK Circuit Analysis

- Sequential circuit with two JK flip-flops. There is one input, X, and one output, Z. Use Method 2



$J_1 = X' Q_0$ $J_0 = X + Q_1$ $Z = Q_1 Q_0 X$

$K_1 = X + Q_0$ $K_0 = X'$

$J_1 = X' Q_0$ $J_0 = X + Q_1$ $Z = Q_1 Q_0 X$

$K_1 = X + Q_0$ $K_0 = X'$

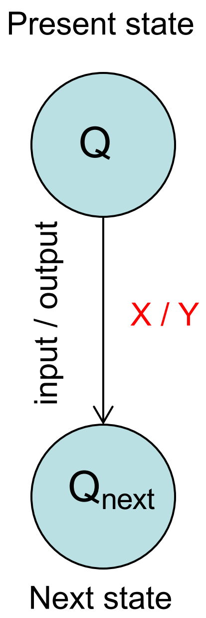
Input, X	Present State		Next State		JK FF Transition				Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	J_1	K_1	J_0	K_0	
0	0	0			0	0	0	1	0
0	0	1			1	1	0	1	0
0	1	0			0	0	1	1	0
0	1	1			1	1	1	1	0
1	0	0			0	1	1	0	0
1	0	1			0	1	1	0	0
1	1	0			0	1	1	0	0
1	1	1			0	1	1	0	1

**Fill in the JK FF transition column

Input, X	Present State		Next State		JK FF Transition				Output, Z
	Q_1	Q_0	Q_{1+}	Q_{0+}	J_1	K_1	J_0	K_0	
0	0	0	0	0	0	0	0	1	0
0	0	1	1	0	1	1	0	1	0
0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	1	0	0
1	1	0	0	1	0	1	1	0	0
1	1	1	0	1	0	1	1	0	1

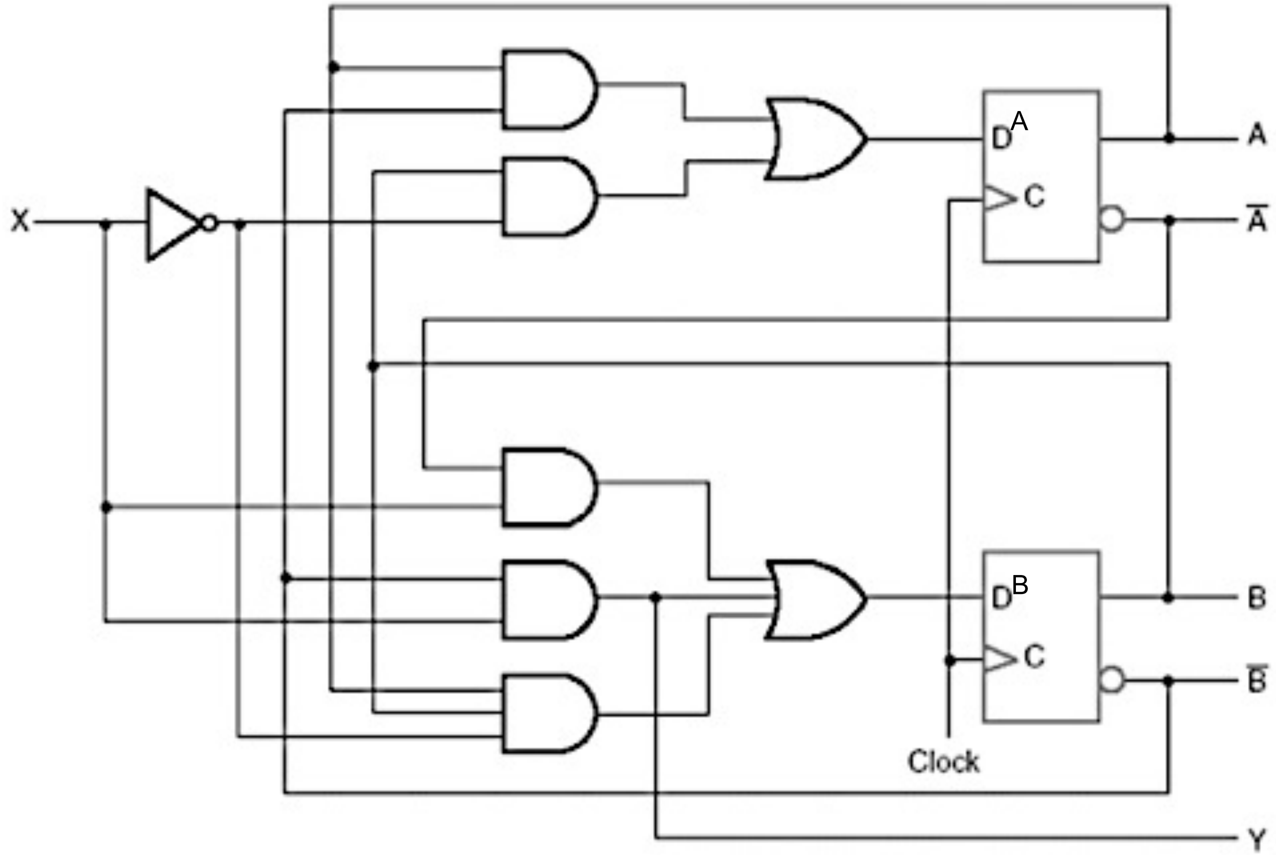
**Fill in the next state column

Draw the state diagram for the example in previous slide.



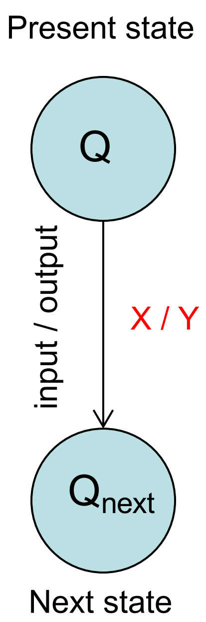
Extra

Exercise 8b.15: Analysis for the following sequential circuit. Use Method 1.



Exercise 8b.15: Draw the state diagram for the example in previous slide.

Extra



Input, X	Present State		Next State		Output, Y
	A	B	A_+	B_+	
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	0	1	1
1	0	1	0	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Exercise 8b.16:

Derive the state table and state diagram for the sequential circuit below. Use Method 2