UNIVERSITI TEKNOLOGI MALAYSIA

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SCSR1013 DIGITAL LOGIC

MODULE 8a: COUNTERS (INTRO & ASYNC)

2013/2014-1

FACULTY OF COMPUTING

Module Content

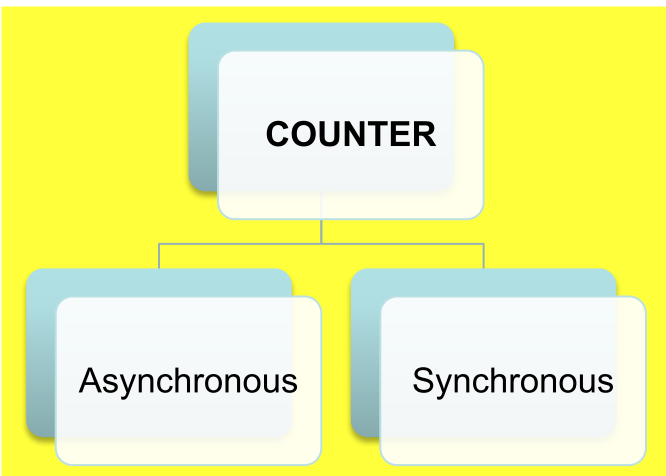
- ASYNCHRONOUS COUNTER
  - 2 bit / 3 bit / 4 bit / BCD Decade
- SYNCHRONOUS COUNTER
  - 2 bit / 3 bit /4 bit / BCD Decade
- UP/DOWN COUNTER
- CASCADED COUNTER
- DESIGN THE SYNCHRONOUS COUNTER
- COUNTER DECODING

The objectives of this module are:

1. To distinguish the different between synchronous and asynchronous counters.
2. To illustrate the designing of counters .
3. To explain the application of counters.
4. To demonstrate the analysis of sequential circuits.

Introduction

- There is a variety of counters based on its construction.
- Counter is type of sequential logic circuit.
- In general, two categories of counters:



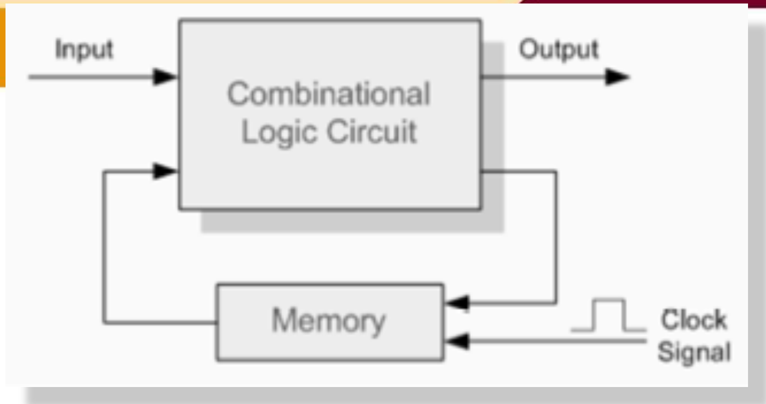
Both categories can be differentiated by criterion:

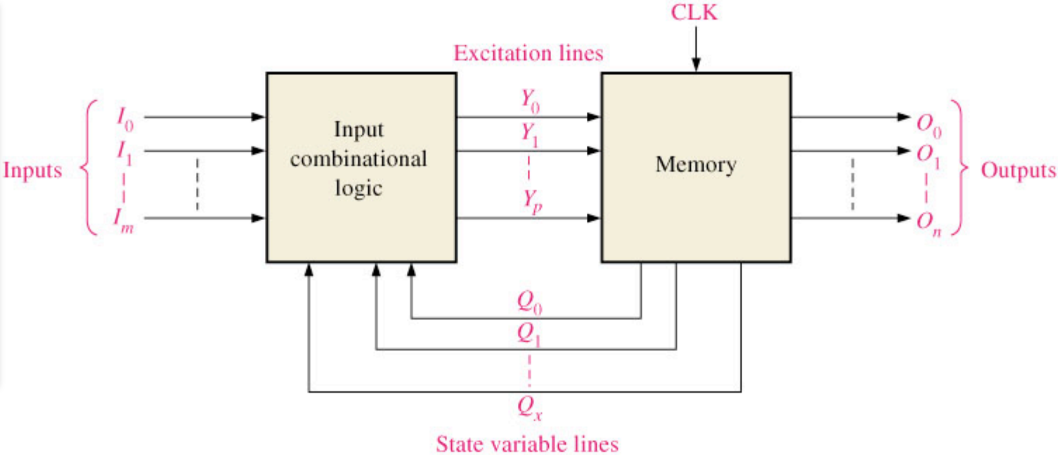
1. Clock Trigger: Positive edged or Negative edged
2. Counts: Binary, Decade
3. Count Direction: Up, Down, or Up/Down

In the previous lectures, the characteristic of S-R, D, J-K and T flip-flops were discussed. These flip-flops can be connected together to perform certain operations.

In the following lectures, we will use these flip-flops to construct a variety of counters. In addition we will also learned the method for analysing the different types of counters.

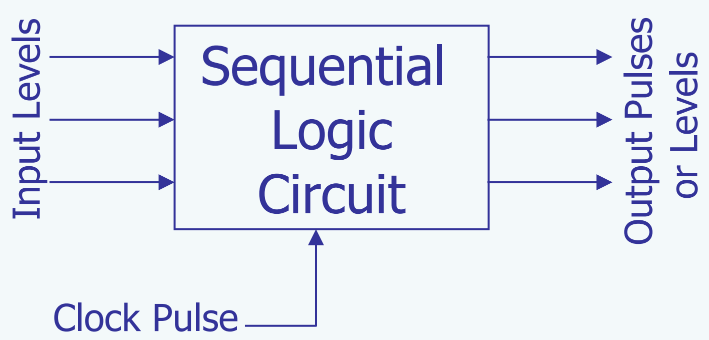
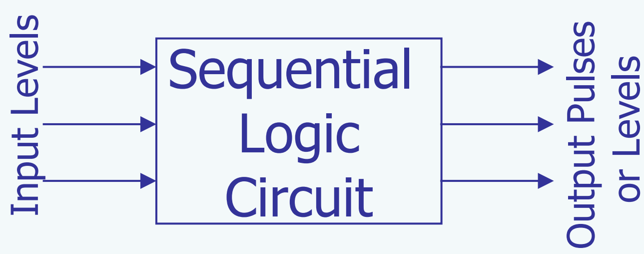
Recap: Sequential Circuit





- General sequential circuit that consists of a combinational logic section and a memory section → flip-flops.
- **Memory** elements are devices capable of **storing binary information**.
- Binary information stored **at any given time** defines the state of the sequential circuit.
- The input and the present state of the memory element determines the output.
- A sequential circuit is specified by a time sequence of inputs, outputs, and internal states.

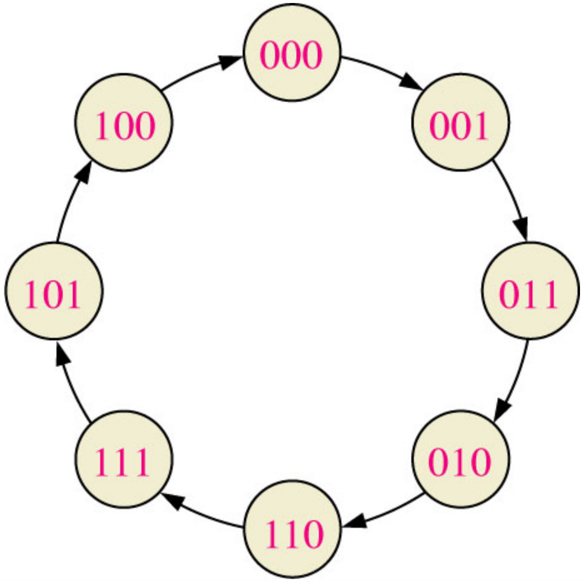
Types of Sequential Circuits

Synchronous	Asynchronous
Use **clock** inputs to synchronize the circuit operation.	Circuit operation is based on a message (**signal**) passing from one stage(e.g. Circuit) to another.
	

Introduction:
Counters

- A **counter** → Any sequential circuit that goes through a prescribed **sequence of states** upon the application of **input pulses**.

- The **sequence of states** in a counter may follow a binary count or any other sequence.



- The states changed by the **input pulse;**
- the input pulses (count pulses) may be clock pulses or they may originate from an external source; may occur at prescribed intervals of time or at random.

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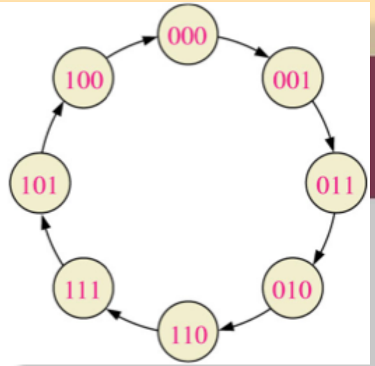
Counters :

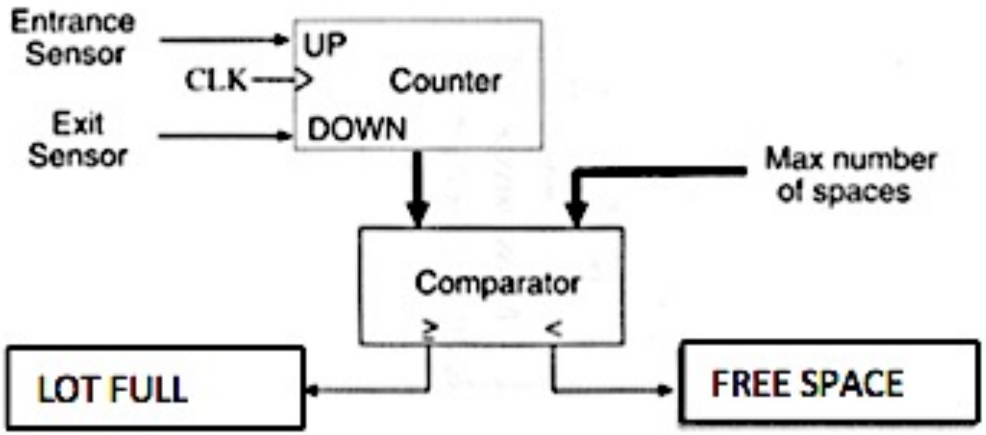
- are generally made up of flip-flops and logic gates.
- can retain an output state after the input condition which brought about that state has been removed.
- classified as sequential circuits.
- can have many more than two states
  - value of a state is expressed as a *multidigit binary number*, whose `1's and `0's are usually derived from the outputs of internal flip-flops that make up the counter.
- The states number is limited only by the amount of electronic hardware that available.



- Main types of flip-flops used:
  - J-K flip-flops, T flip-flops or D flip-flops.

Uses of Counters

- To count the number of times that a certain event takes place; the occurrence of event to be counted is represented by the input signal to the counter (see figure below).



- To control a fixed sequence of actions in a digital system
  - e.g gate A must be open before gate B.
- To generate timing signals
  - e.g a bomb can only be detonated 20 second after a button is pressed

There are many devices used that can tell the time without having to be manually programmed

- To generate clocks of different frequencies.
  - By dividing the frequency, we can get a different clock frequencies from the same source

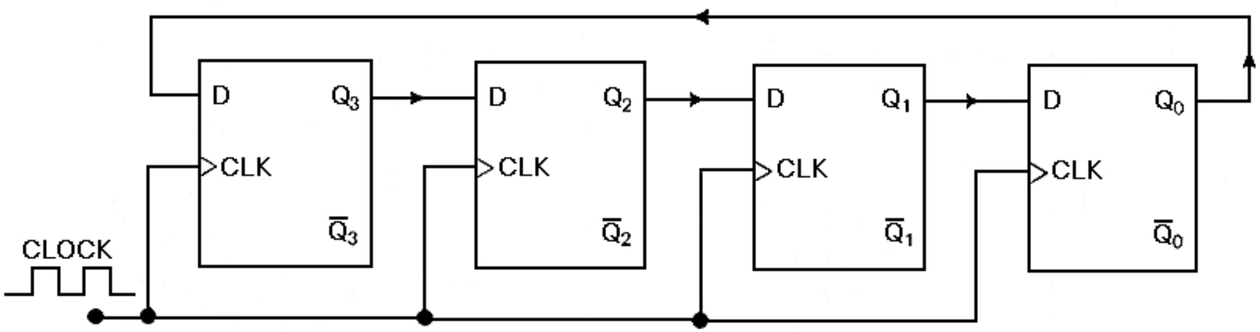
Characteristic of Counter

- Counter can be described by the following characteristics:
  1. Asynchronous or synchronous
  2. Counting sequence
  3. Modulus (MOD)
  4. Whether the counter repeat the counting sequence

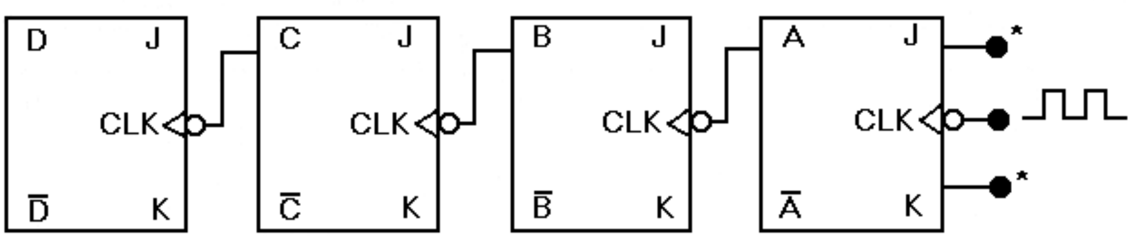
Counters: Characteristics

1. Asynchronous / Synchronous

- Whether the clock come from the same source or not
  - Synchronous – all clock from the same source
  - Asynchronous – clock for each flip-flop comes from a different source



Synchronous Counter



Asynchronous Counter

* All J and K inputs assumed to be at logic 1.

2. Counting Sequence: Up | Down | Up-Down

- Up or Down – unidirectional – the count sequence only one way
- Up-Down – bidirectional – the direction of the count can be change during operation

- Because of limited word length, the count sequence is limited.
  - For an *n*-bit counter, the range of the count is [0, 2^n-1].
  - The count sequence usually repeats itself.

- When **counting up**, the count sequence goes in this manner: 0, 1, 2, … 2^n-2, 2^n-1, 0, 1, …etc.

- When **counting down** the count sequence goes in the same manner: 2^n-1, 2^n-2, … 2, 1, 0, 2^n-1, 2^n-2, … etc.

3-bit Up Counter	3-bit Down Counter
000	000
001	111
010	110
011	101
100	100
101	011
110	010
111	001

- The **complement** of the count sequence counts in reverse direction:

- If the counter output counts up, the complement output counts down.

- If the counter output counts down, the complement output counts up.

3-bit Up Counter	Complement of the Count
000	111
001	110
010	101
011	100
100	011
101	010
110	001
111	000

3. Modulus (MOD):

- Modulus (MOD): the number of state that the counter can have.
  - e.g. MOD 4 (4 states with the following state 0,1,2,3), MOD 9 (0,1,2,...,8).
  - the maximum count usually $2^N - 1$, where N is the number of the FF, or for the truncated sequence the max count will be $< 2^N - 1$.

  E.g. MOD 9 (0,1,2,...,8) is truncated sequence.

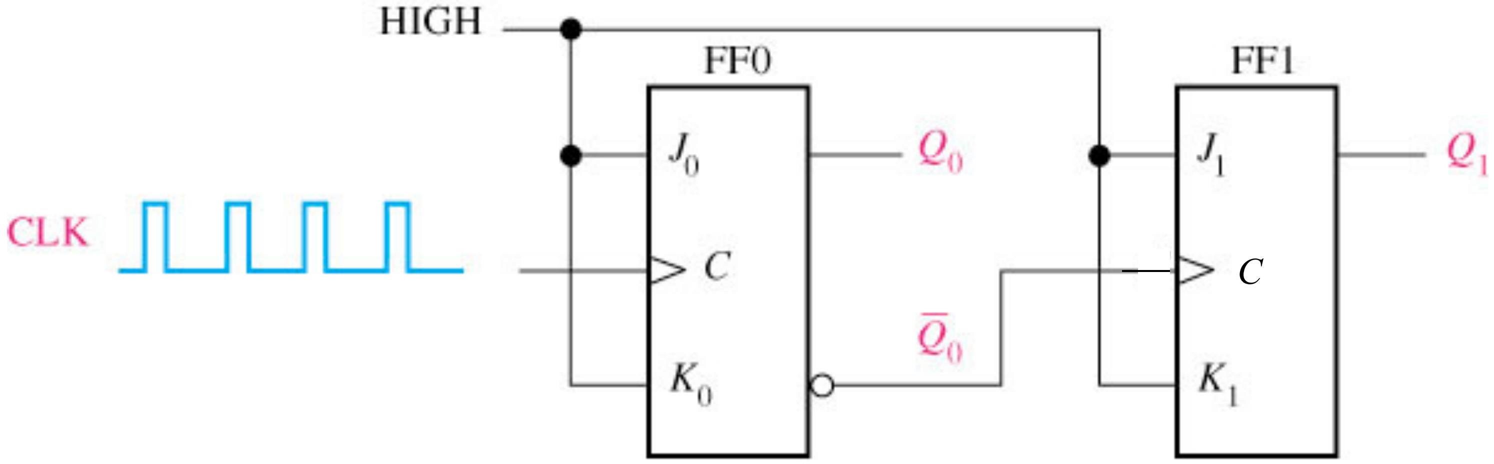
4. Repeat of Counting Sequence:

- Whether the counter repeat the counting sequence:
  - Recycle – if the counter goes back to the first count after the maximum count
  - Saturated – the counter repeat the maximum count if count up or repeat the minimum if count down

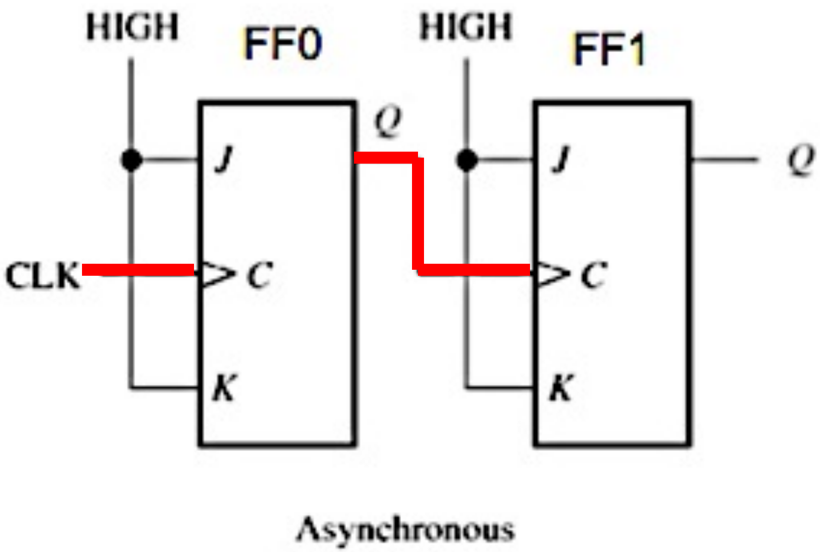
Asynchronous Counters

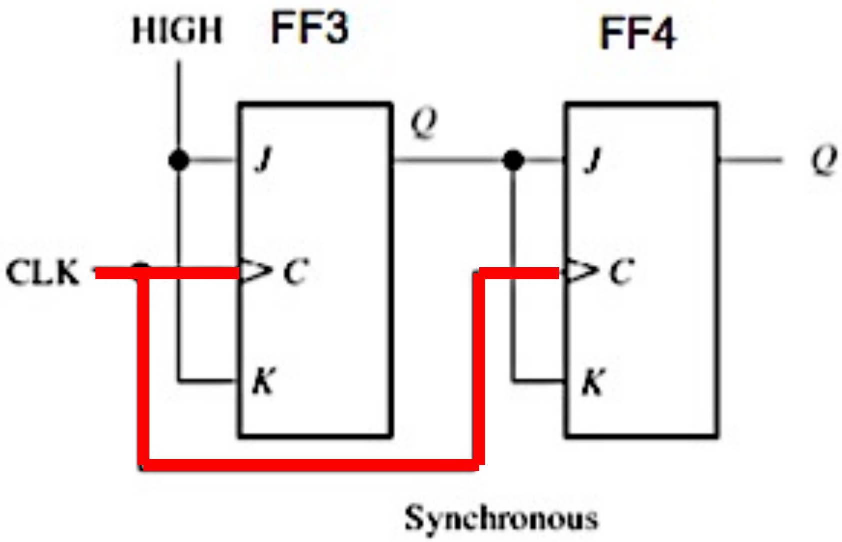
Asynchronous Counter (AC)

- An AC is one in which the flip-flop (ff) within the counter do not change states at exactly the same time because they do not have a common clock pulse.
- The **clock input** of an AC is always connected only to the LSB ff
- An AC also known as **ripple counter** – message (signal) passing or propagation delay.



- Comparison of asynchronous & synchronous.
- See the different clock connection !





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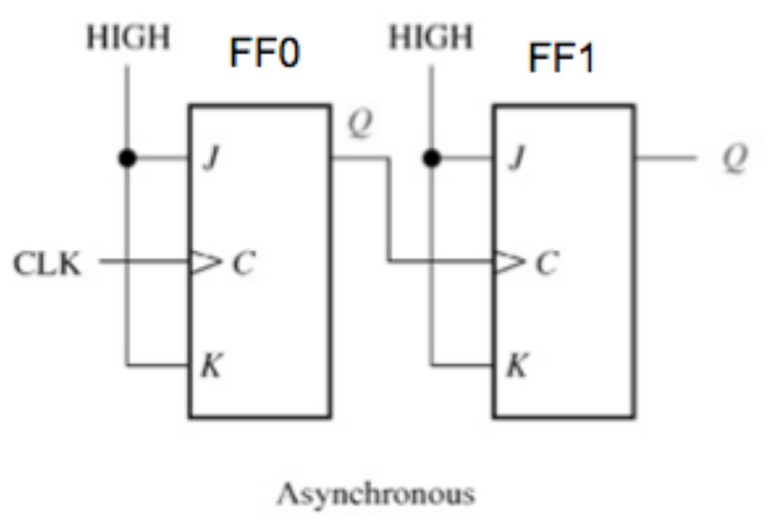


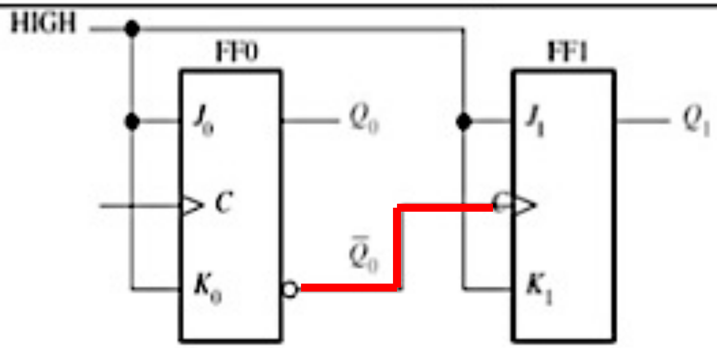
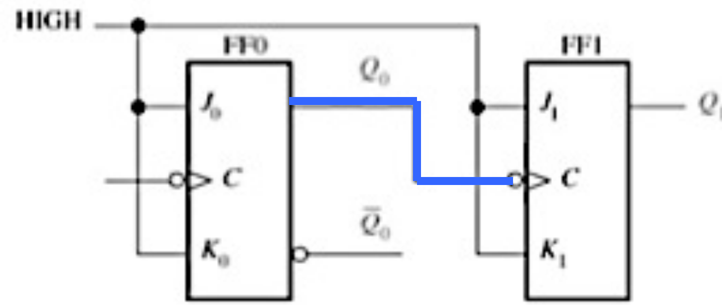
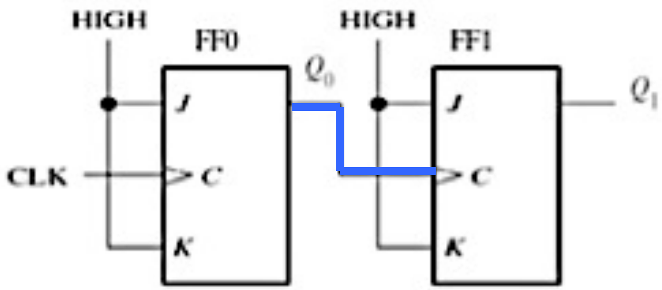
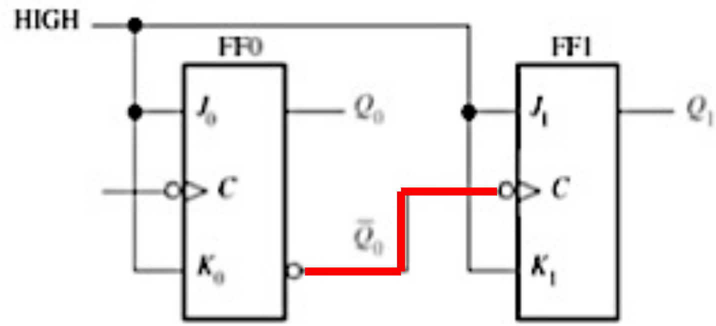
Asynchronous counter operation:

- The external clock is connected to the clock input of the first flip-flop (FF0) only.
- So, FF0 changes state at **positive edge** of each clock pulse, but FF1 changes only when triggered by the positive edge of the Q output of FF0.
- Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF0 can never occur at exactly the same time.
- Therefore, the flip-flops cannot be triggered simultaneously, producing an **Asynchronous operation**

This asynchronous counter is slow because the cascaded clocking scheme

- The clock source ripples from stage-to-stage
- The ripple effect is similar to that of a ripple carry adder circuit

Generalization of an Asynchronous Counter

	Positive Edge	Negative Edge
Count Up		
Count Down		

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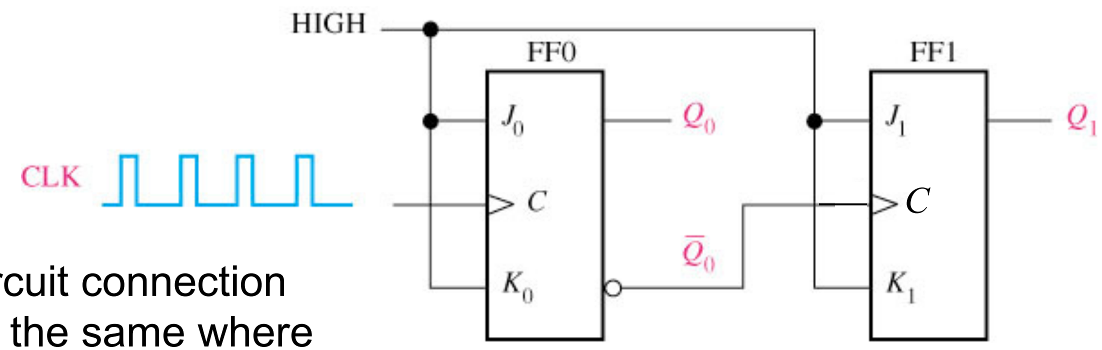
Summary of Asynchronous Counter:

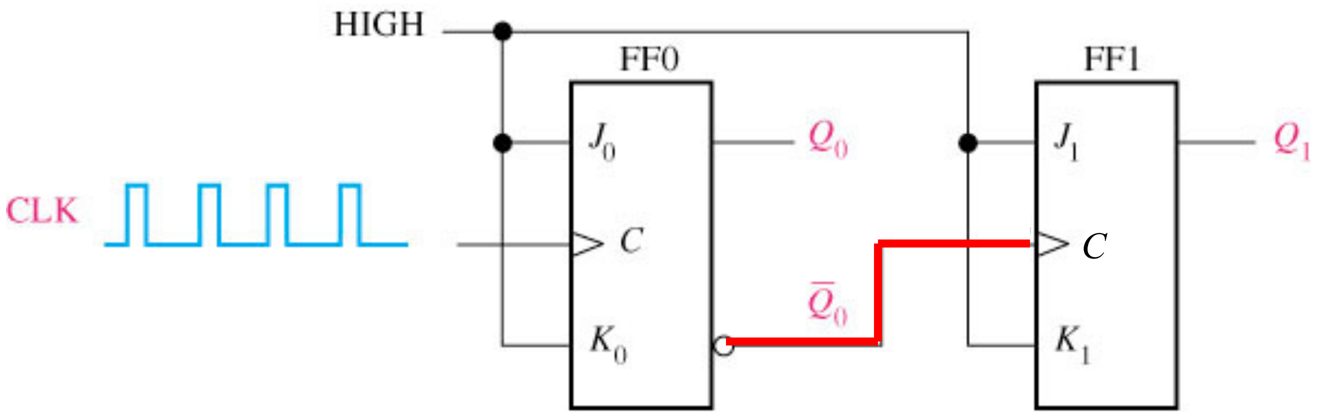


1. The circuit connection almost the same where external clock connected to LSB Flip Flop (FF)

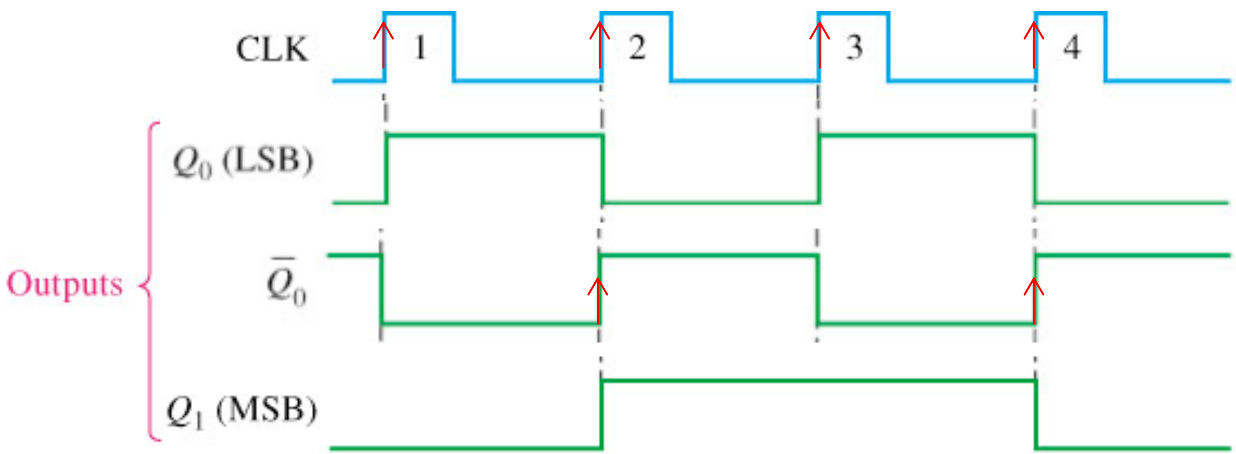
2. Clock for each FF come from the previous FF, except for the first FF (i.e. FF0)

3. Every FF operates in Toggle mode (i.e. next output is a complement of the previous output).
   - To operate in toggle mod : **for RS:** R=Q' and S= Q, **for JK :** J =K=1, **for D:** D= Q', **for T:** T =1
4. The design connection is the same , if we want more bits just add more flip-flops.
5. The difference in connection will be determine whether we want to count UP or DOWN and by using which type of flip-flop – positive edge or negative edge.

Count Up 2-bit AC



- Positive edge
- Assume that Q_0 initially LOW



- Output of Q_0 is based on CLK
- Output of Q1 is based on $\overline{Q0}$

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Notice:

1. Input JK for each FF is tied up together. Therefore J=K=1. In other word, the JK FF function in a Toggle mode i.e. every clock pulse Q will be complemented.
2. The clock of FF1 come from the complemented output of FF0, $\overline{Q_0}$
3. For FF0, every positive edge of the clock the output, Q_0 will toggle.
4. For FF1, the clock depend on $\overline{Q_0}$ and the output Q_1 will only toggle on the positive edge of $\overline{Q_0}$
5. The output of the circuit counter is read $Q_1 Q_0$

MSB LSB

CLOCK PULSE	$Q_{1(MSB)}$ (Bit 2)	Q_0 (LSB) (Bit 1)
Initially	0	0
1	0	1
2	1	0
3	1	1
4	0	0

Clock pulse 4:
Recycles

The transition of the counter from its final state → original state

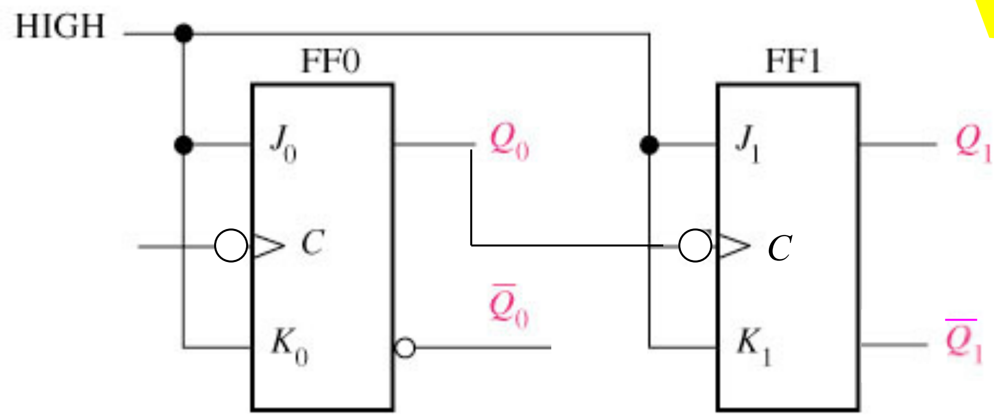
The 2-bit ripple counter circuit above has four different states, each one corresponding to a count value. Similarly, a counter with *n* flip-flops can have 2^n states. The number of states in a counter is known as its MOD (modulo). Thus a 2-bit counter is a mod-4 counter.

Exercise 8a.1: A 2-bit count up ripple counter is designed using J-K flip-flop with negative edge triggered clock.

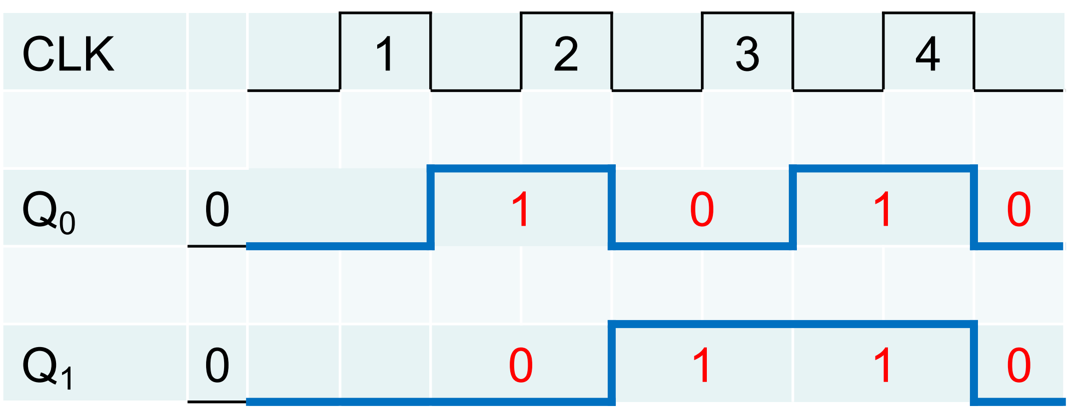
a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 5 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.

Extra

Solution 8a.1: a) Draw the connection of logic symbol.



b) Draw the waveform outputs for 4 clock cycles.

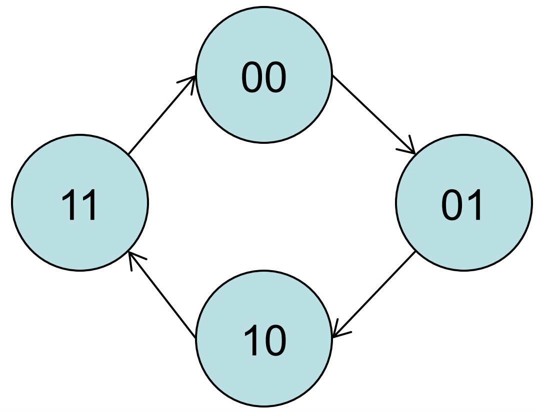


Extra

c) Construct a state table for the counter.

Clock Pulse	**Q_1**	**Q_0**
Initial	0	0
1	0	1
2	1	0
3	1	1
4	0	0

d) Draw the state diagram the the counter.

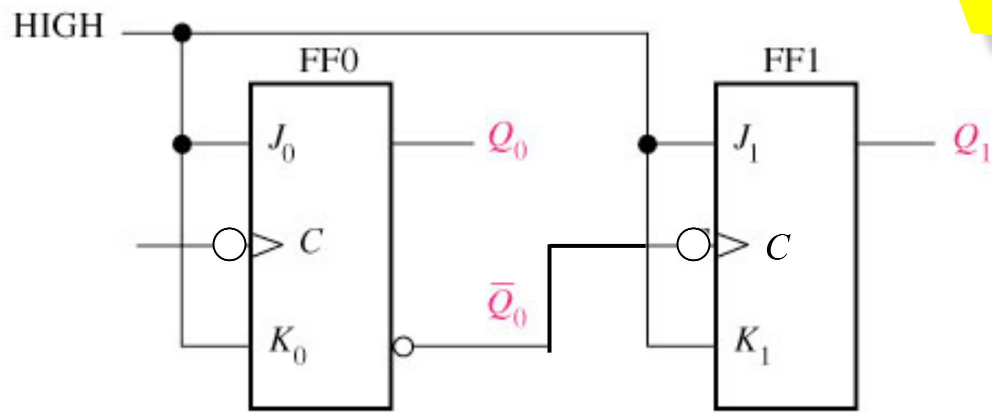


Exercise 8a.2: A 2-bit count down ripple counter is designed using J-K flip-flop with negative edge triggered clock.

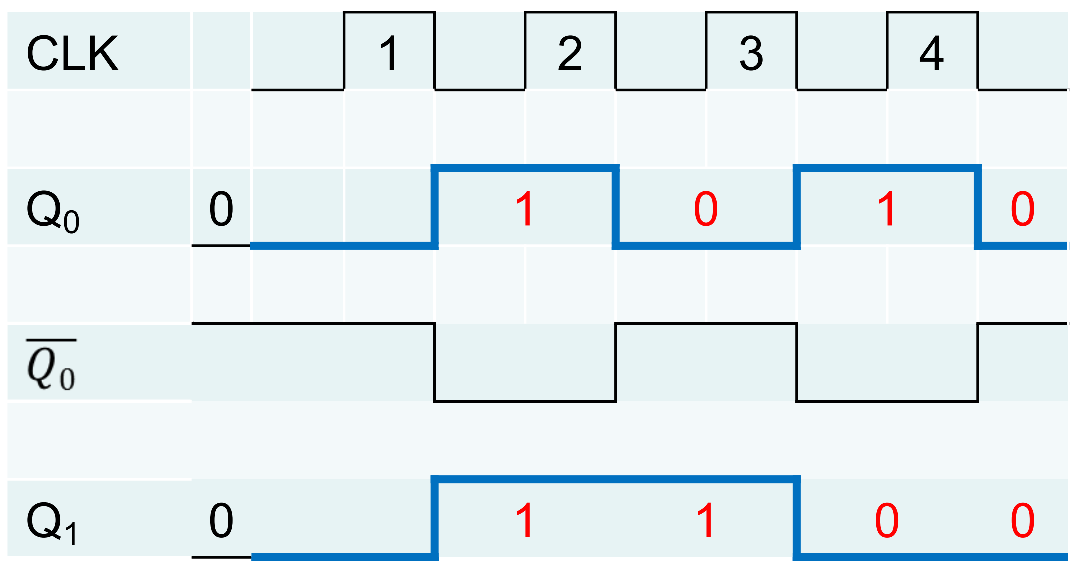
a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 4 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.

Extra

Solution 8a.2: a) Draw the connection of logic symbol.



b) Draw the waveform outputs for 4 clock cycles.

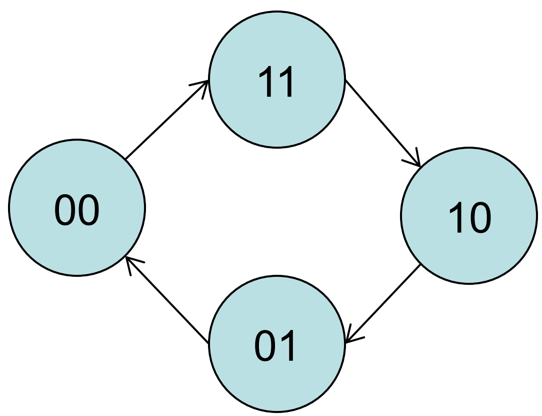


Extra

c) Construct a state table for the counter.

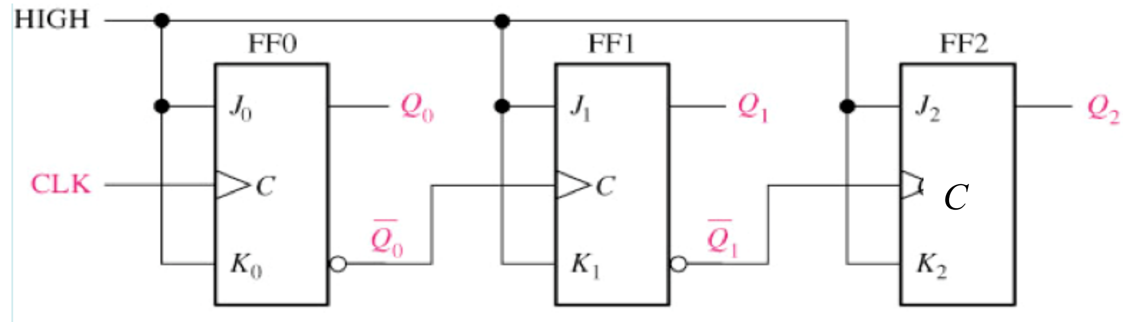
Clock Pulse	**Q_1**	**Q_0**
Initial	0	0
1	1	1
2	1	0
3	0	1
4	0	0

d) Draw the state diagram the the counter.

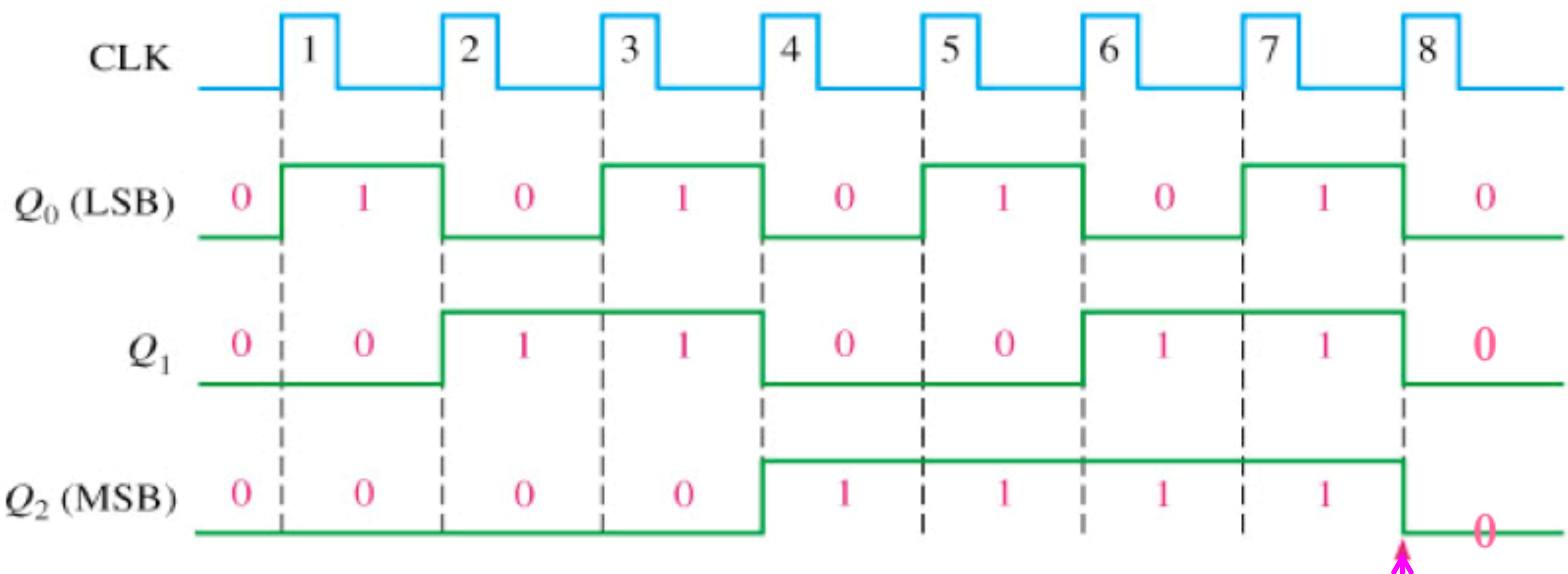


Count Up 3-bit AC

- The circuit connection is the same as 2 bit asynchronous counter, for a 3 bit counter just add another flip-flop.



- Positive edge
- Assume that Q_0 initially LOW



Recycle back to 0

The timing diagram of the 3 bit asynchronous counter.

- The count change every positive edge of a clock.
- The counting sequence is 0,1,2,3,4,5,6,7 and recycle back to 0

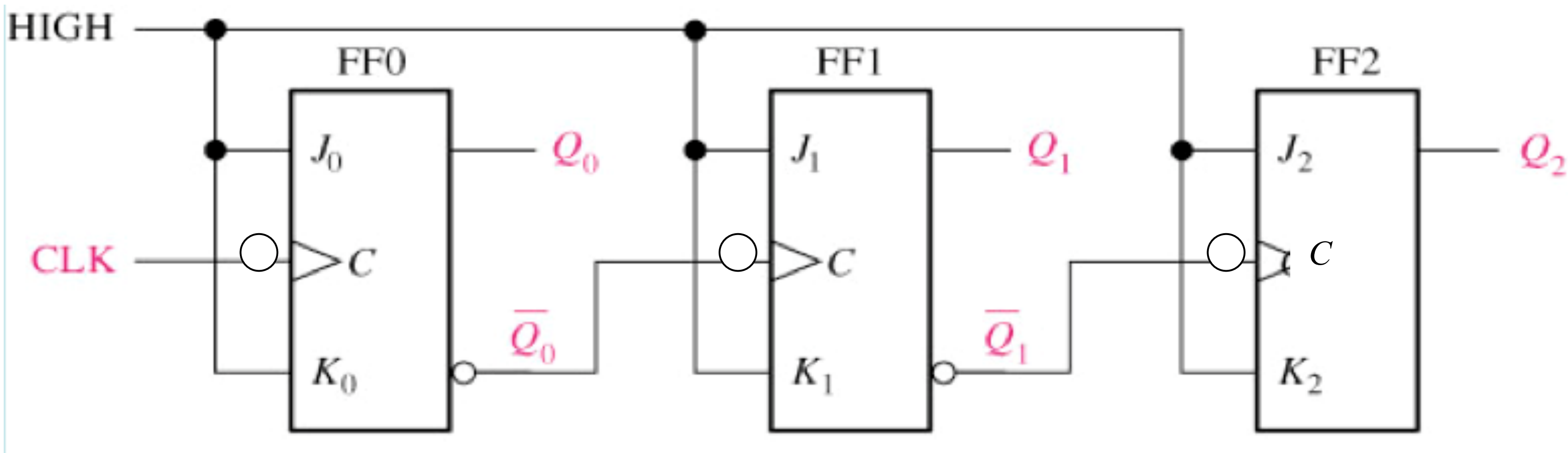
CLOCK PULSE	Q_2 (MSB) (Bit 3)	Q_1 (Bit 2)	Q_0 (LSB) (Bit 1)
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Exercise 8a.3: A 3-bit count down ripple counter is designed using J-K flip-flop with negative edge triggered clock.

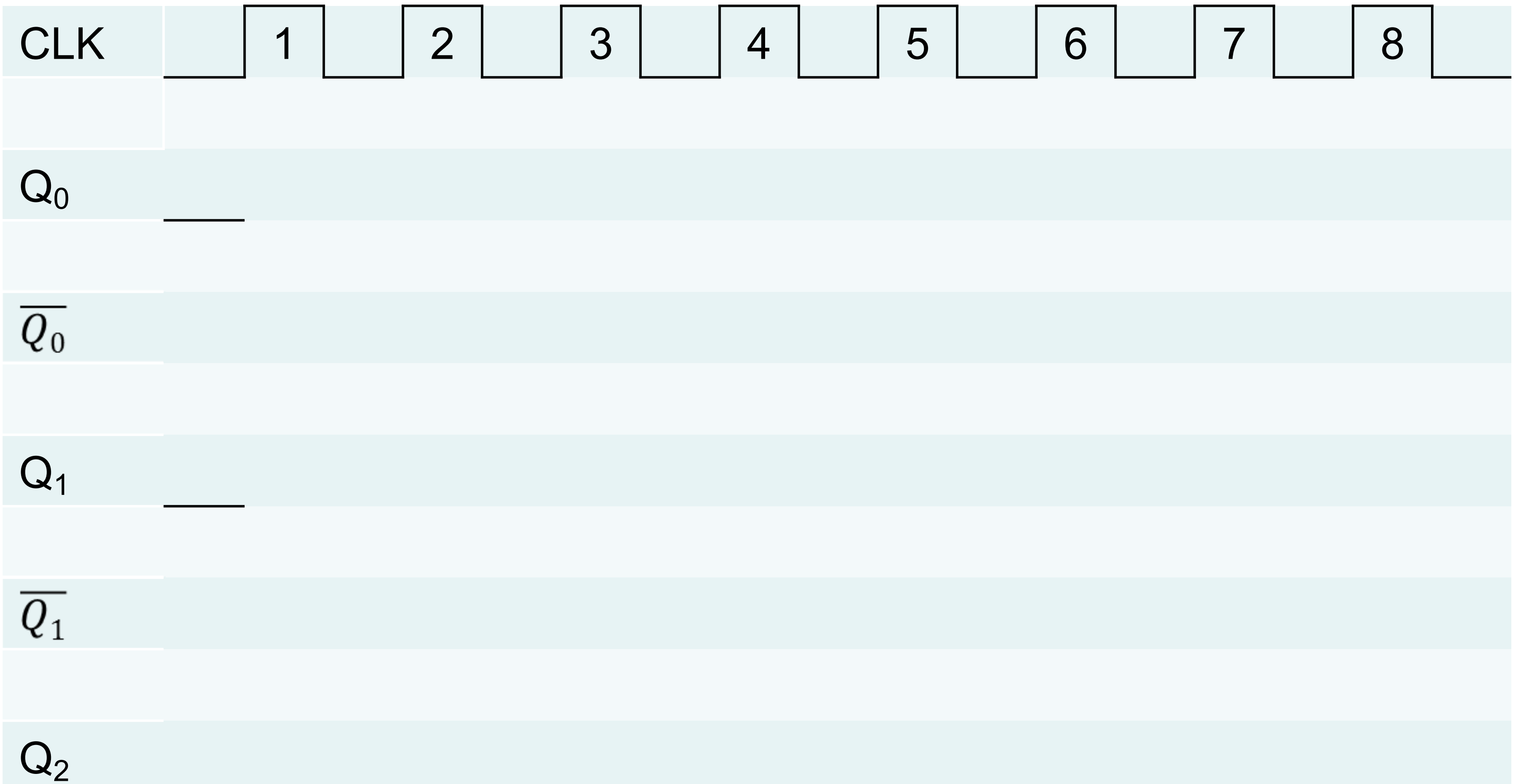
a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 8 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.

Extra

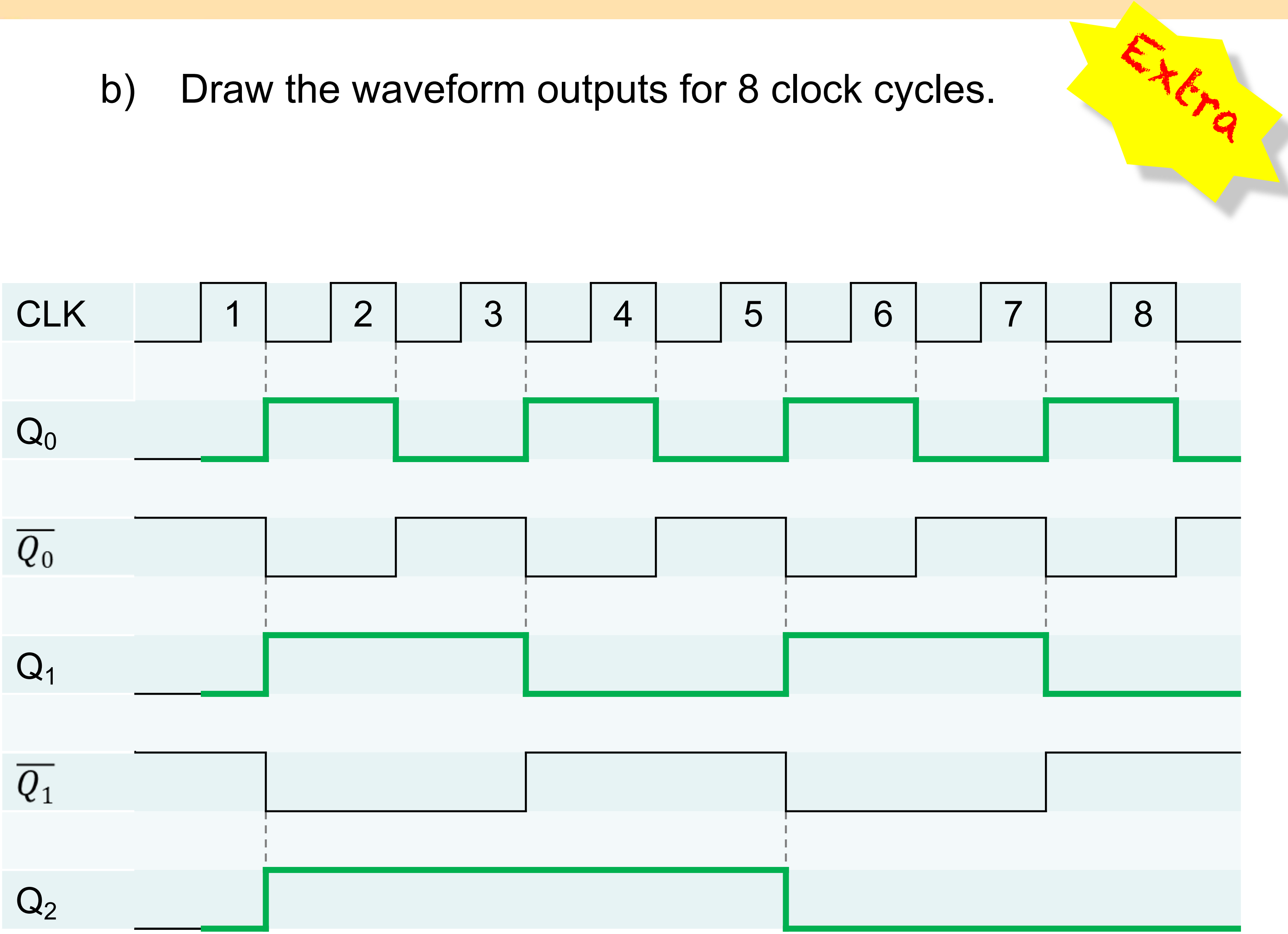
Solution 8a.3: a) Draw the connection of logic symbol.



Extra



b) Draw the waveform outputs for 8 clock cycles.

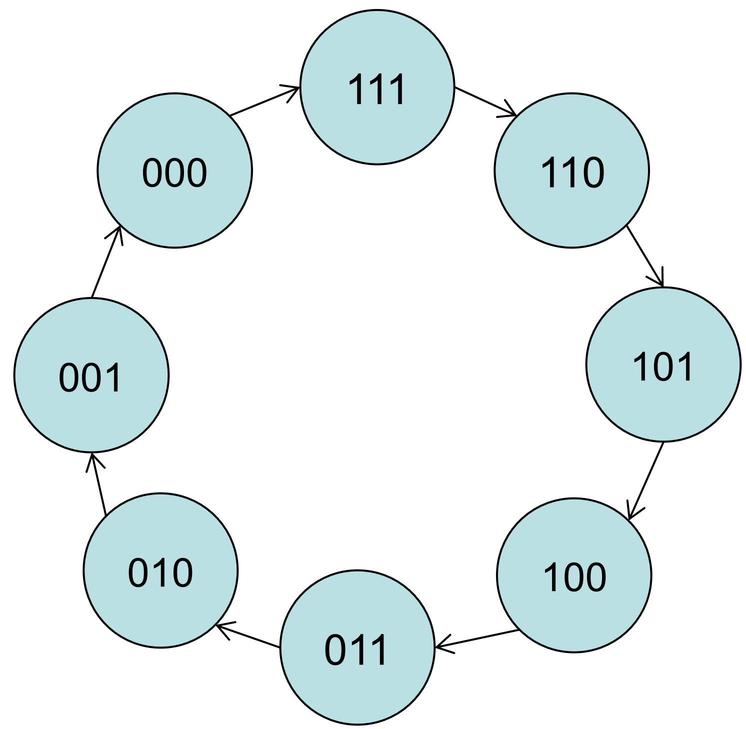


Extra

c) Construct a state table for the counter.

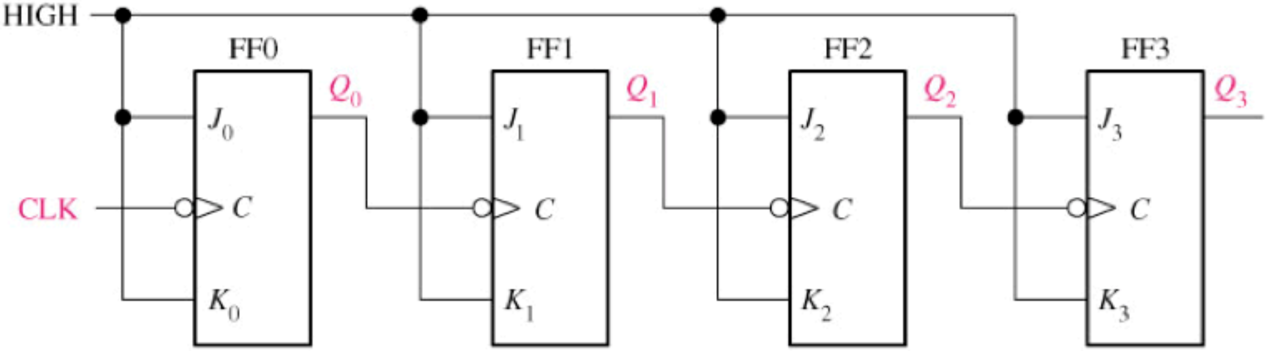
Clock Pulse	Q_2	Q_1	Q_0
Initial	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

d) Draw the state diagram the counter

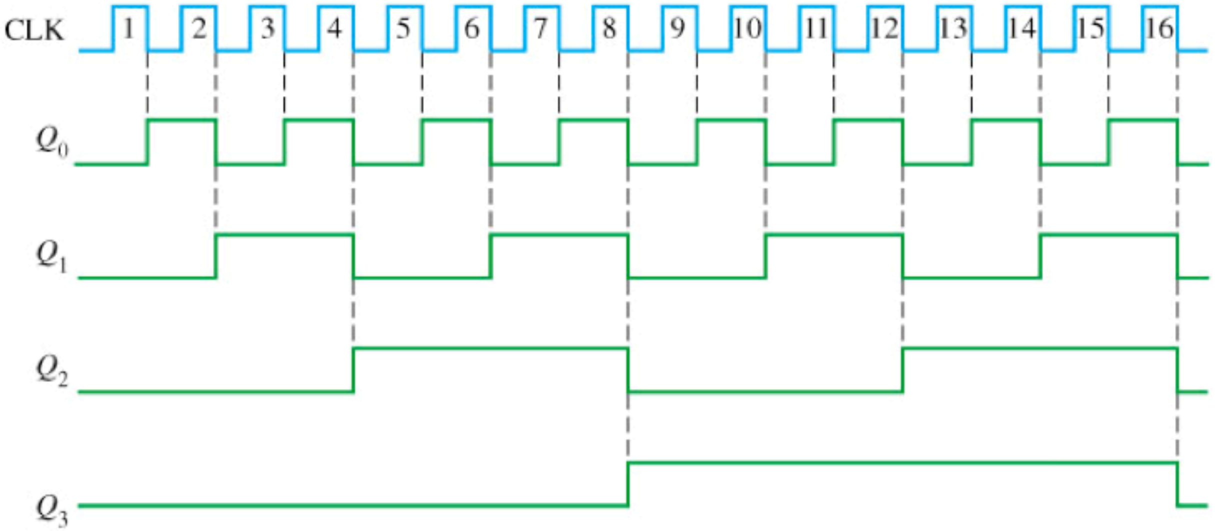


Count Up 4-bit AC

- The counter using a negative edge JK FF.
- But still a count up counter because clock is connected to Q.



(a)



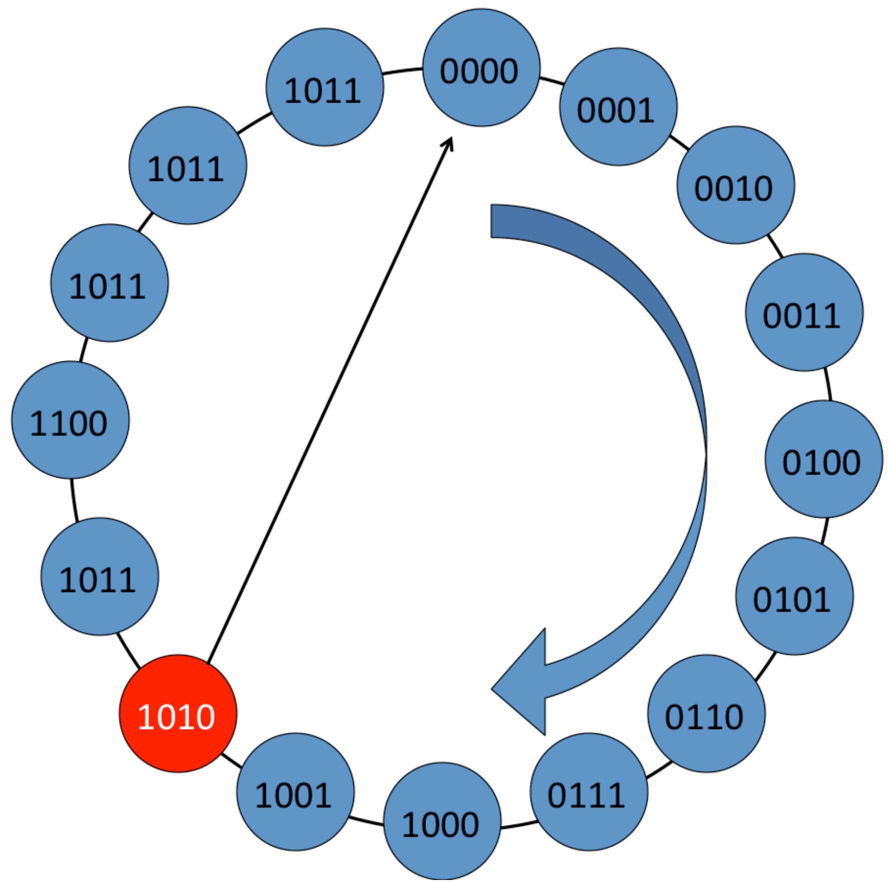
(b)

Exercise 8a.4: A 4-bit count down ripple counter is designed using J-K flip-flop with positive edge triggered clock.

a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 8 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.

Asynchronous Decade Counter

- Maximum number of possible state (max. modulus) of a counter is 2^n.
- However, it can be designed less than 2^n → **Truncated Sequence**
- One common modulus for counters with truncated sequences is ten → **decade counter**
- It will force the counter to cycle before going through all its normal states.



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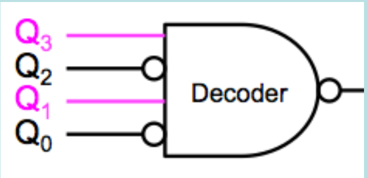
Asynchronously Clocked Modulus-10

Decode ten (1010_2) with a NAND gate and connect the output to the CLEAR inputs of all flip-flops.

Q_3	Q_2	Q_1	Q_0
1	0	1	0



Decoder Design

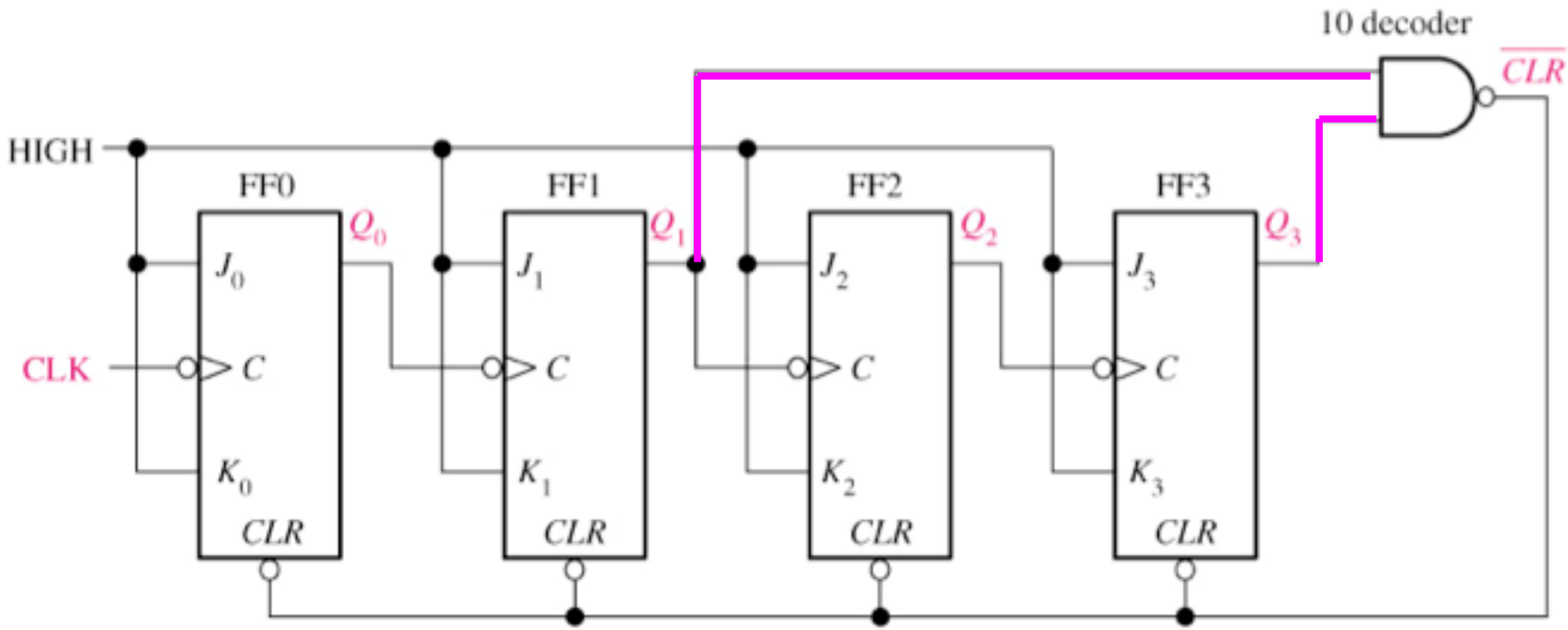


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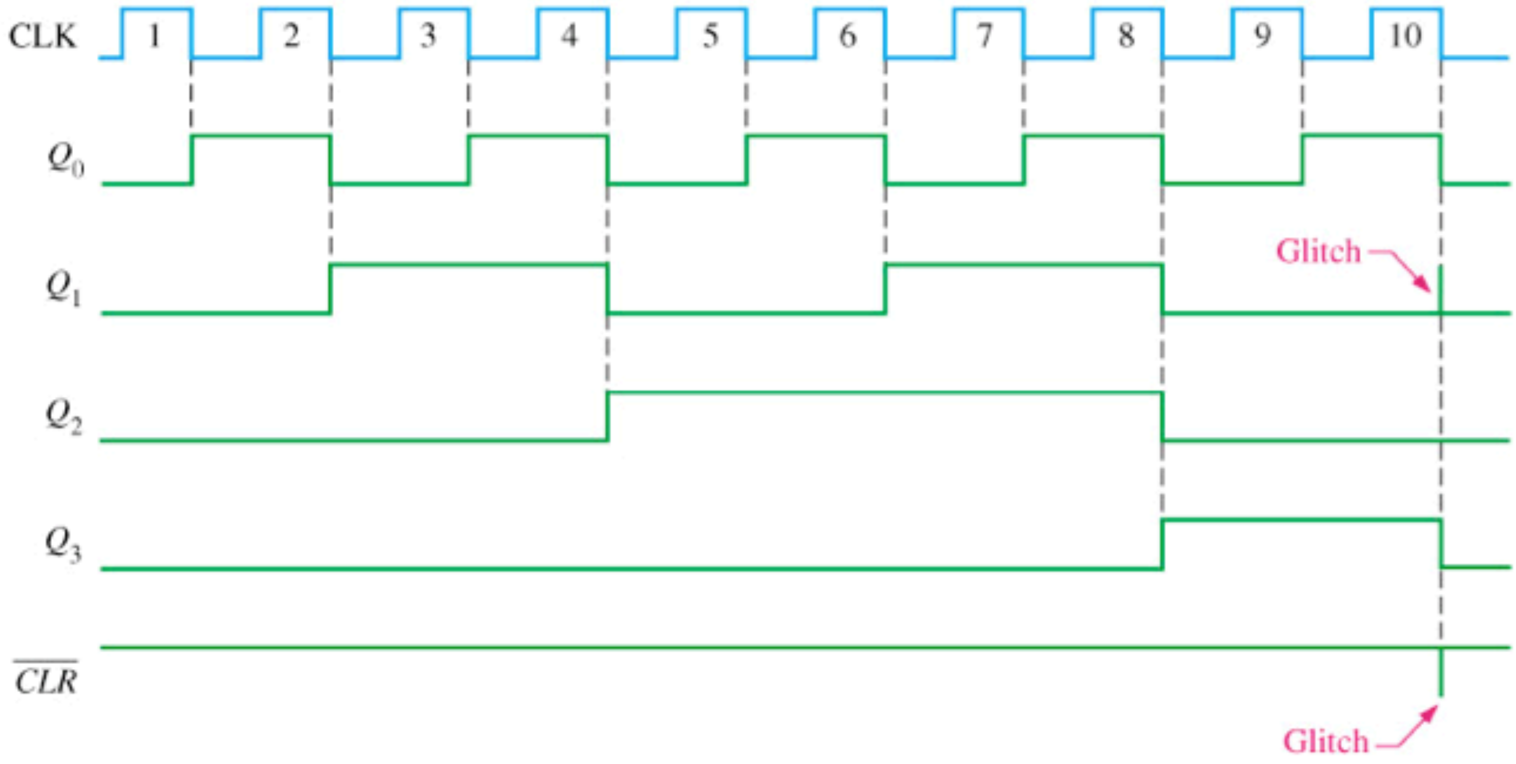
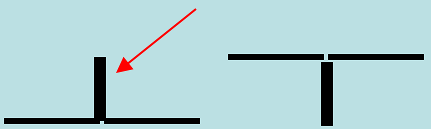
Figure: Count Up 4-bit Asynchronous Decade Counter



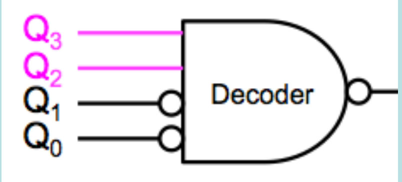
Notice that there is a **glitch** in Q_1. The reason of this glitch is that Q_1 must first go HIGH before the count 10 can be decoded. Several nanoseconds after the decoding gate goes LOW.



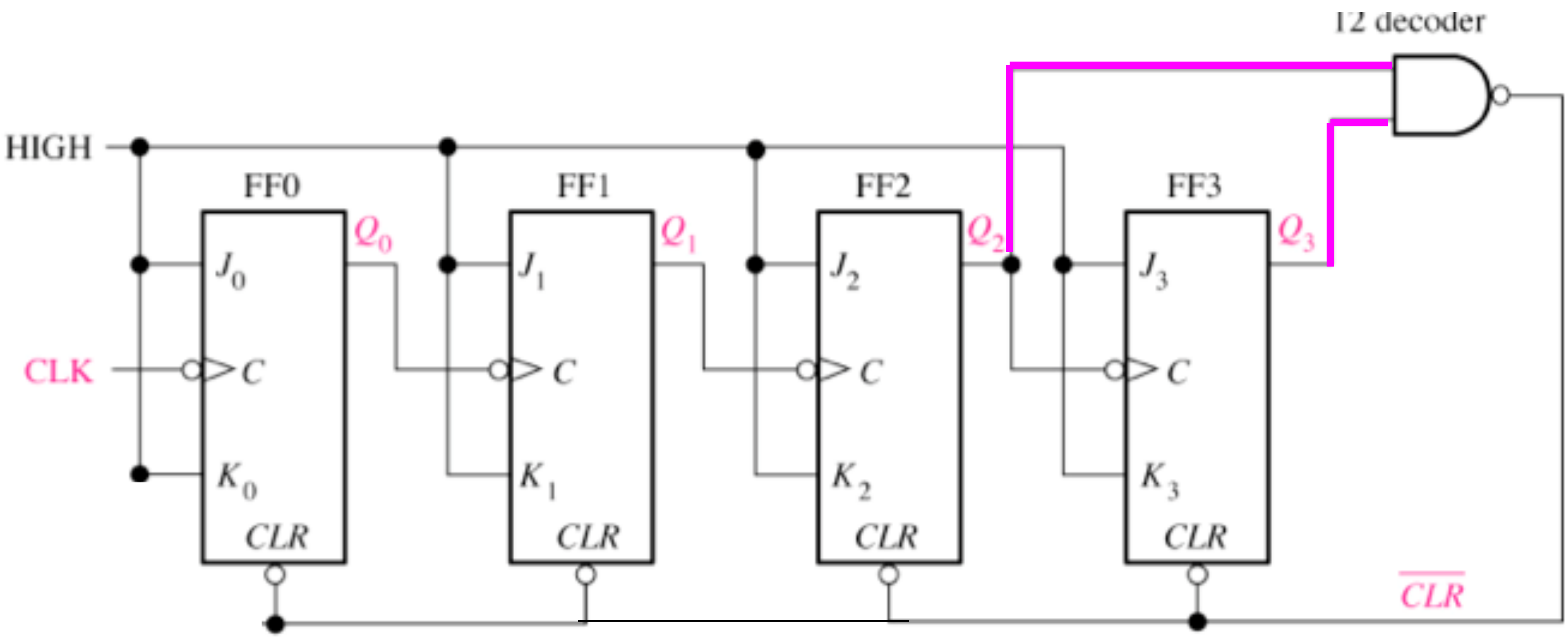
Asynchronously Clocked Modulus-12

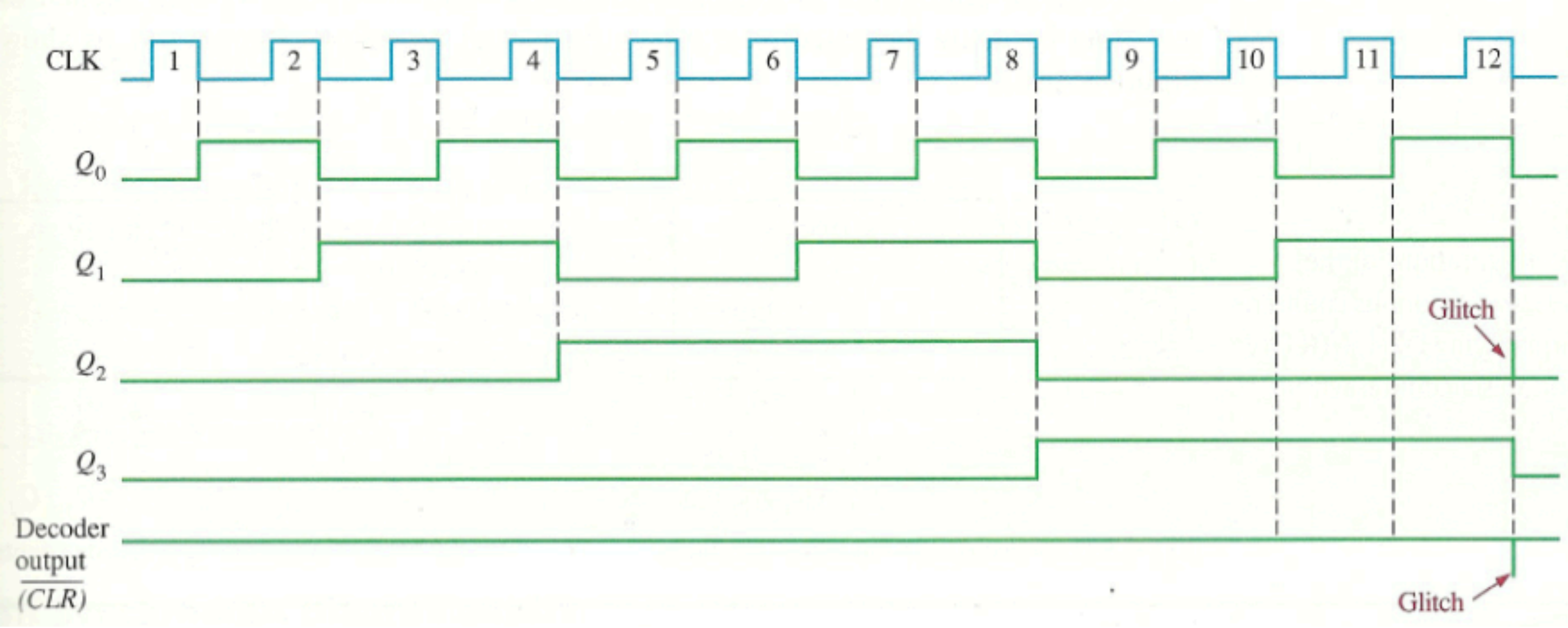
Decode twelve (1100_2) with a NAND gate and connect the output to the CLEAR inputs of all flip-flops.

Q_3	Q_2	Q_1	Q_0
1	1	0	0



Decoder Design




CLK
1
2
3
4
5
6
7
8
9
10
11
12
Q_0
Q_1
Q_2
Q_3
Decoder output $(\overline{CLR})$
Glitch
Glitch

Advantage and Disadvantage of AC

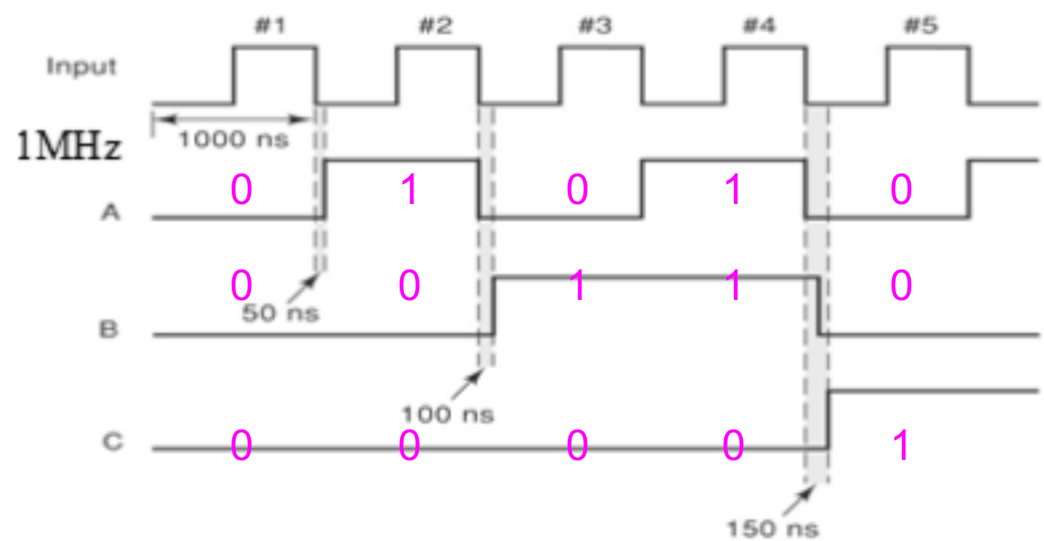
- Advantage:
  - The design step is simple (easy)
- Disadvantage:
  - Propagated delay accumulate as in ripple binary adder which may cause a missing counting state
    - Especially at high speed (frequency) operation, therefore this kind of counter cannot operates at high frequency.
    - The maximum operating frequency $f_{max} = \frac{1}{Nt_{pd}}$ where N is the number of flip-flop an t_{pd} is the propagation delay of the flip-flop

Effect of propagation delay on AC

Assume 3 bits counter using a flip-flop with a propagation delay of 50ns.

Low frequency

Case 1 : operating at low frequency of 1 MHz
For each stage there is a 50 ns delay and it accumulates up to 150ns at the 3rd stage. The accumulated delay is still lower than the period of the signal which is 1000ns , therefore there is no effect to the counting sequence.

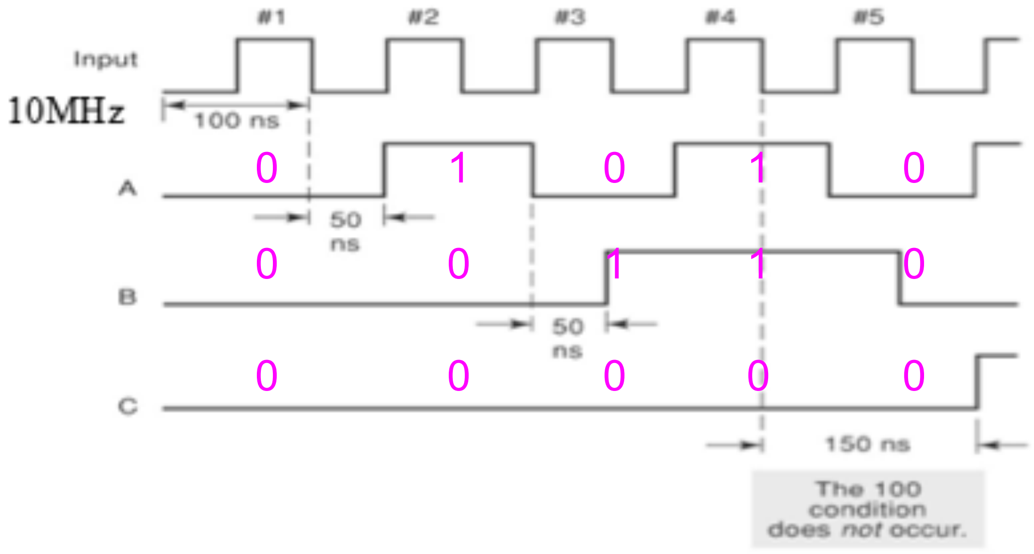


continue...

High frequency

Case 2: operating at a higher frequency of 10 MHz

The clock period is only 100ns. For a 3 stage flip-flop the accumulated delay is the same as before which is 150ns. But, now the accumulated delay is more than the clock period, therefore there is a missing count, 100 doesn't exist!



Exercise 8a.5: If a propagation delay of a mod 32 asynchronous recycle UP counter using JK FF is 40ns, what is the maximum operating frequency?

Solution:

$$\text{Number of flip-flops} = \left\lceil \frac{\log MOD}{\log 2} \right\rceil$$

$$= \frac{\log 32}{\log 2}$$

$$= \frac{\log 2^5}{\log 2}$$

$$= \frac{5 \log 2}{\log 2}$$

$$N = 5$$

$$f_{max} = \frac{1}{Nt_{pd}}$$

$$= \frac{1}{5(40ns)}$$

$$= \frac{1}{5(40 \times 10^{-9} s)}$$

$$f = 5 \text{ MHz}$$