UNIVERSITI TEKNOLOGI MALAYSIA

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SCSR1013 DIGITAL LOGIC

MODULE 7:
ATCHES & FLIP-FLOPS

FACULTY OF COMPUTING

INTRODUCTION TO LATCH & FLIP-FLOP

LATCH

- S-R Latch
- Gated S-R Latch
- Gated D Latch

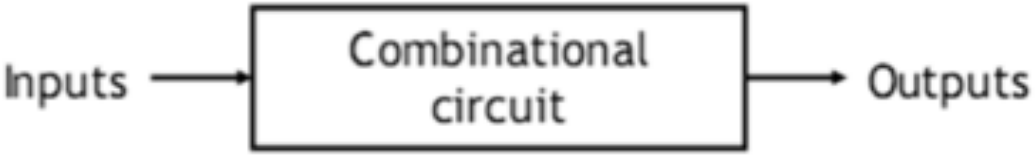
FLIP-FLOPS

- Edge-Triggered D Flip-Flop
- S-R Flip-Flop
- J-K Flip-Flop
- T Flip-Flop

Introduction to Latch & Flip-Flop

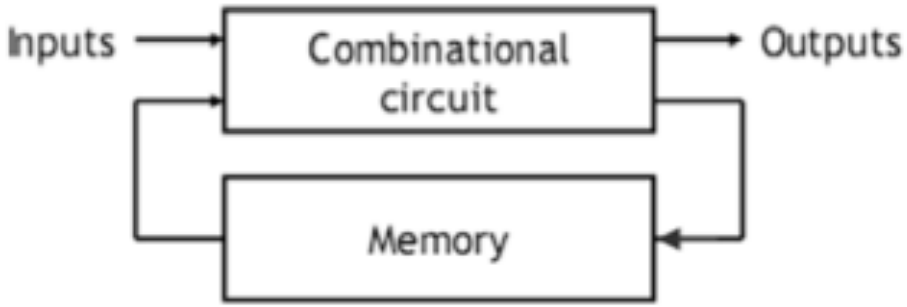
Sequential Vs Combinational Logic Circuit

Combinational Logic Circuit:



- The output depend on the input
- It has no memory element
  - Therefore it cannot memorize the previous output

Sequential Logic Circuit:

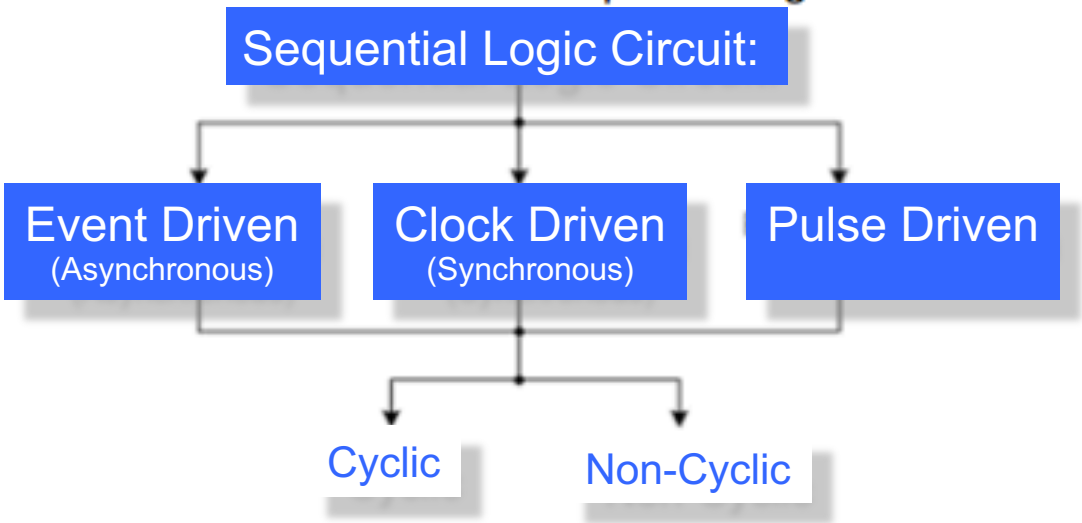


- It has memory element
- The output depend on the input, as well as the previous output from the feedback elements

Sequential Logic circuits can be divided into 3 main categories:

1. Clock Driven - Synchronous Circuits that are synchronized to a specific clock signal.
2. Event Driven - Asynchronous Circuits that react or change state when an external event occurs.
3. Pulse Driven - Which is a Combination of Synchronous and Asynchronous.

Classification of Sequential Logic



Sequential logic circuits that return back to their original state once reset, i.e. circuits with loops or feedback paths are said to be "Cyclic" in nature.

Latch

- Latch is a type of temporary storage device
- It has two stable states (bi-stable).
- Latch is level sensitive, or level-triggered.
  - are dependent on the voltage level applied , not on any signal transition.
- Type of Latch :
  - i) S-R
  - ii) Gated S-R
  - iii) Gated D

LOW HIGH

INFO :

A ***bi-stable*** state is one with *two-stable* output states.

S → Set

R → Reset

D → Data

Flip-Flop

- Flip-flop (FF) are synchronous bi-stable storage devices capable of storing one bit, where the output state only changes at a specified point on a triggering input called the Clock (C).

- So FF are edge-triggered, means that the output changes are synchronized with the Clock signal.
  - This may either be a LOW-to-HIGH (rising edge) or a HIGH-to-LOW (falling edge) transition.

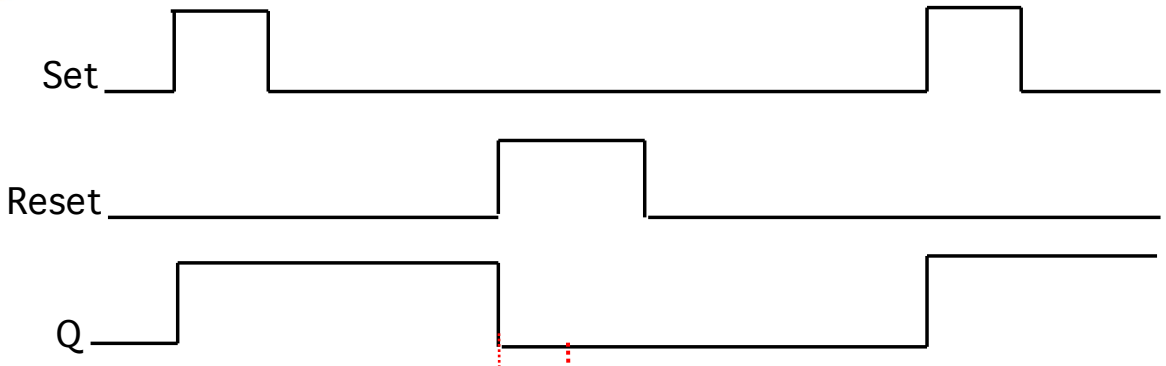
- Type of Flip-Flop:
  - i) D
  - ii) S-R
  - iii) J-K
  - iv) T

INFO :
Rising edge = positive edge
Falling edge = negative edge

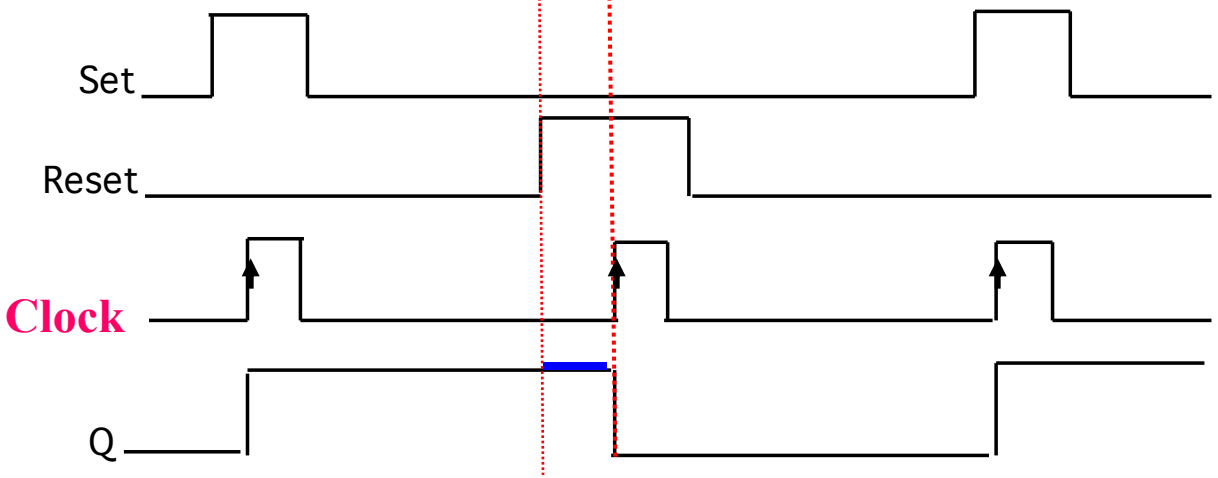
J K ☐ Two control inputs

Difference:
Latch vs Flip-Flop

Latch



Flip-flop

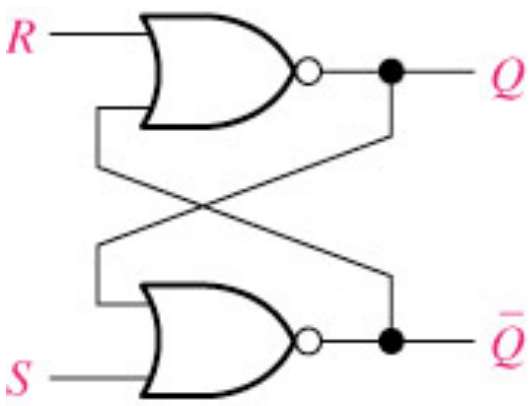


Latches

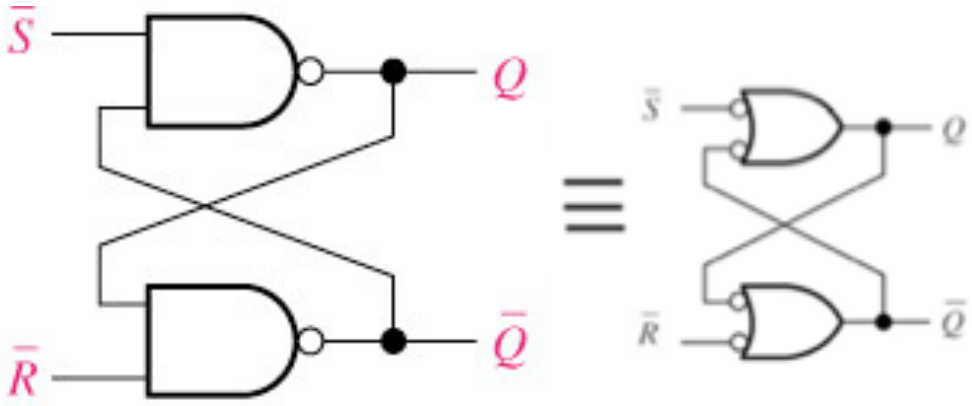
i) **S-R**
ii) **Gated S-R**
iii) **Gated D**

S-R Latch

- The output of each gate is connected to an input of the opposite data.
- This produces a regenerative feedback.

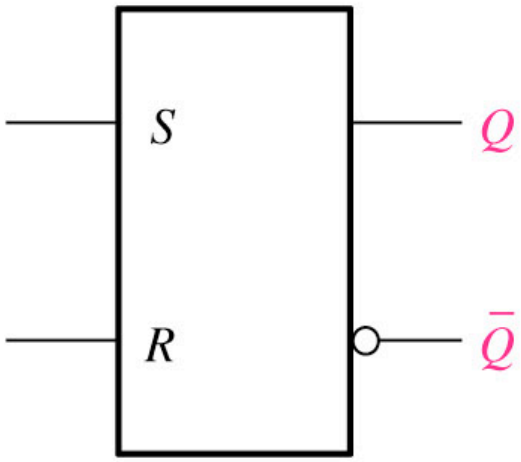


(a) Active-HIGH input S-R latch

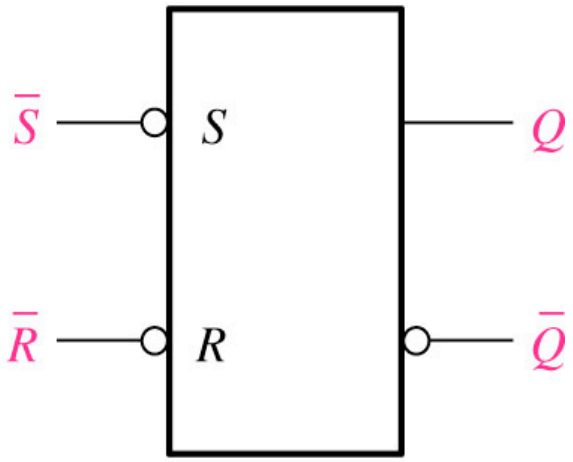


(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

S-R Latch: Logic symbol

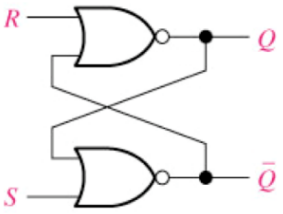


(a) Active-HIGH input S-R latch



(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

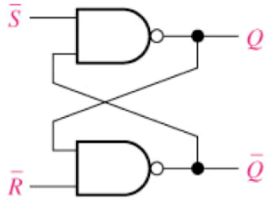
Circuit (a) Active-HIGH input S-R latch :

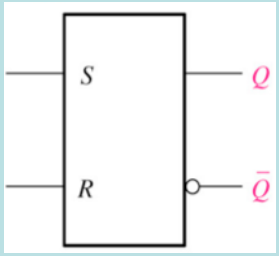


- use NOR gate
- Input R and S
- Output Q and Q'

Circuit (b) Active-LOW input S'-R' latch :

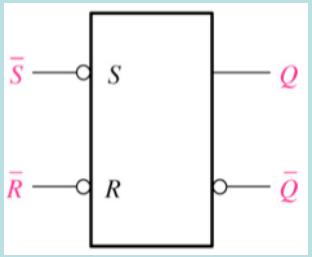
- use NAND gate
- Input S' and R'
- Output Q and Q'





Active-HIGH

INPUTS		OUTPUTS		COMMENTS
S	R	Q	$\overline{Q}$	
0	0	NC	NC	No change. Latch remains in present state
0	1	0	1	Latch RESET
1	0	1	0	Latch SET
1	1	0	0	Invalid condition



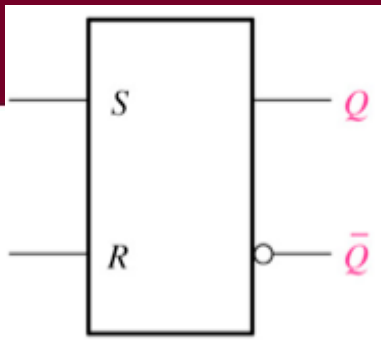
Active-LOW

INPUTS		OUTPUTS		COMMENTS
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
0	0	1	1	Invalid condition
0	1	1	0	Latch SET
1	0	0	1	Latch RESET
1	1	NC	NC	No change. Latch remains in present state

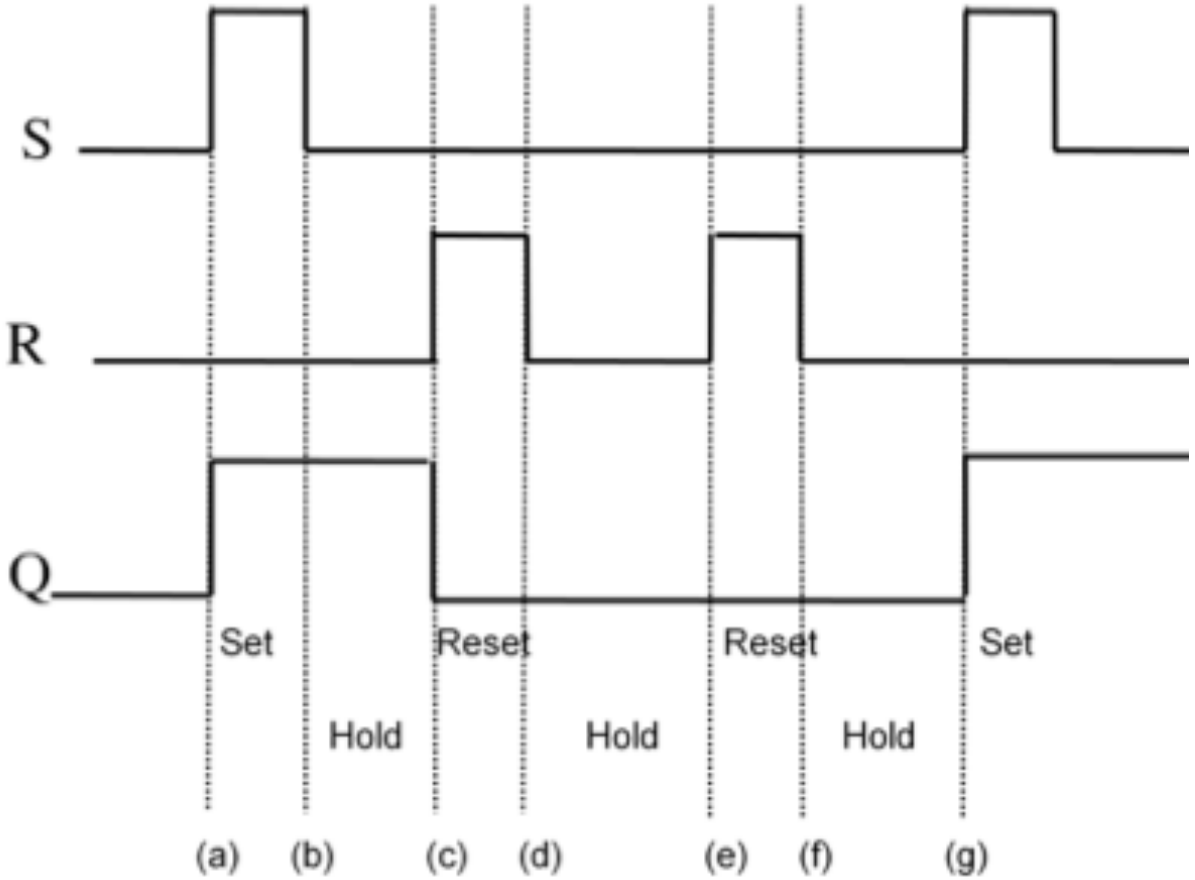
Explanation :

- The Q and not-Q outputs are supposed to be in opposite states.
- Q=1 and not-Q=0 is defined as *Set* (by making S=1 and R=0)
- Q=0 and not-Q=1 is conversely defined as *Reset* (by making S=0 and R=1)
- When S and R are both equal to 0, the multivibrator's outputs "*Not Change*" in their prior states.
- If Q and not-Q happen to be forced to the same state (both 0 or both 1), that state is referred to as *invalid*.

Example: S-R Latch (Active HIGH)



Logic symbol



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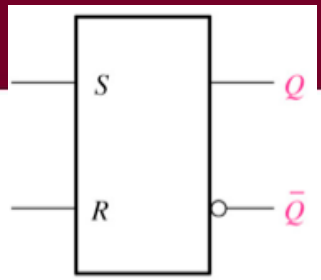


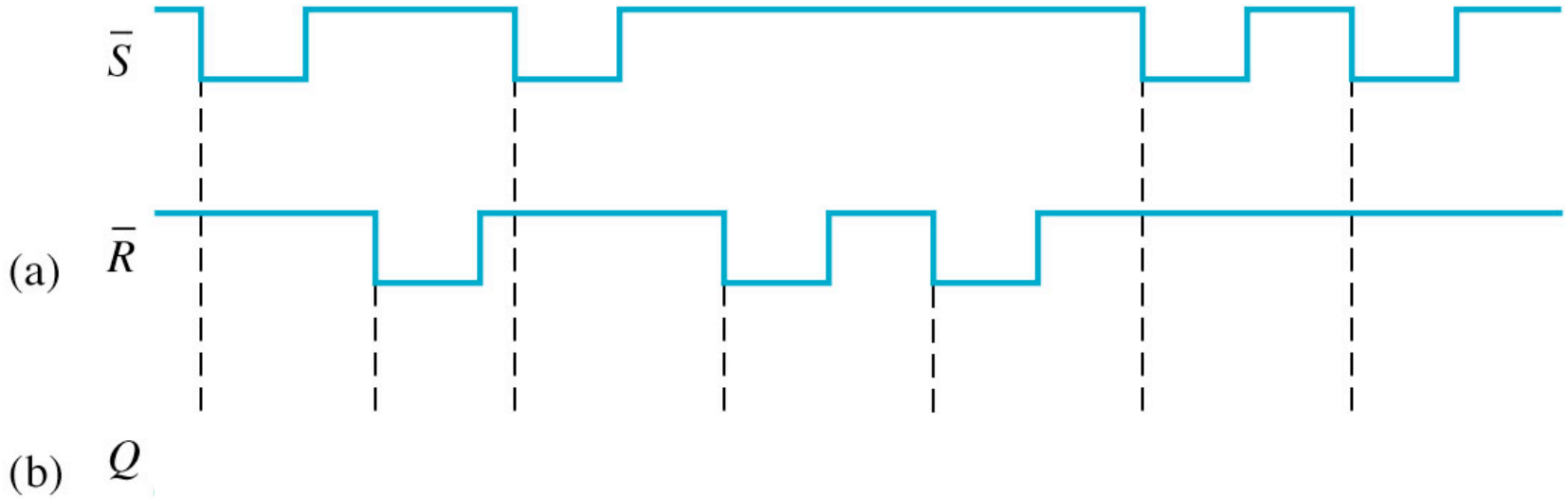
Logic symbol

Explaination:

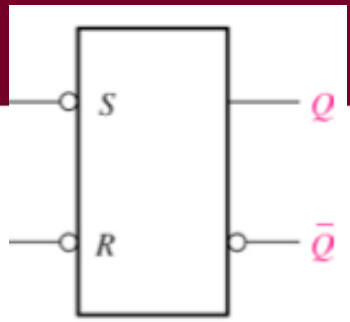
Location	S	R	Q	State
(a)	1	0	1	SET
(b)	0	0	1	HOLD
(c)	0	1	0	RESET
(d)	0	0	0	HOLD
(e)	0	1	0	RESET
(f)	0	0	0	HOLD
(g)	1	0	1	SET

Extra DIY

Exercise 7.1: If the $\overline{S}$ and $\overline{R}$ waveform in (a) are applied to the inputs of latch (active-LOW), determine the waveform that will be observed on the Q output in (b). Assume that Q is initially LOW.

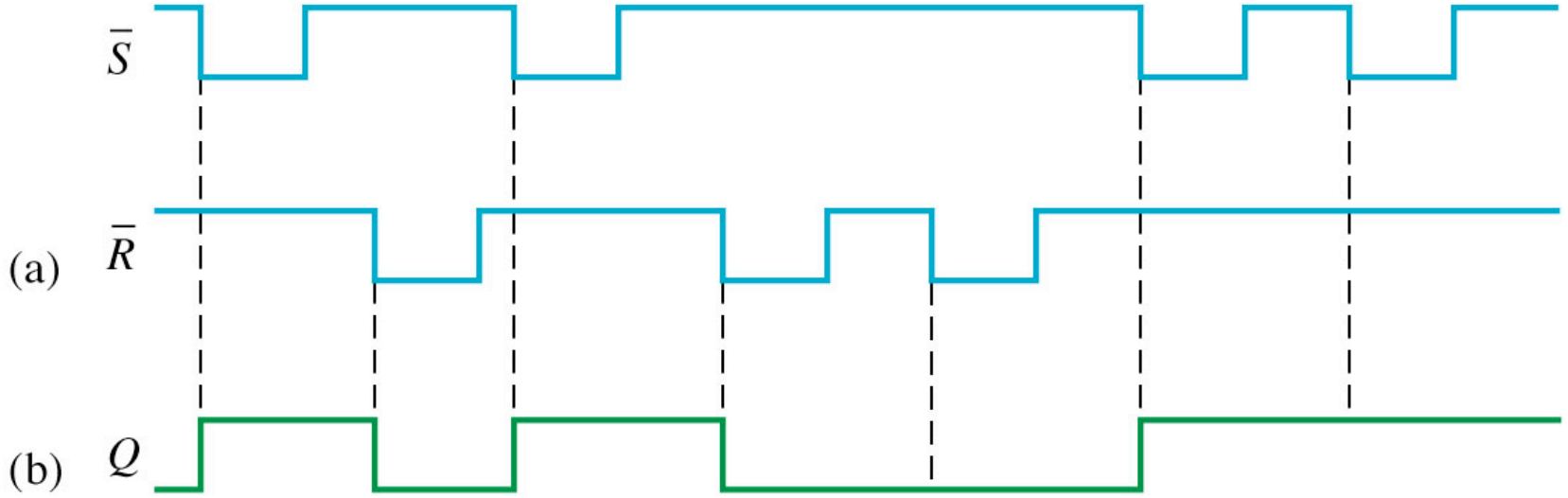


Extra DIY

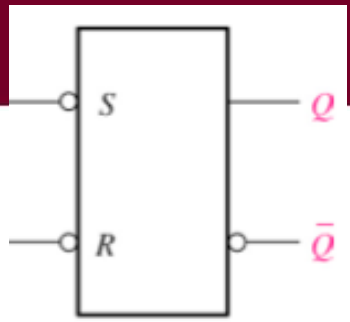


Logic symbol

Solution:

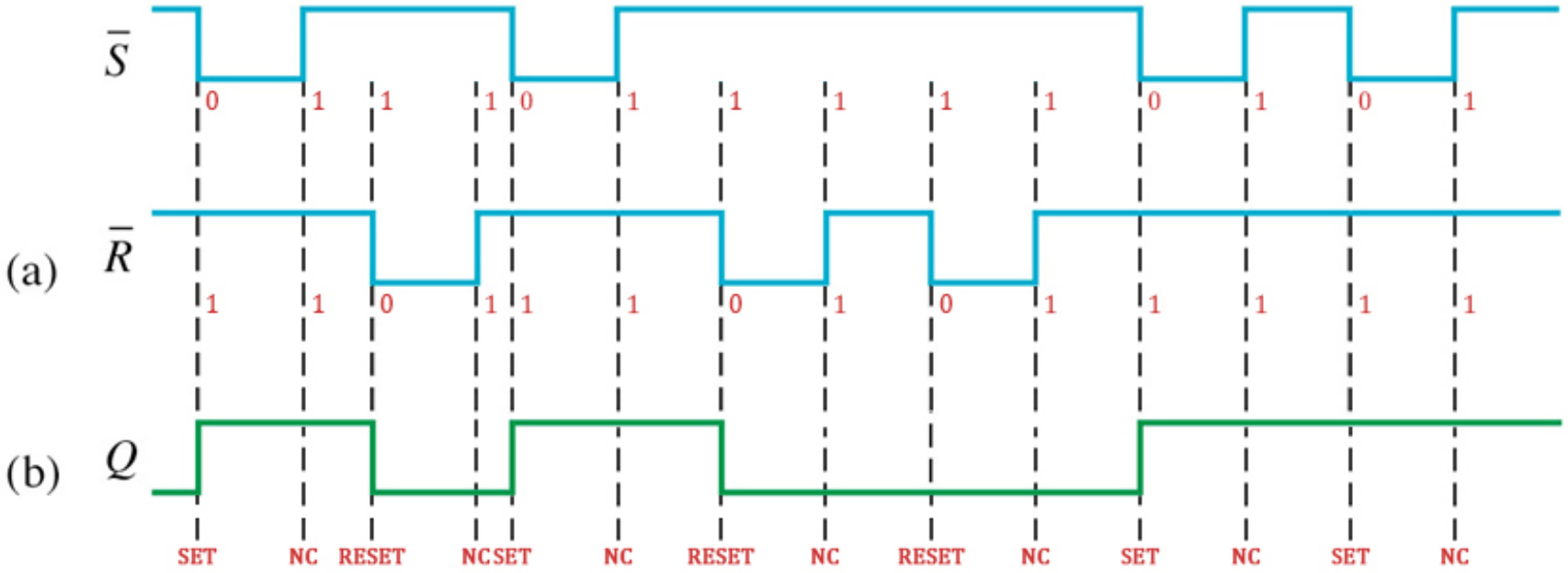


Extra DIY



Logic symbol

Solution:



Gated S-R Latch

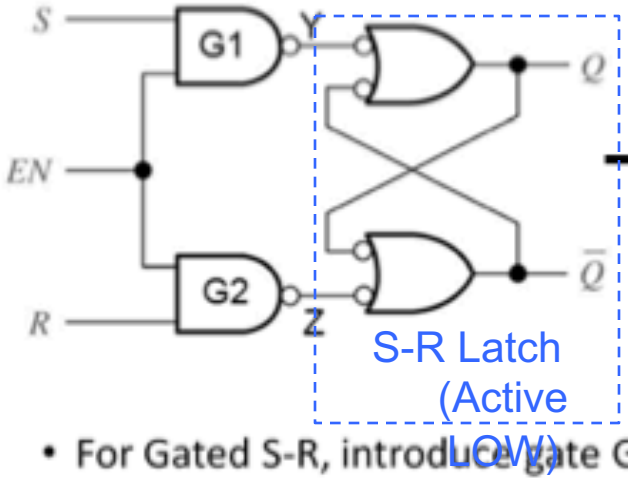
- Is a gated latch requires an enable input (EN).
- The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input.
- The latch will not change until EN is HIGH, but as long as it remains HIGH, the output is controlled by the state of the S and R input.

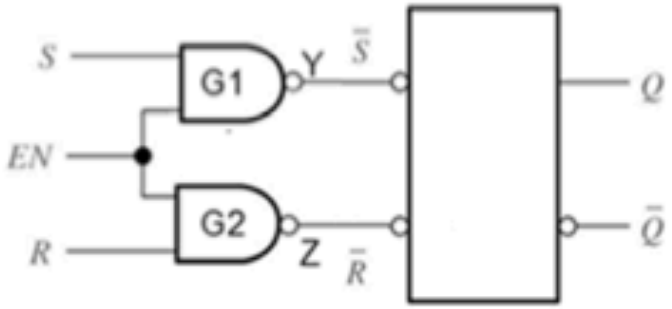
- The invalid state occurs when both S and R are simultaneously HIGH.

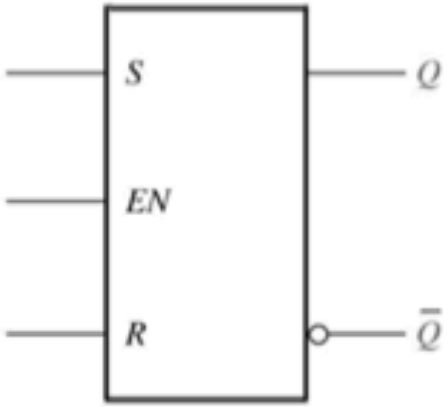
INFO :

EN = 1, Latch is On
EN = 0, Latch is Off

Gated S-R Latch: Circuit and Symbol







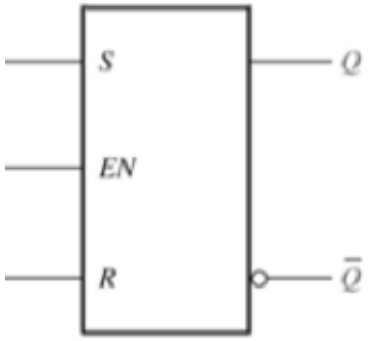
- For Gated S-R, introduce gate G1 and G2
  - behaves as a gate that control whether to allow S to Y and R to Z or to make $Y = Z = 1$

$$Y = \overline{(S \cdot EN)} \qquad Z = \overline{(R \cdot EN)}$$

  - If EN = 0, Y =1 and Z=1
  - If EN=1, Y =S' and Z = R' this will change an active low SR to an active HIGH SR flip-flop

Gated S-R Latch: Truth Table

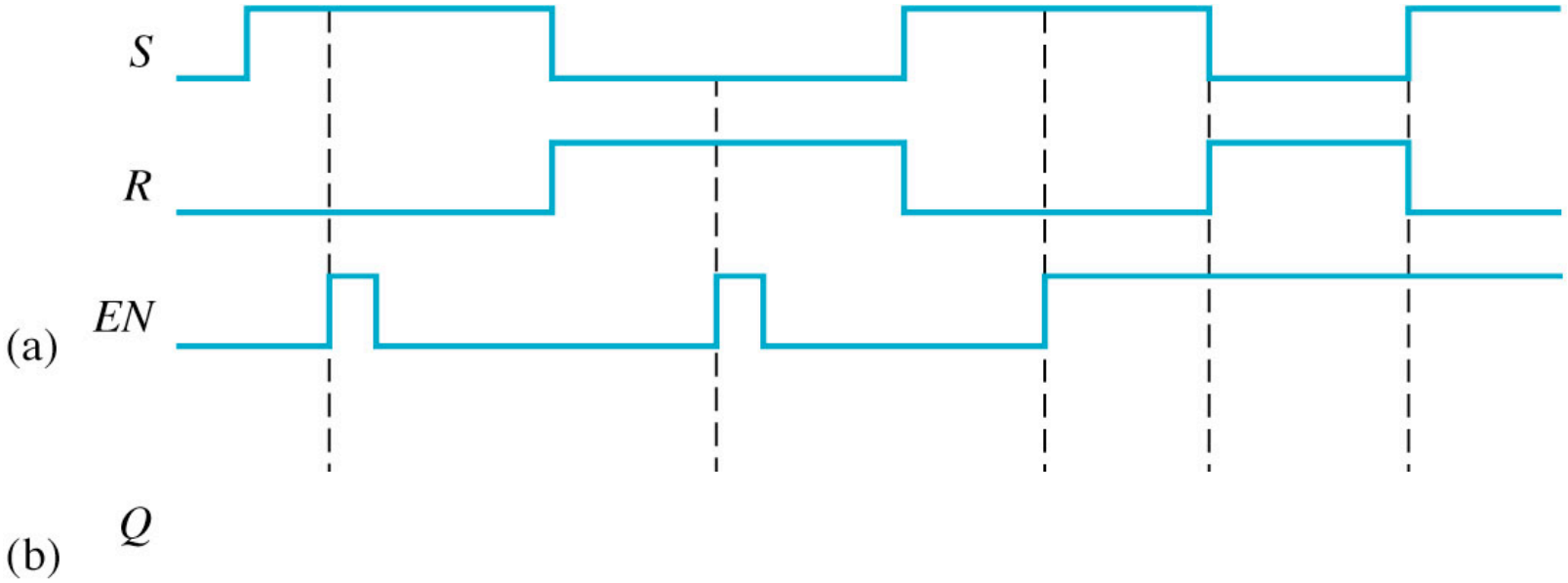
EN	S	R	Output
0	0/1 (X)	0/1 (X)	No Change
1	0	0	No Change
1	0	1	Q=0 (RESET)
1	1	0	Q=1 (SET)
1	1	1	Invalid

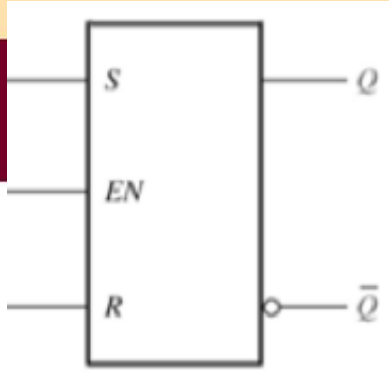


Logic symbol

Example: Gated S-R Latch.

Find the waveform for Q. Assume that Q is initially LOW.

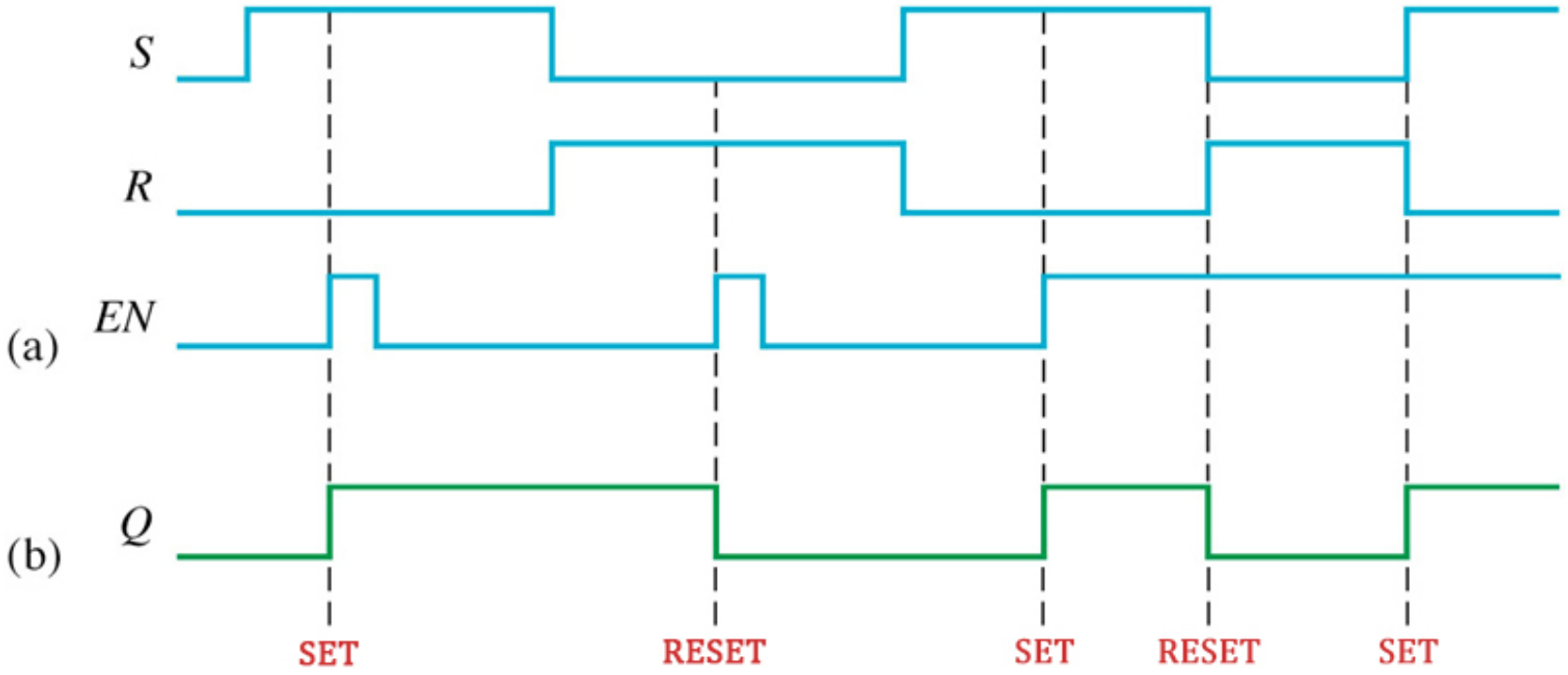




Logic symbol

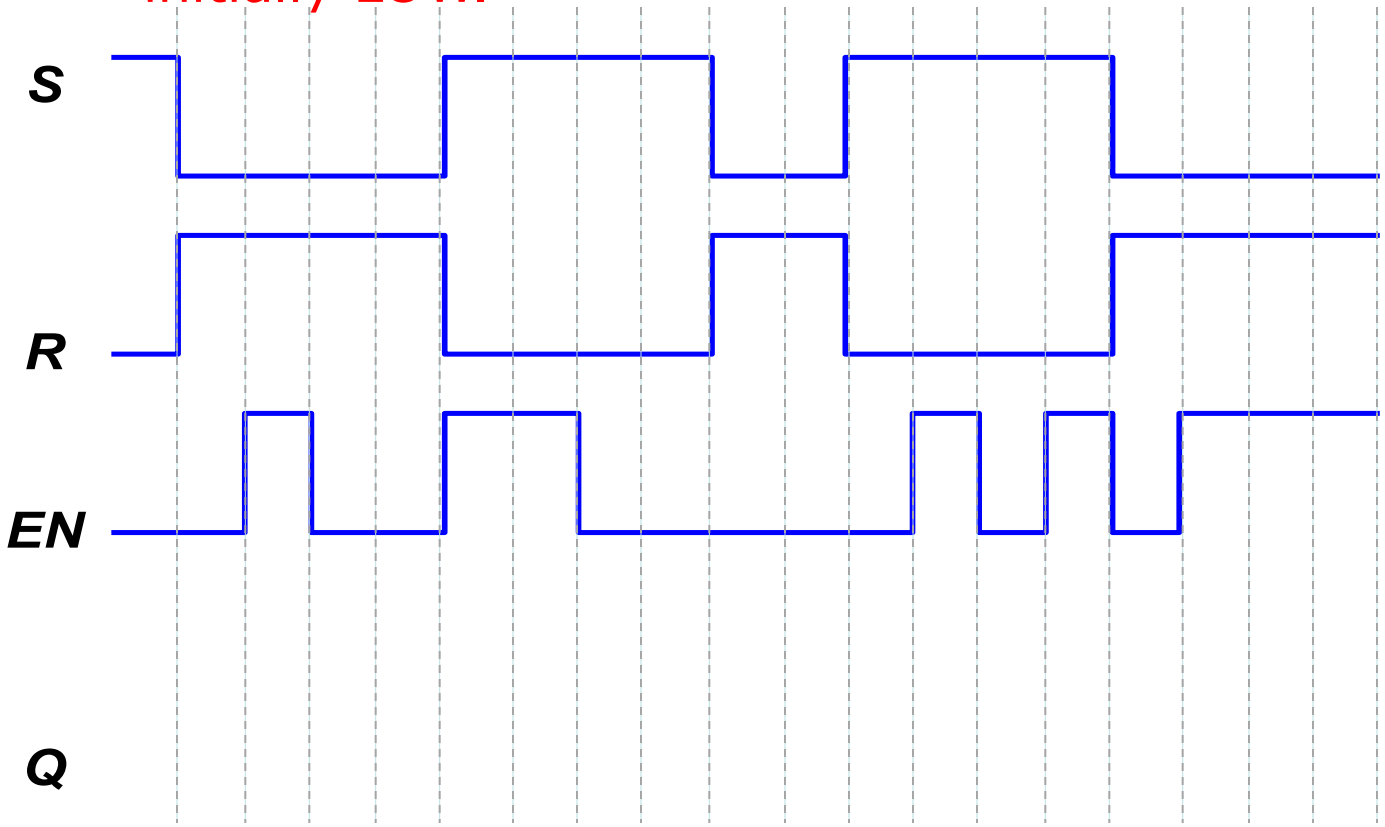
Solution:

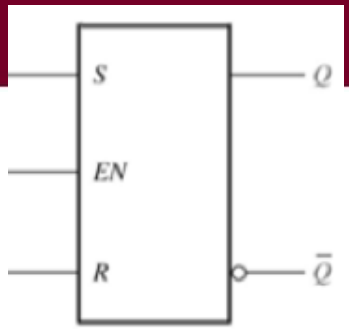
EN	S	R	Output
0	0/1 (X)	0/1 (X)	No Change
1	0	0	No Change
1	0	1	Q=0 (RESET)
1	1	0	Q=1 (SET)
1	1	1	Invalid



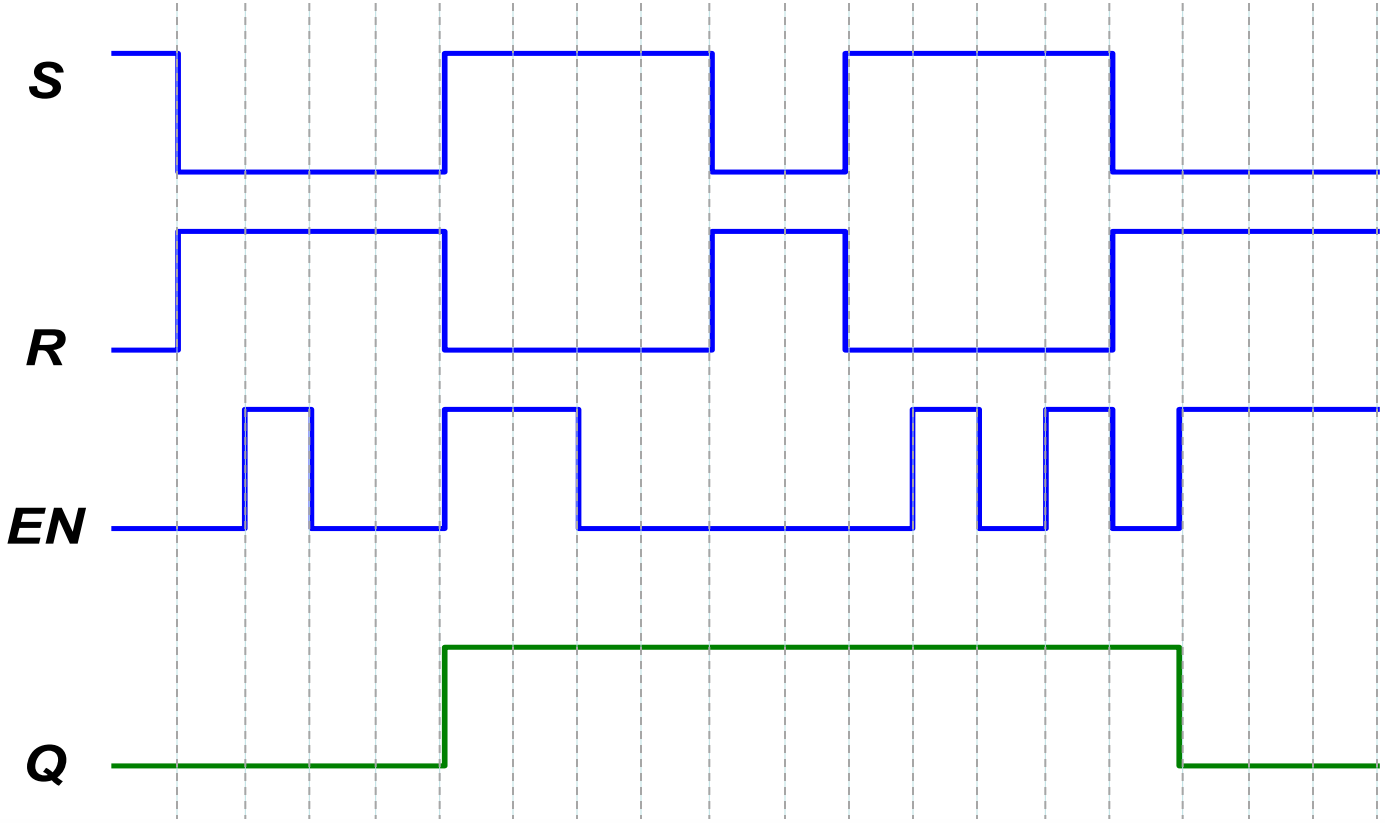
Example: Gated S-R Latch.

Find the waveform for Q. Assume that Q is initially LOW.

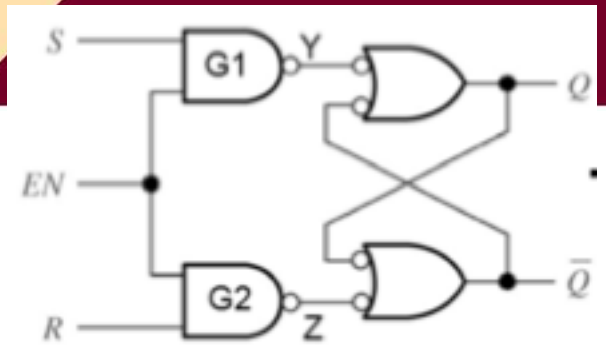


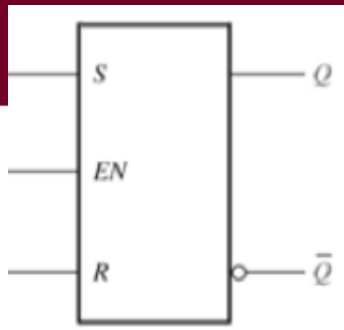


Solution:



Exercise 7.2:

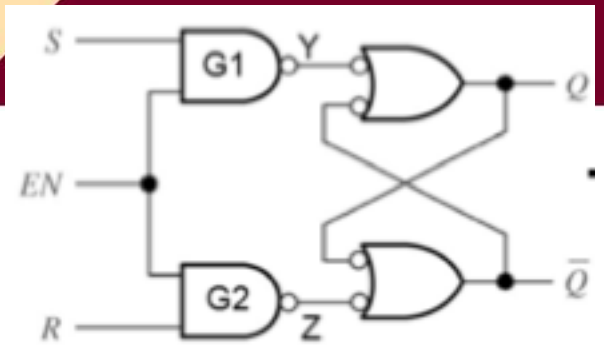


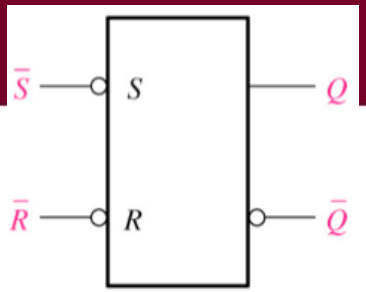


Referring to logic diagram above, fill in the table. Assume initially Q = 0 and Q' = 1

EN	S	R	Y	Z	Q
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Solution:



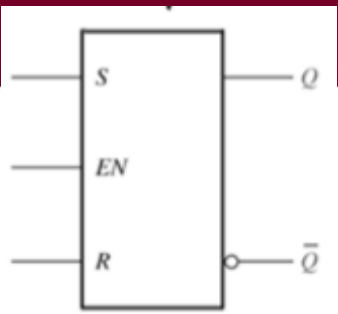


S-R Latch (Active LOW)

Referring to logic diagram above, fill in the table. Assume initially Q = 0 and Q' = 1

EN	$\bar{S}$	$\bar{R}$	Y	Z	Q
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	1	1	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	1	0	0	1

continue...



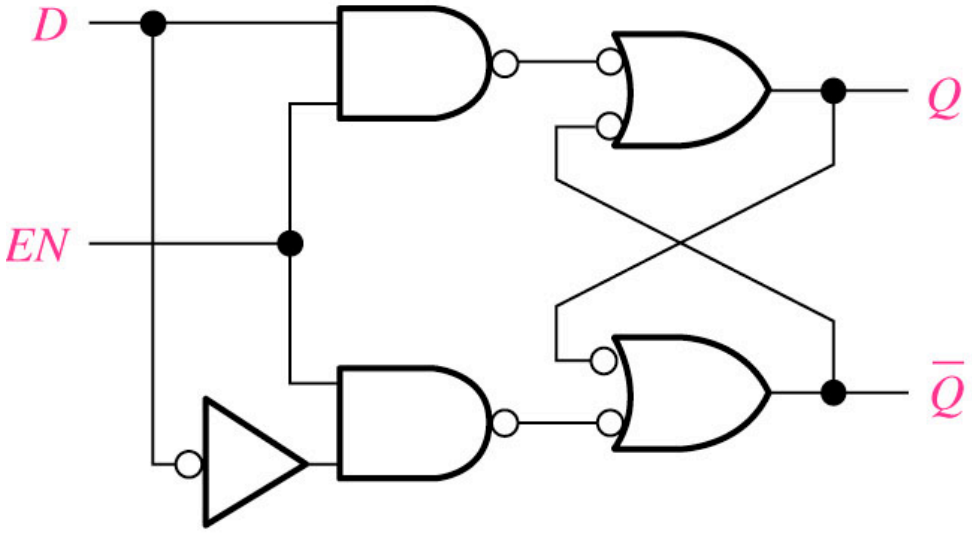
Double check the answer:

Referring to logic diagram above, fill in the table. Assume initially Q = 0 and Q' = 1

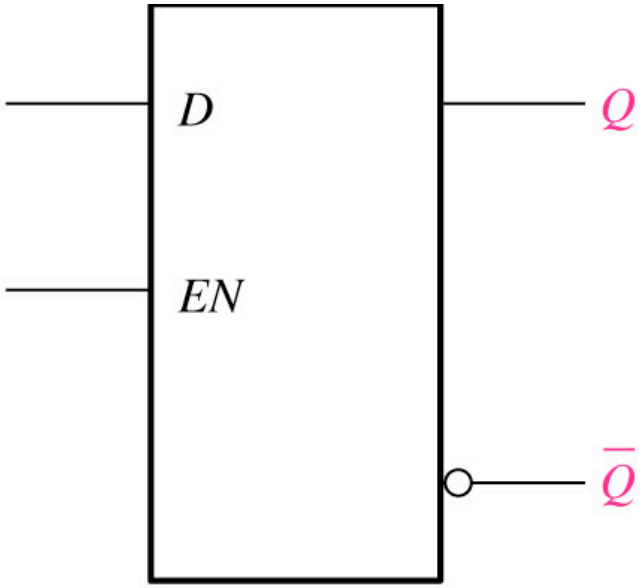
EN	S	R	Y	Z	Q	STATE
0	0	0	1	1	0	HOLD
0	0	1	1	1	0	HOLD
0	1	0	1	1	0	HOLD
0	1	1	1	1	0	HOLD
1	0	0	1	1	0	HOLD
1	0	1	1	0	0	0 (RESET)
1	1	0	0	1	1	1 (SET)
1	1	1	0	0	1	INVALID

Gated D Latch:

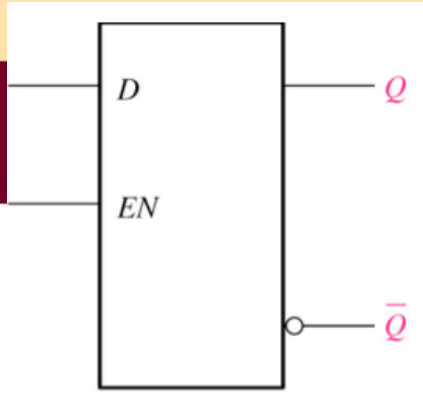
Logic diagram & logic symbol



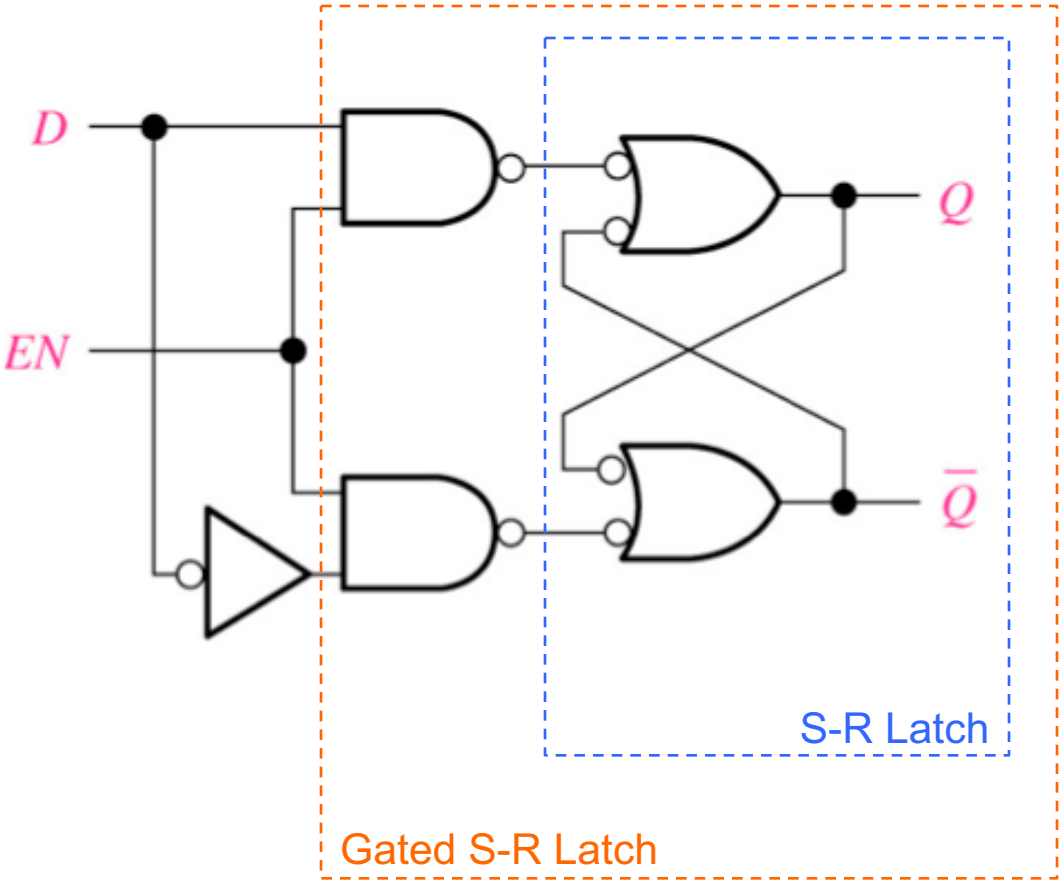
(a) Logic diagram



(b) Logic symbol



Gated D Latch

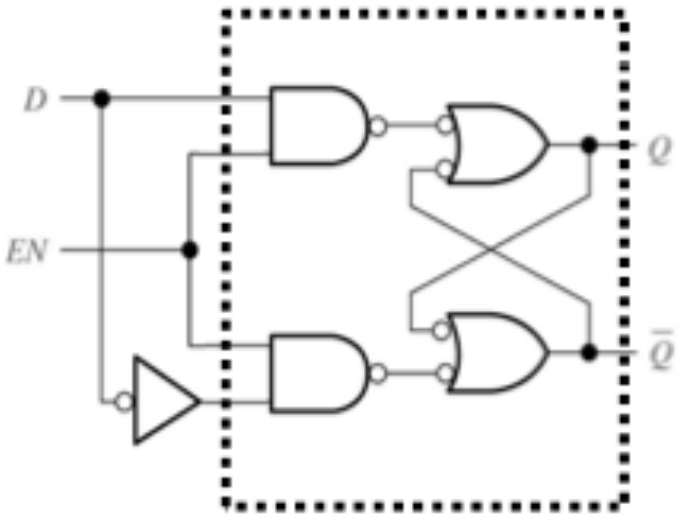


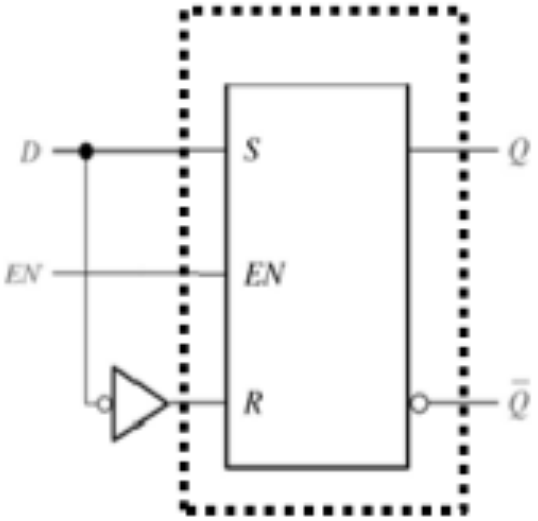
Gated D Latch: Truth Table

EN	D	Output
0	0	No Change
0	1	No Change
1	0	Q = 0
1	1	Q = 1

INFO :

EN = 1, Latch is On
EN = 0, Latch is Off





The purpose of the inverter is to make sure that R is the complement of S and R will never be the same as S. So that, we have only two condition at the input of SR.

Condition 1: D = 0, therefore S = 0, R = 1 which make Q = 0
Condition 2: D = 1, therefore S = 1, R = 0 which make Q = 1

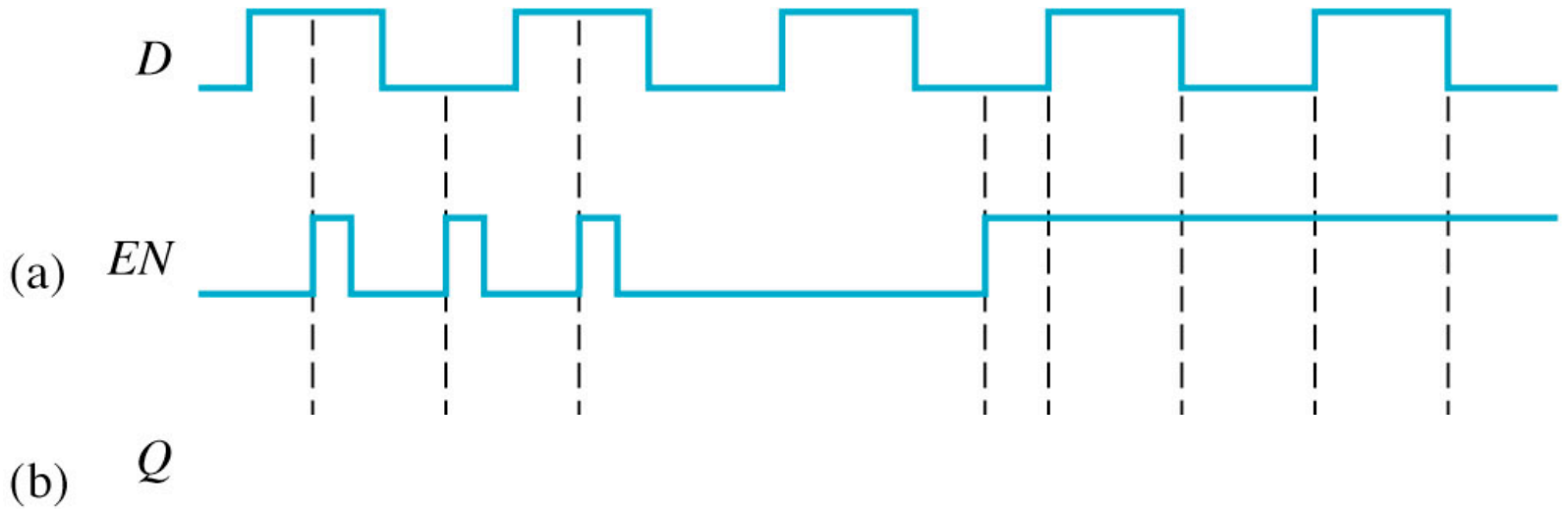
Just like gated SR, when EN=0, the output does not change. BUT, if EN=1, the output will depend on the value of input D.

So, we can conclude that Q=D when EN=1.

EN=1 ☐ Q=D

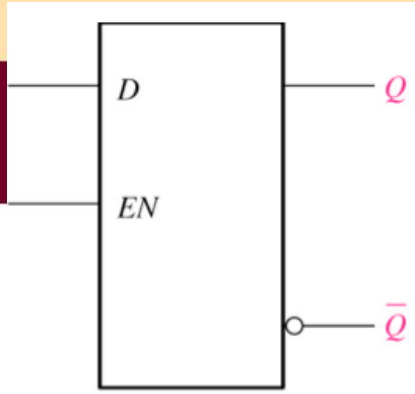
Example: Gated D Latch.

Find the waveform for Q. Assume that Q is initially LOW.

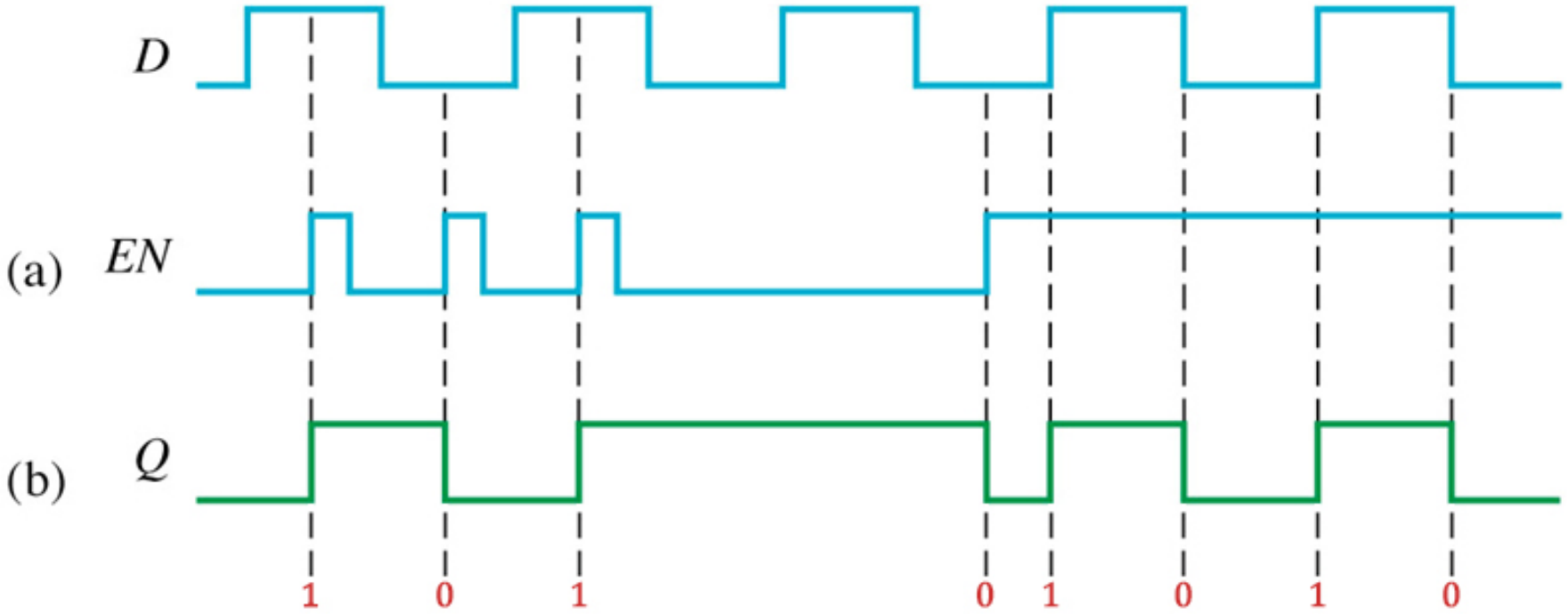


Solution:

EN	D	Output
0	0	No Change
0	1	No Change
1	0	Q = 0
1	1	Q = 1



Logic symbol



Flip-Flops

i) **Edge-Triggered D**
ii) **S-R**
iii) **J-K**
iv) **T (Toggle)**

Edge-Triggered FF

Flip-flop is an important device in a sequential circuit

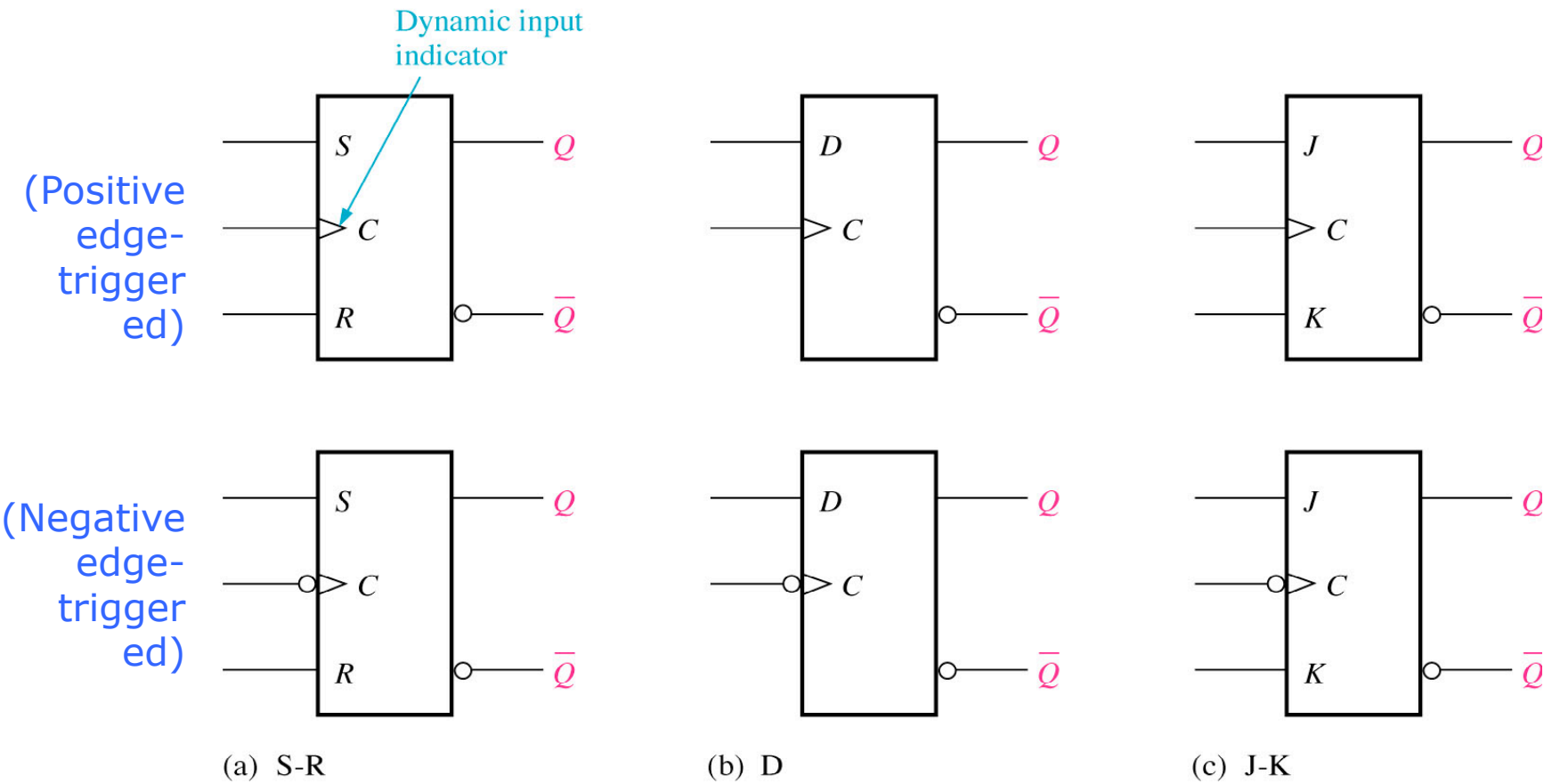
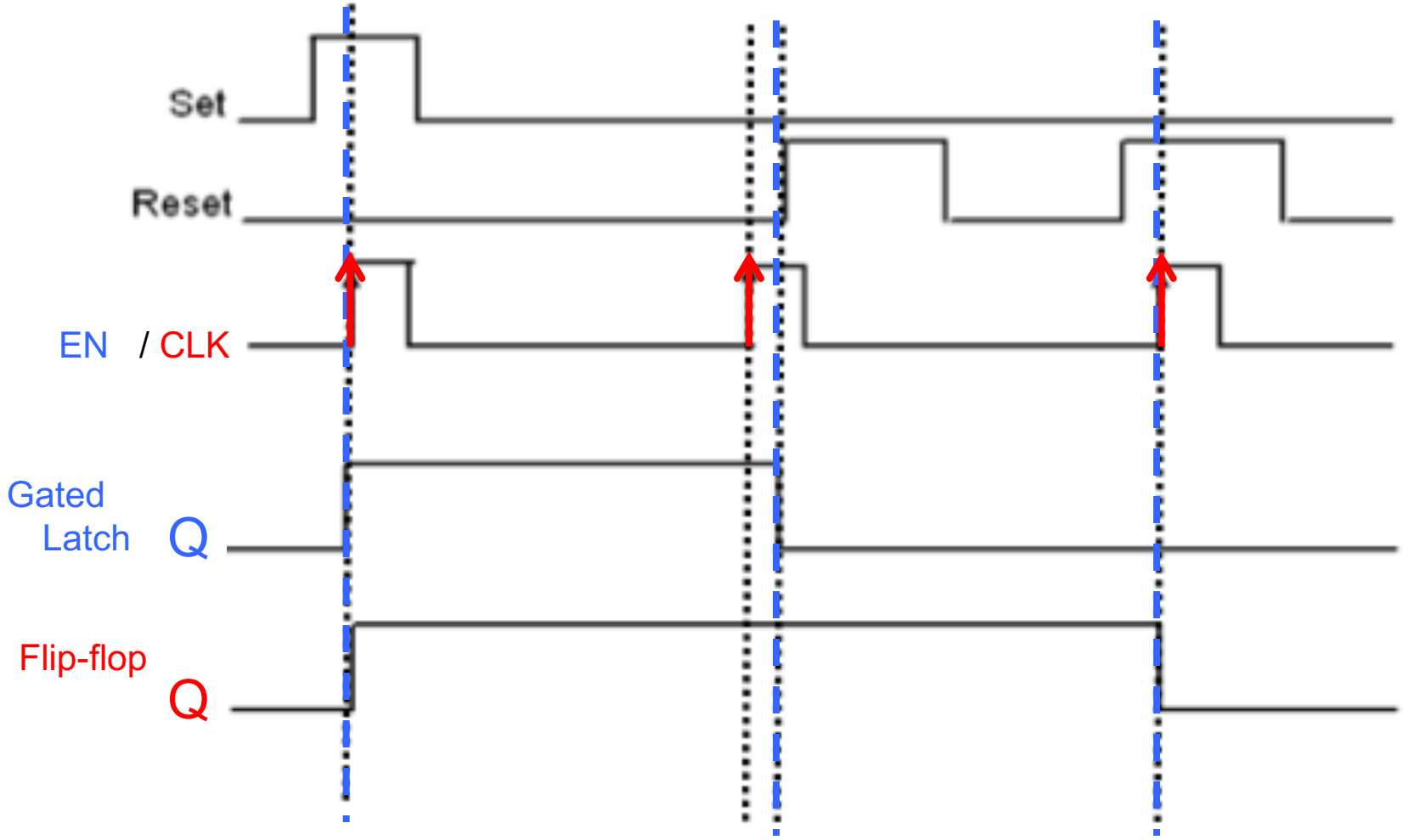


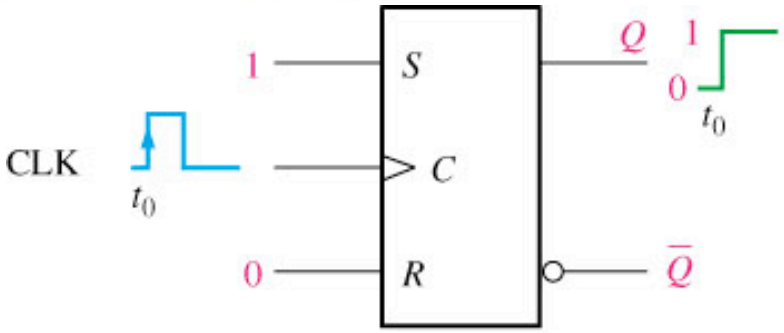
Figure : Edge-Triggered FF logic symbol



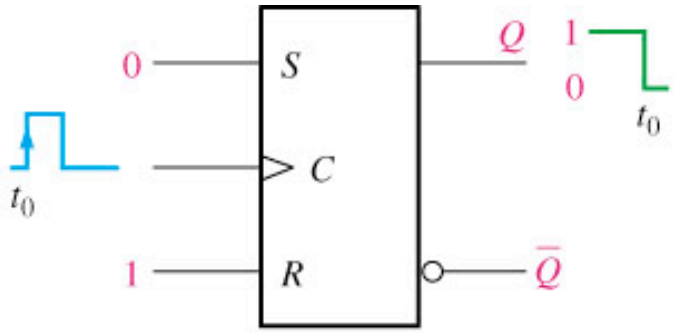
The different between Gated Latch (EN) and Flip-Flop (CLK):

- Gated Latch is activated by using Level-triggered EN (i.e '0' or '1')
- FF is activated by using edge-triggered CLK i.e 'transition from '0 to 1' or '1 to 0')

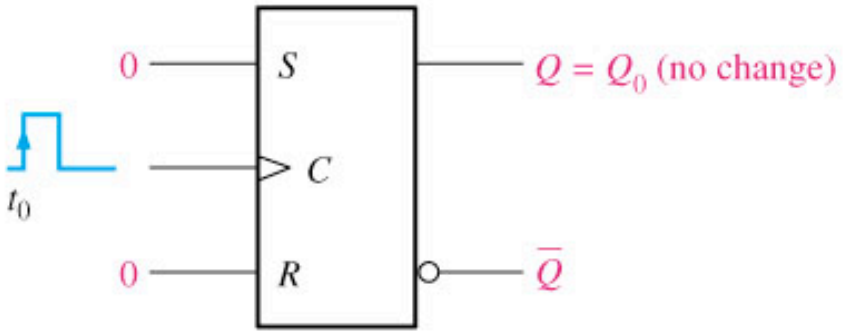
S-R Flip-Flop



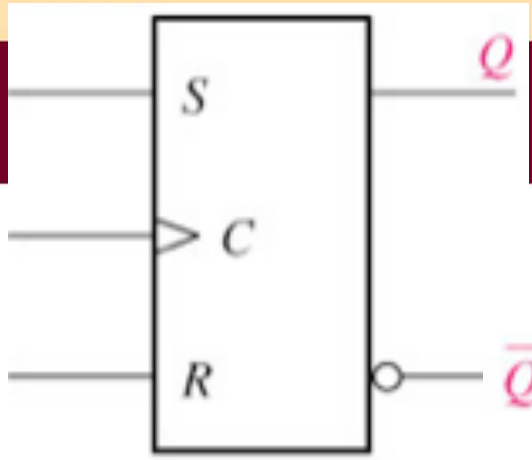
(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0, R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0, R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

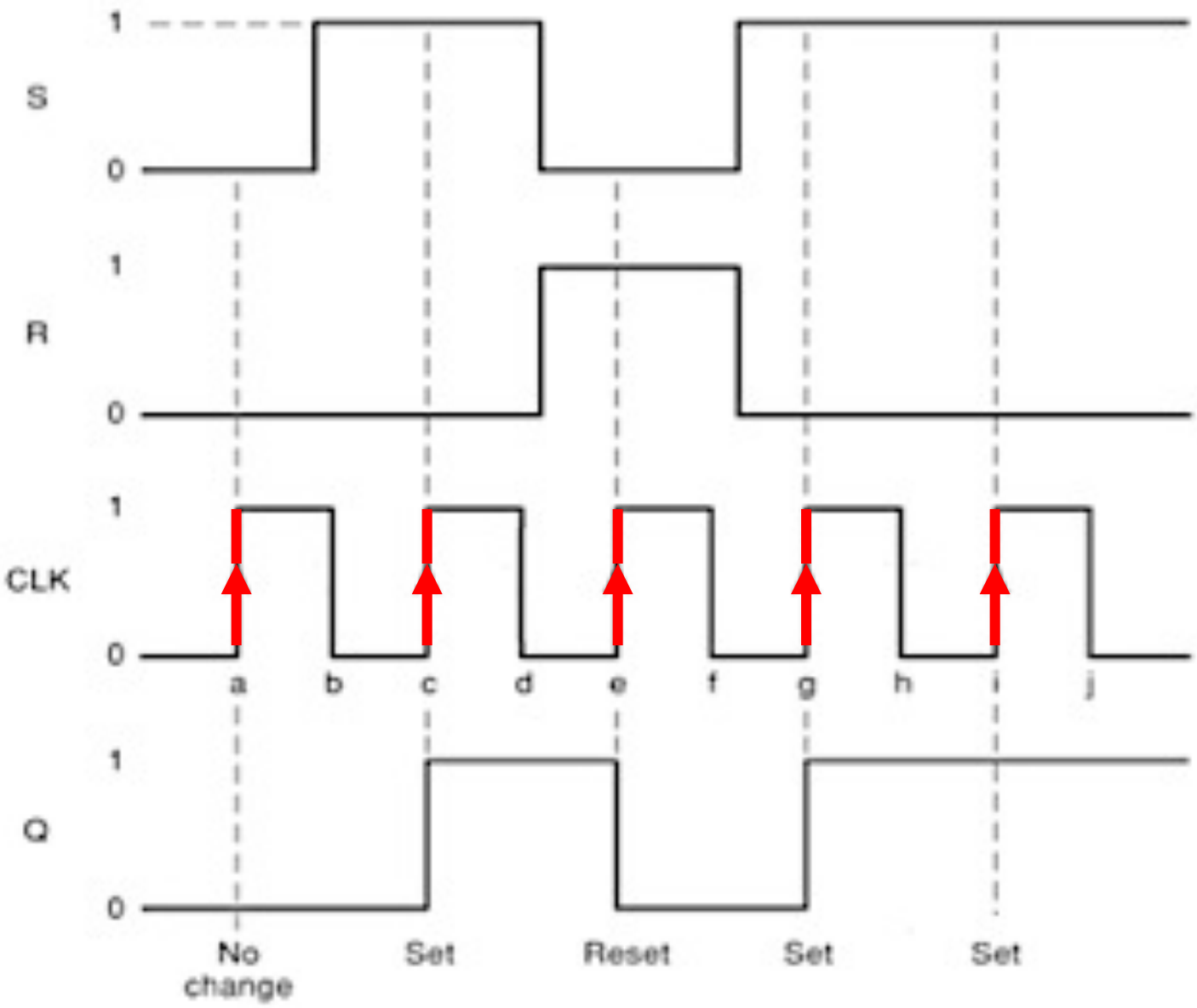


S	R	CLK	Output		Comments
			Q	$\overline{Q}$	
0	0	↑	Q_0	$\overline{Q_0}$	No Change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

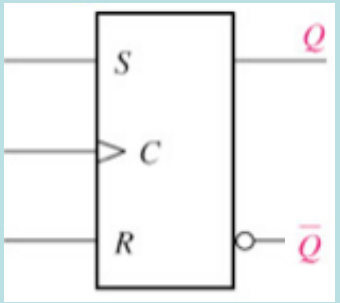
TRUTH TABLE

↑ = clock transition LOW to HIGH

Q_0= output level prior to clock transition



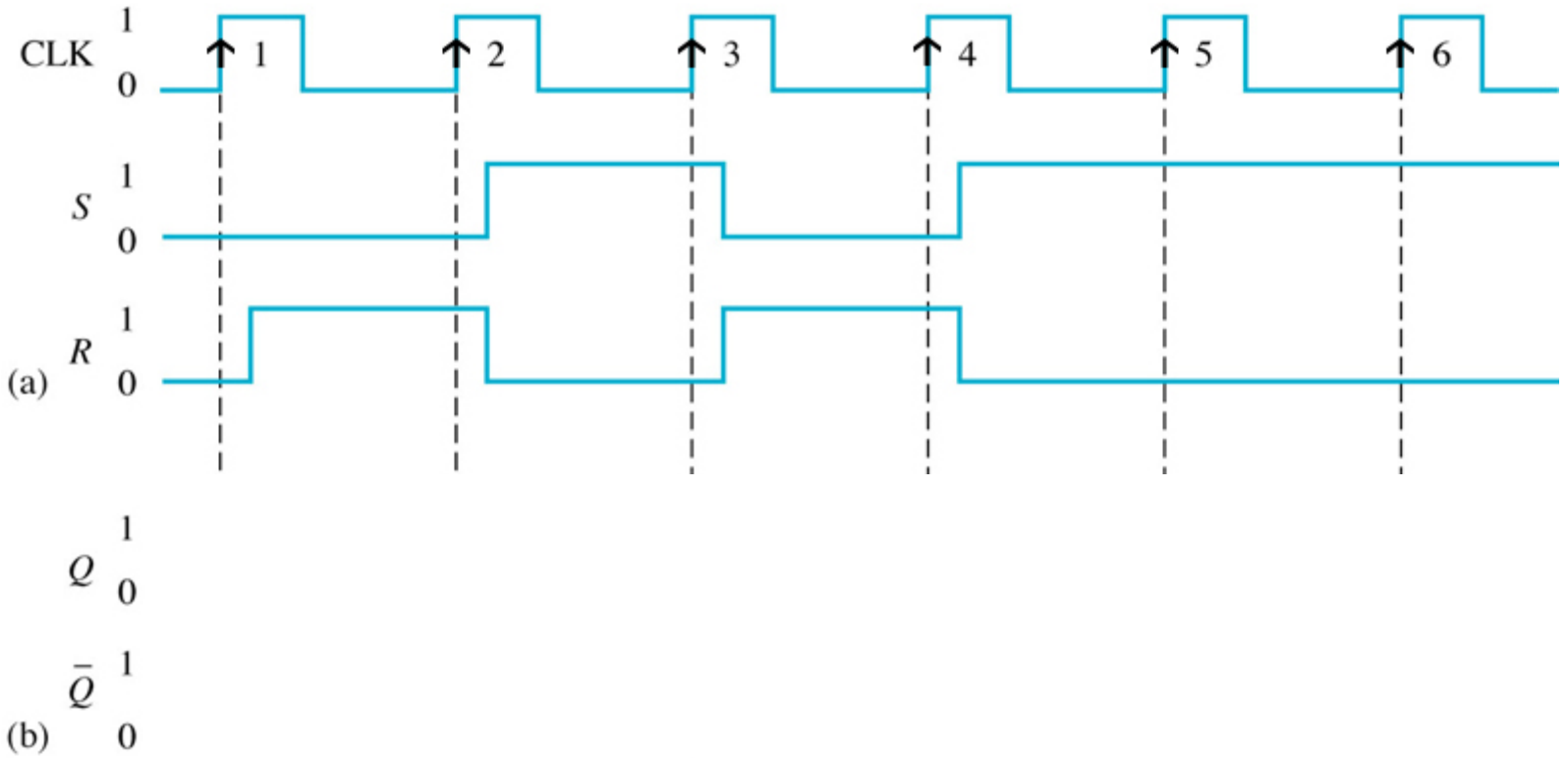
Positive edge-triggered

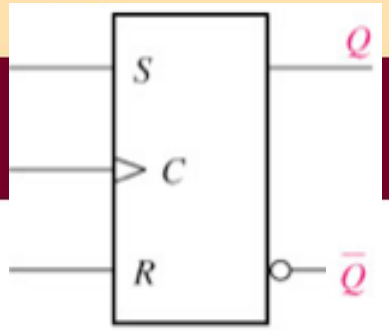


Example: S-R Flip-Flop.

Find the waveform for Q and Q.

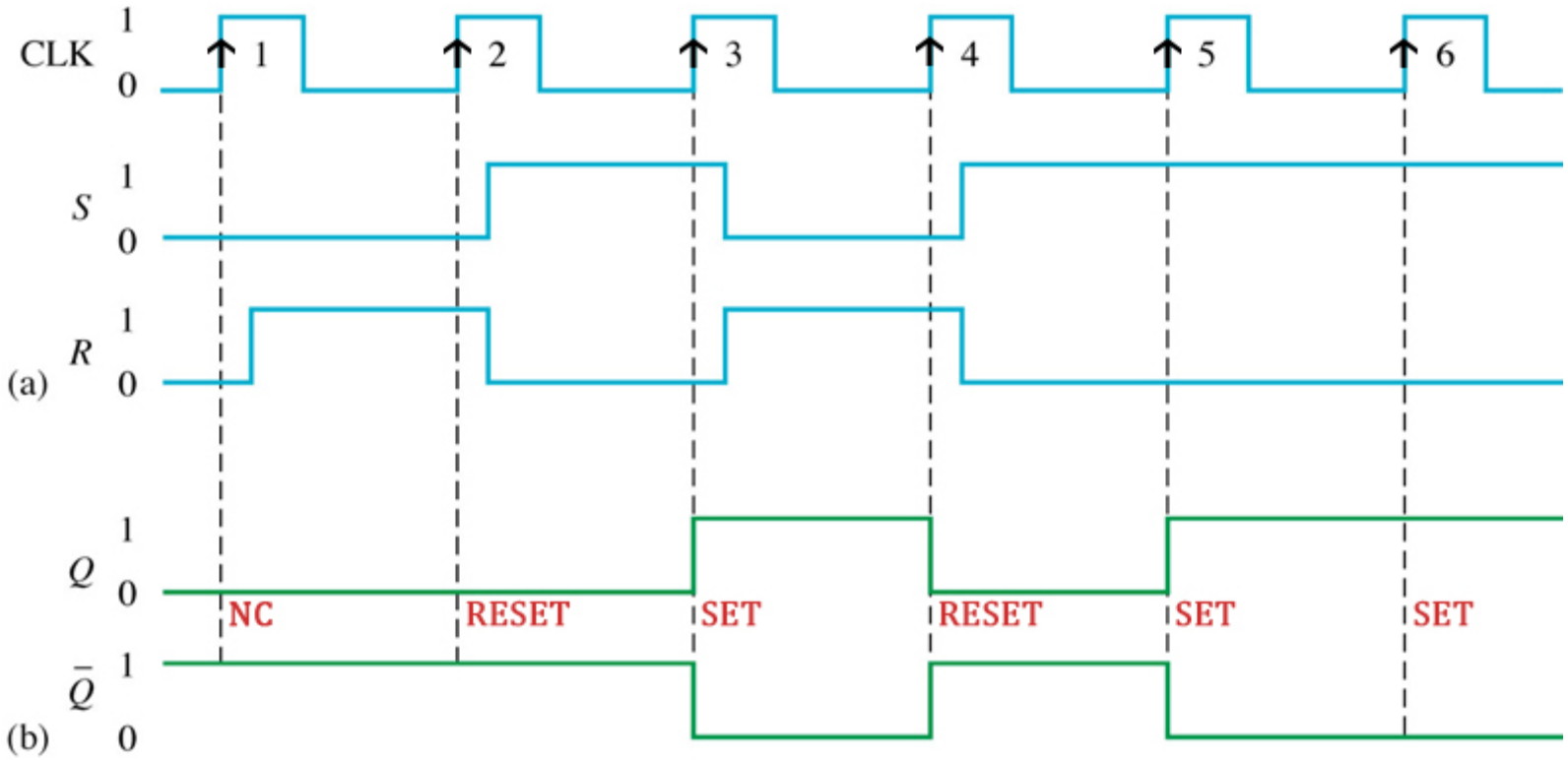
Assume that the the positive edge-triggered flip-flop is initially RESET.

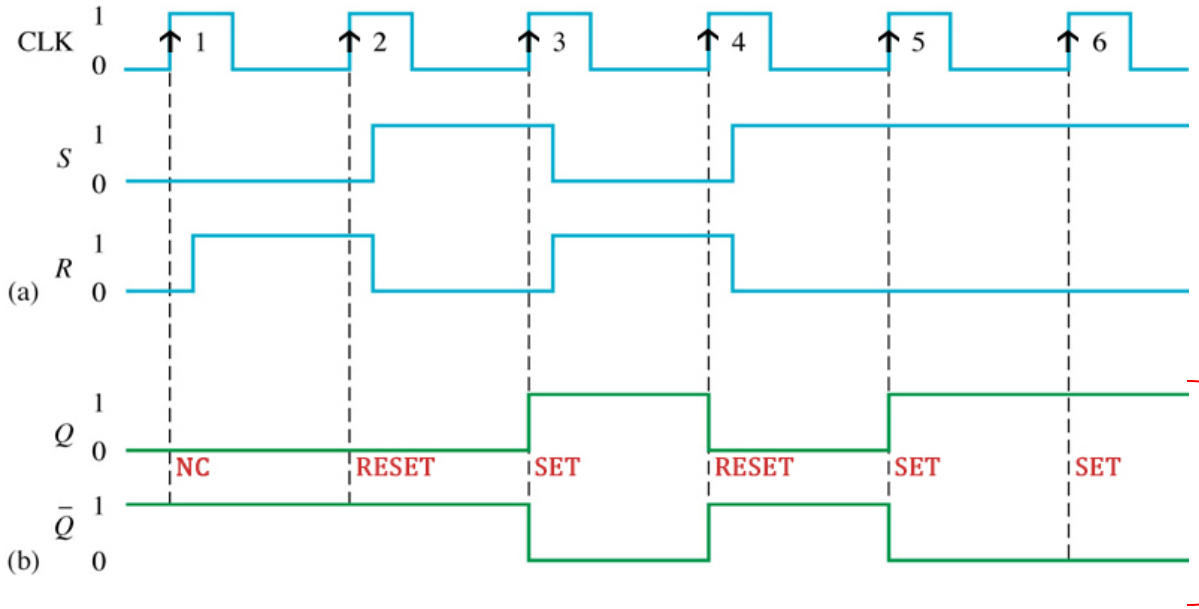




Logic symbol

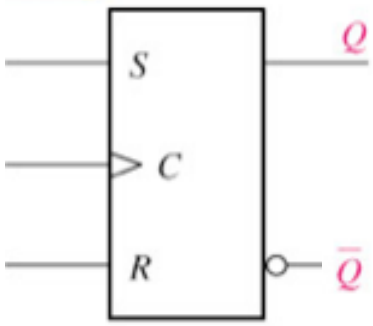
Solution:





Once Q is determined, Q' is easily found since it is simply the complement of Q.

Clock Pulse	S	R	Q
1	LOW	LOW	Does not change
2	LOW	HIGH	LOW (RESET)
3	HIGH	LOW	HIGH (SET)
4	LOW	HIGH	LOW (RESET)
5	HIGH	LOW	HIGH (SET)
6	HIGH	LOW	Stay HIGH

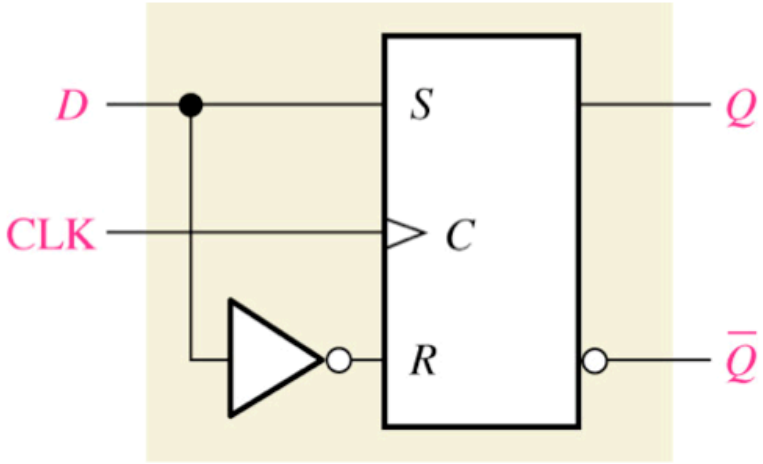


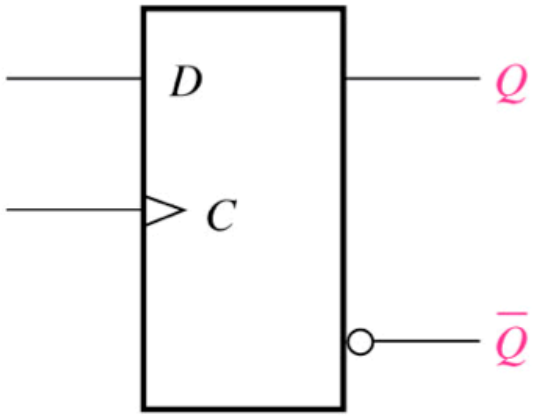
Logic symbol

D Flip-Flop

D ☐ Data or Delay

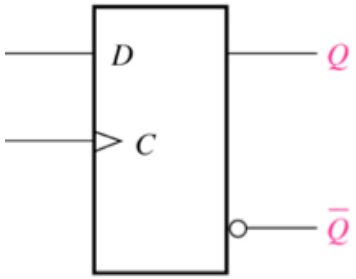
- D FF is useful when a single data bit (1 or 0) is to be stored.
- The addition of an inverter to an S-R FF creates basic D FF where a positive edge-triggered type is shown.





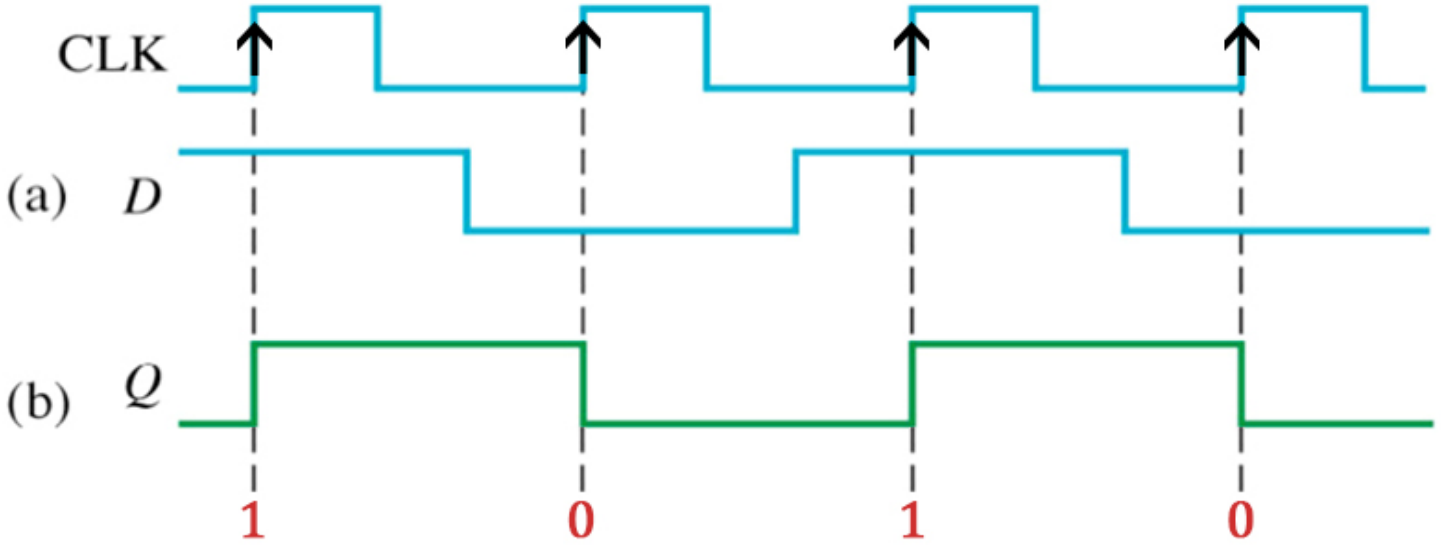
Logic symbol

INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	$\overline{Q}$	
1	↑	1	0	SET (store a 1)
0	↑	0	1	RESET (store 0)



Logic symbol

(for positive edge-triggered)

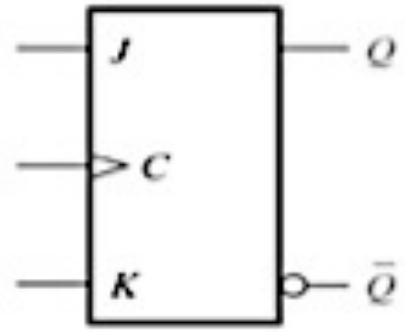


Remember, Q follows D at the active or triggering clock edge.

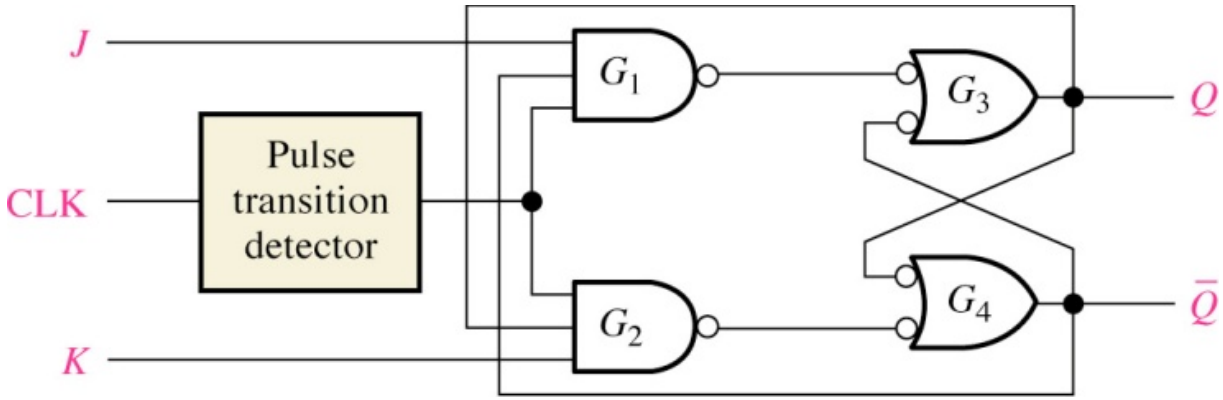
J-K Flip-Flop

- The JK FF is versatile and is a widely used type of FF.
- The difference between J-K and S-R:

J-K has no invalid state as S-R.



Logic Symbol

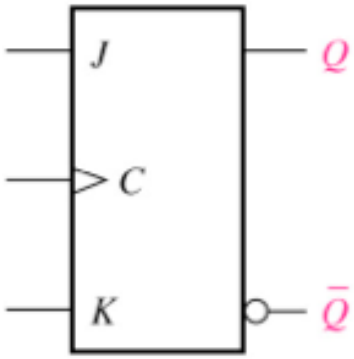


J	K	CLK	Output		Comments
			Q	$\overline{Q}$	
0	0	↑/↓	Q_0	$\overline{Q_0}$	No Change
0	1	↑/↓	0	1	RESET
1	0	↑/↓	1	0	SET
1	1	↑/↓	Q_0	Q_0	Toggle

TRUTH TABLE

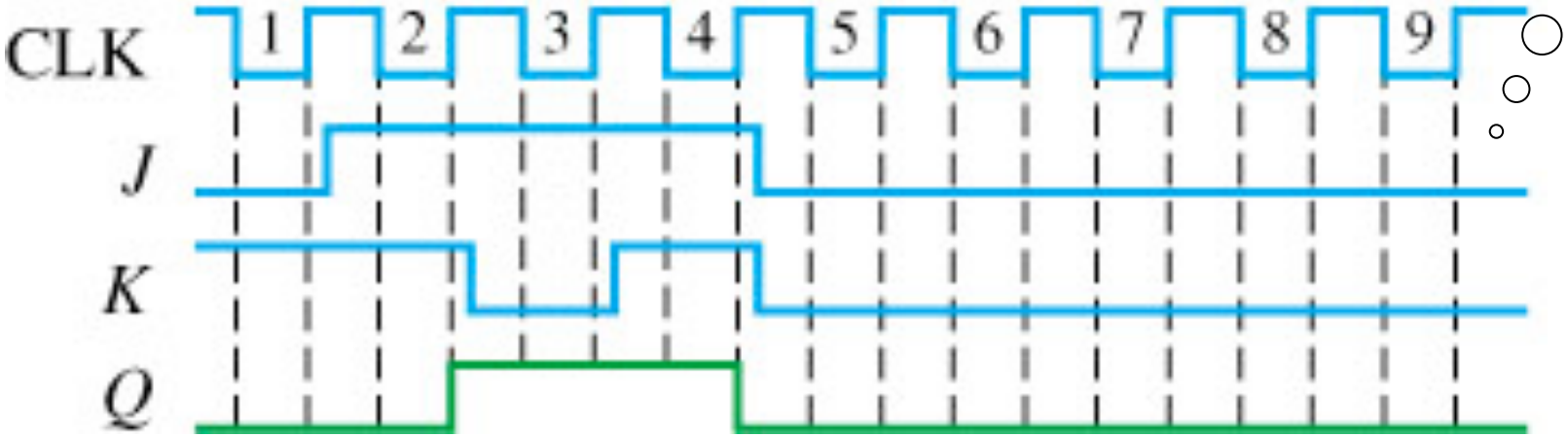
↑ = clock transition LOW to HIGH

Q_0= output level prior to clock transition



Logic symbol

Positive or negative triggered ?

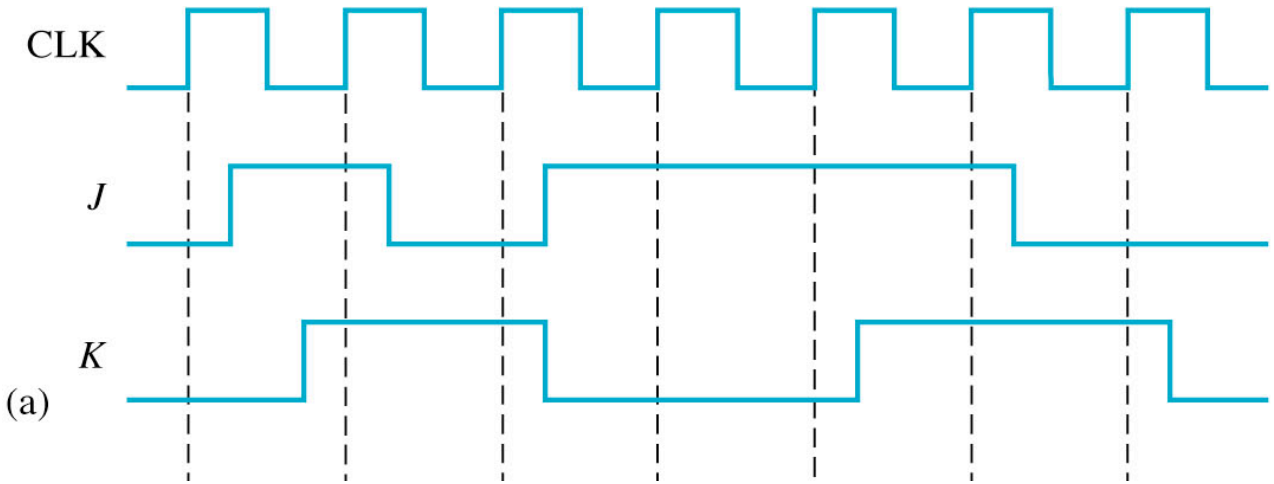


Example: J-K Flip-Flop.

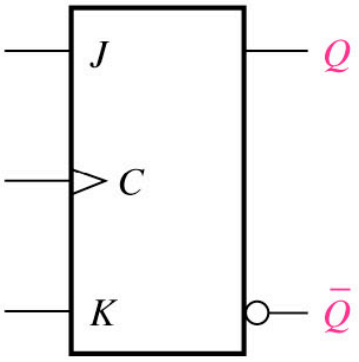
Find the waveform for Q.

Assume that Q is initially LOW.

Positive or negative triggered?



(a)

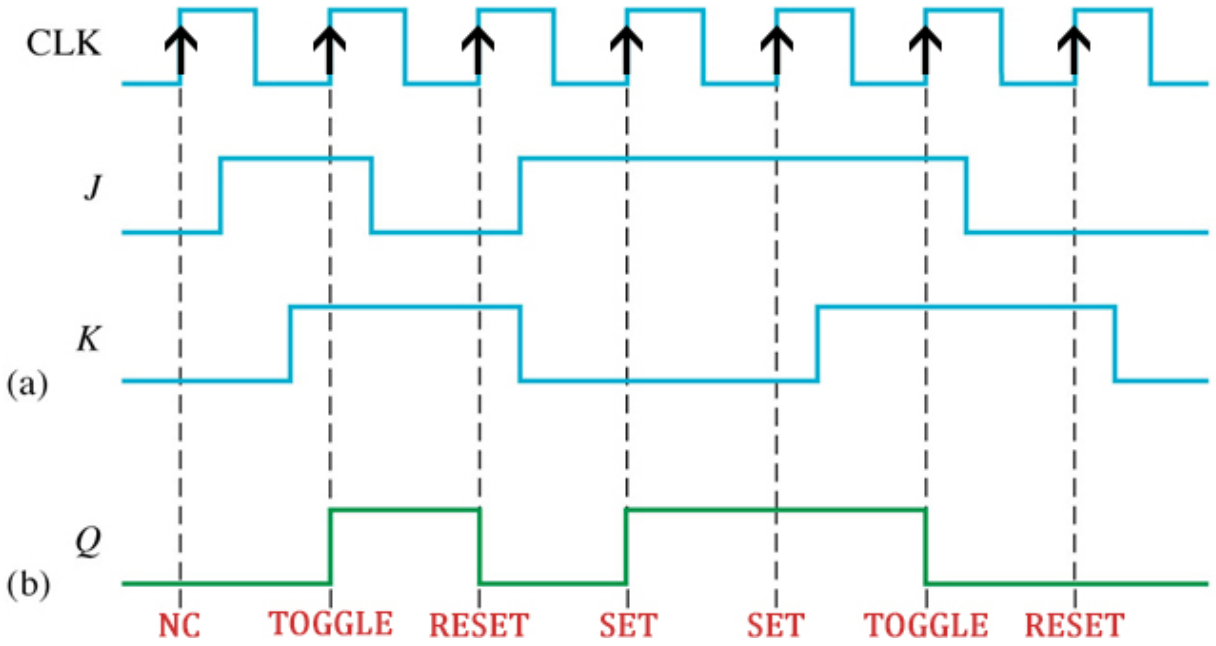


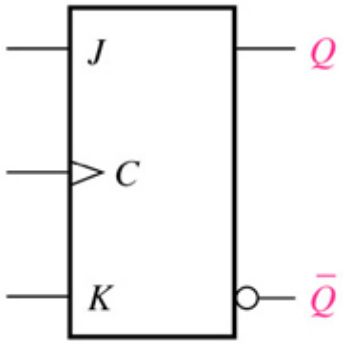
Logic symbol

(b)

Positive trigger ed

Solution:





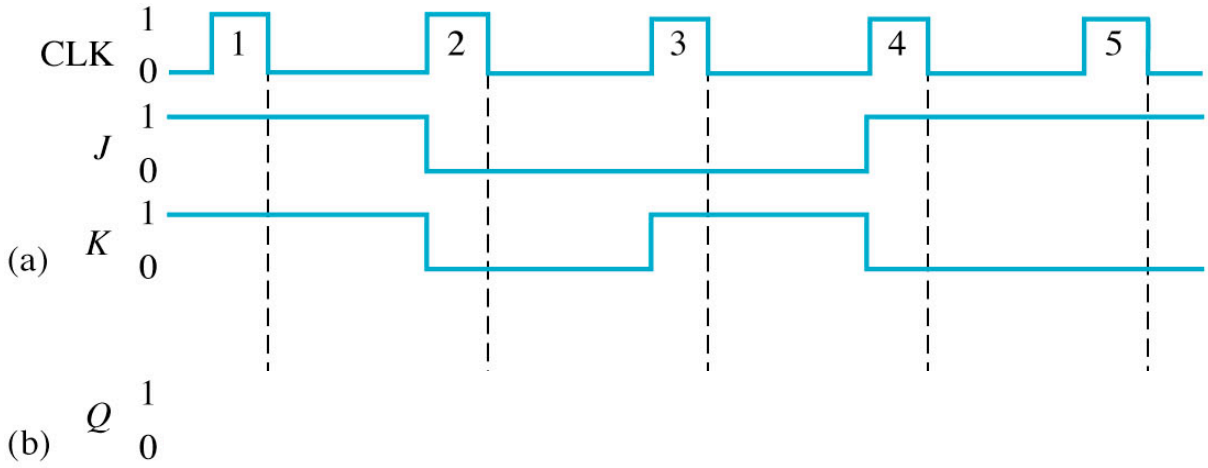
Logic symbol

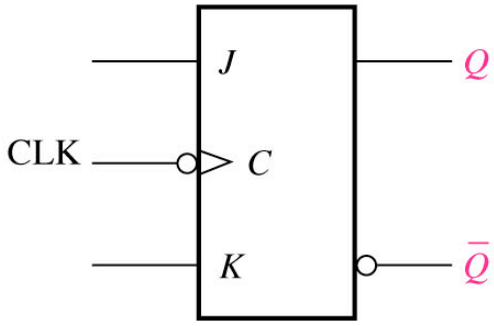
Example: J-K Flip-Flop.

Find the waveform for Q.

Assume that Q is initially LOW.

Positive or negative triggered?

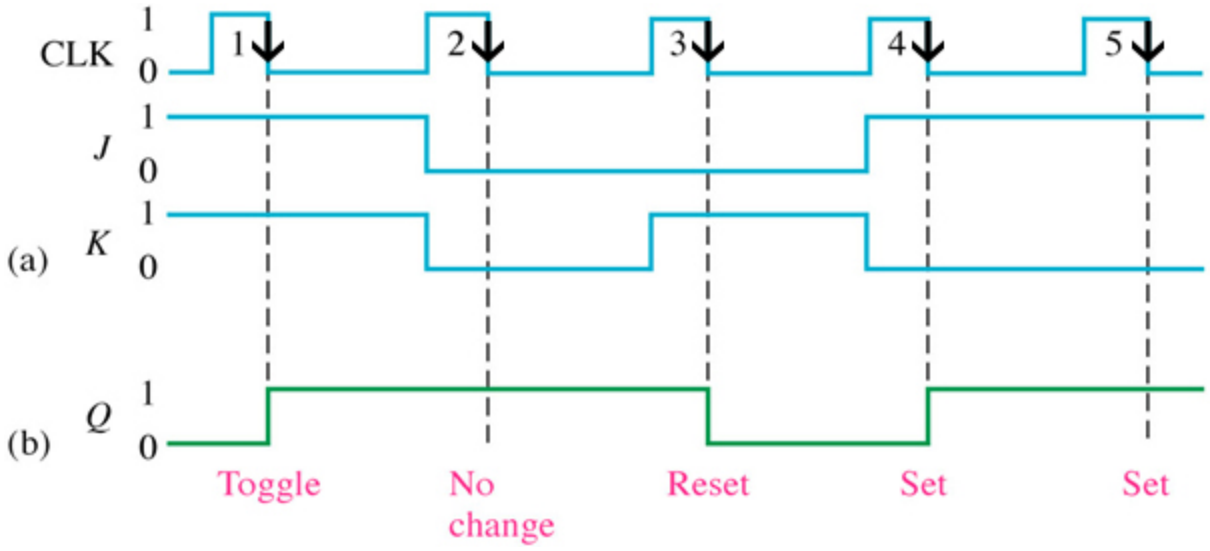


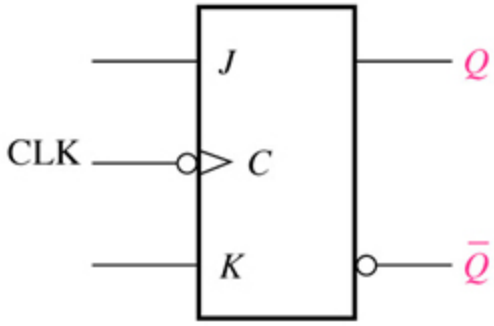


Logic symbol

negative trigger ed

Solution:

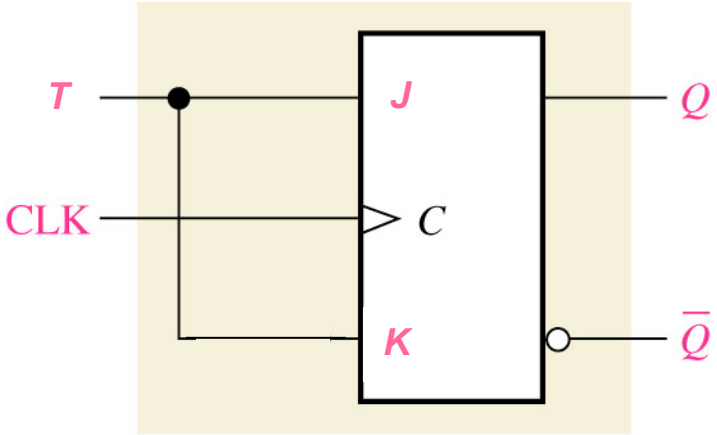


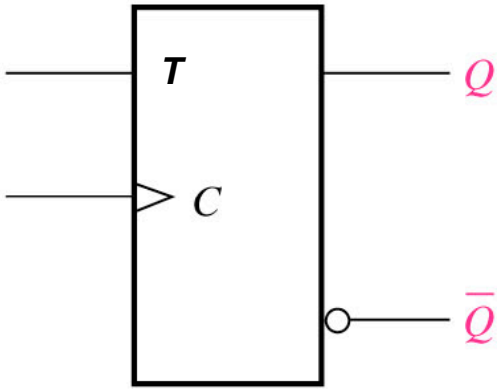


Logic symbol

T Flip-Flop

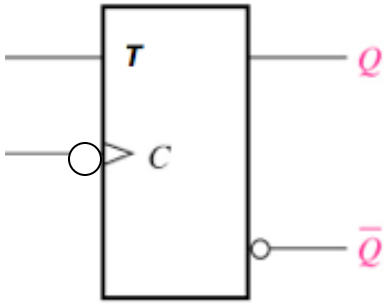
- Also called as toggle flip flop.
- Frequently used in building counters





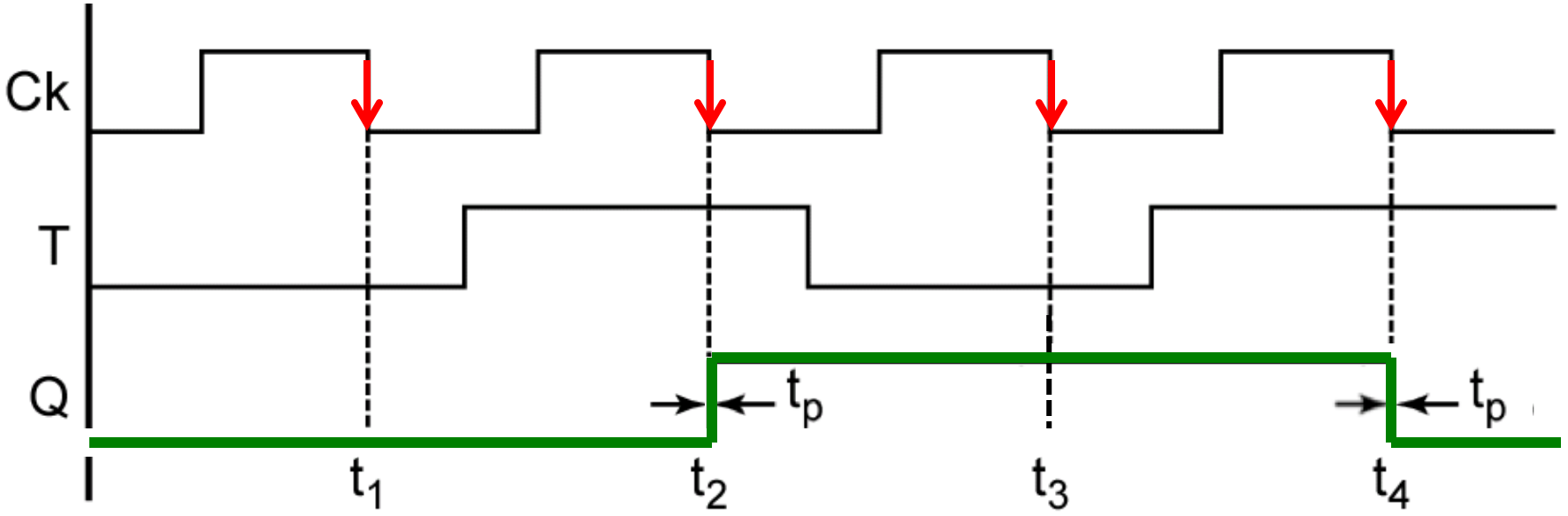
Logic Symbol

T	CLK ↑/↓	Output Q	Output $\overline{Q}$	Comments
0	↑/↓	0	0	HOLD
0	↑/↓	1	1	HOLD
1	↑/↓	0	1	TOGGLE
1	↑/↓	1	0	TOGGLE



Logic symbol

Timing Diagram for T Flip-Flop (Negative-Edge Trigger)

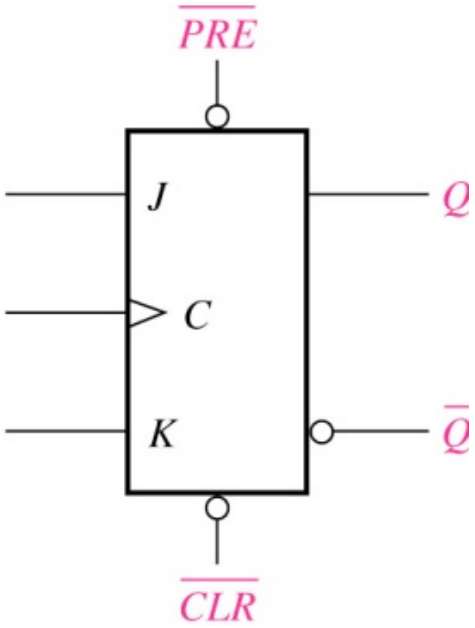


FF Asynchronous Input

- Synchronous → inputs transferred on the triggering edge of the clock
- Asynchronous → inputs effect FF state independent of the clock
  - Normally labeled (depends on the manufacturer)

Preset $\overline{PRE}$ or direct SET
Clear $\overline{CLR}$ or direct RESET

$\overline{PRE}$	$\overline{CLR}$	FF	MODE
0	1	SET	Asynchronous
1	0	RESET	Asynchronous
1	1	JK	Synchronous



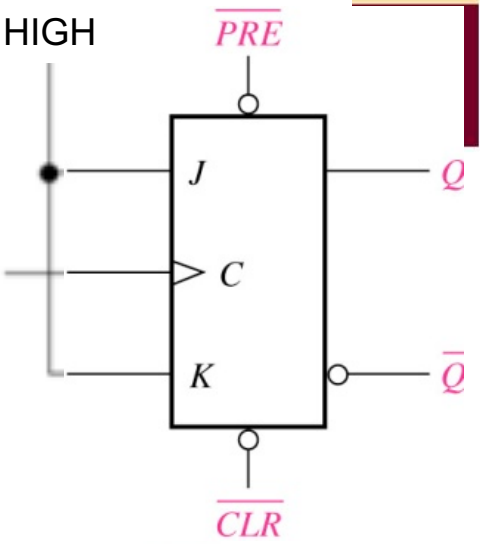
- Flip-flop input priority:

Priority	FF Input	
Highest	$\overline{PRE}, \overline{CLR}$	(Asynchronous input)
Medium	Clock	
Lowest	S-R, J-K, D, T	(Synchronous input)

- Flip-flop asynchronous input has the highest priority.
  - Which means that if the asynchronous input active, the output will immediately change regardless the value of synchronous input or clock.

- There are two types of asynchronous input:
  - preset , $\overline{\text{PRE}}$ - to set initial value of 1 to the output
  - clear, $\overline{\text{CLR}}$ - to reset the output to 0

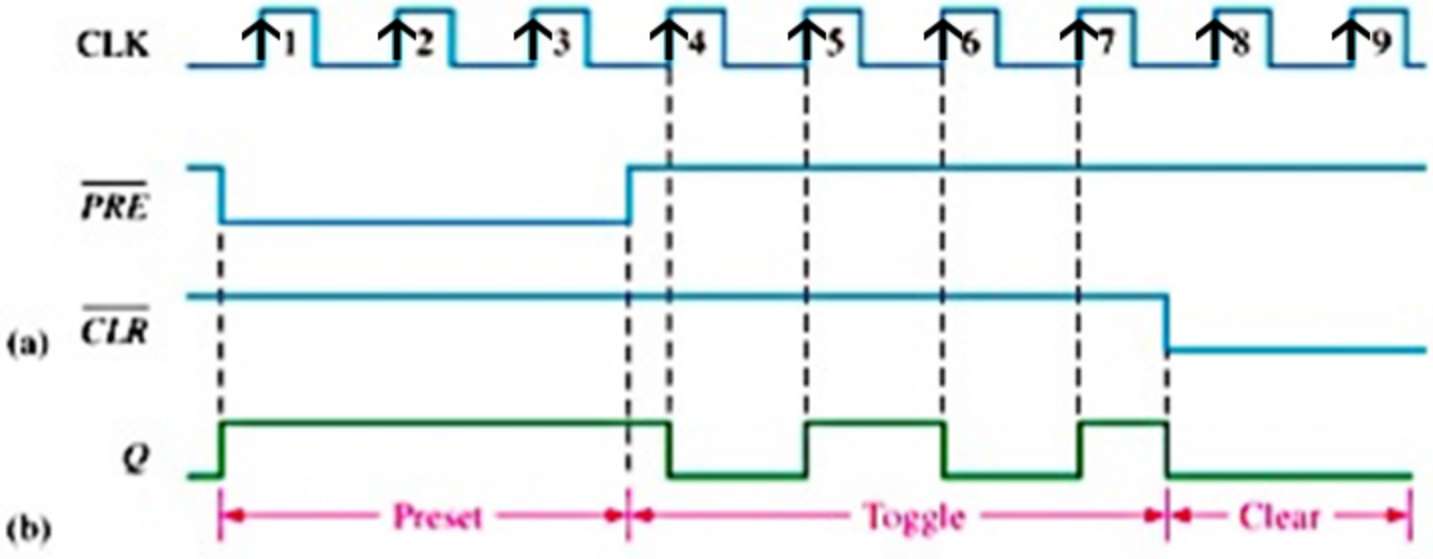
Note:
When J=K=1, it works as T flip-flop



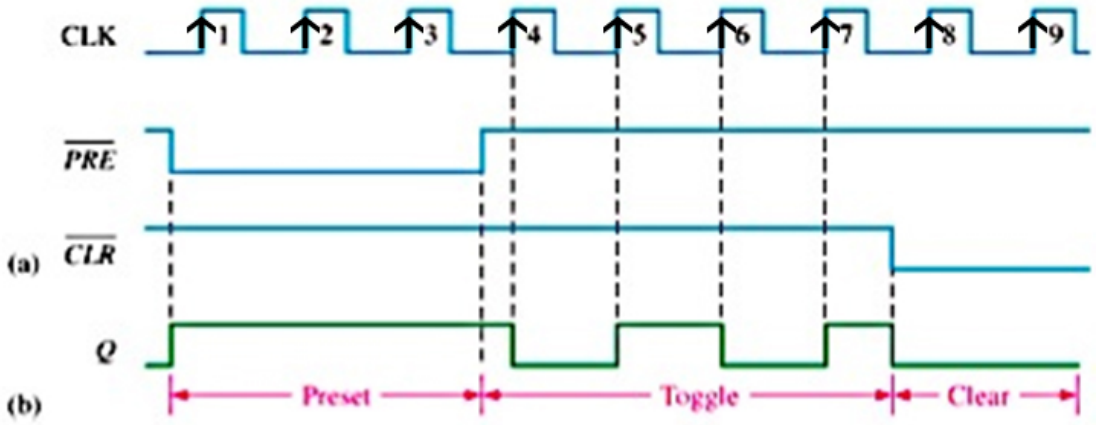
Example: J-K Flip-Flop.

Find the waveform for Q.

Assume that Q is initially LOW.



$\overline{PRE}$	$\overline{CLR}$	FF	MODE
0	1	SET	Asynchronous
1	0	RESET	Asynchronous
1	1	JK	Synchronous



Q

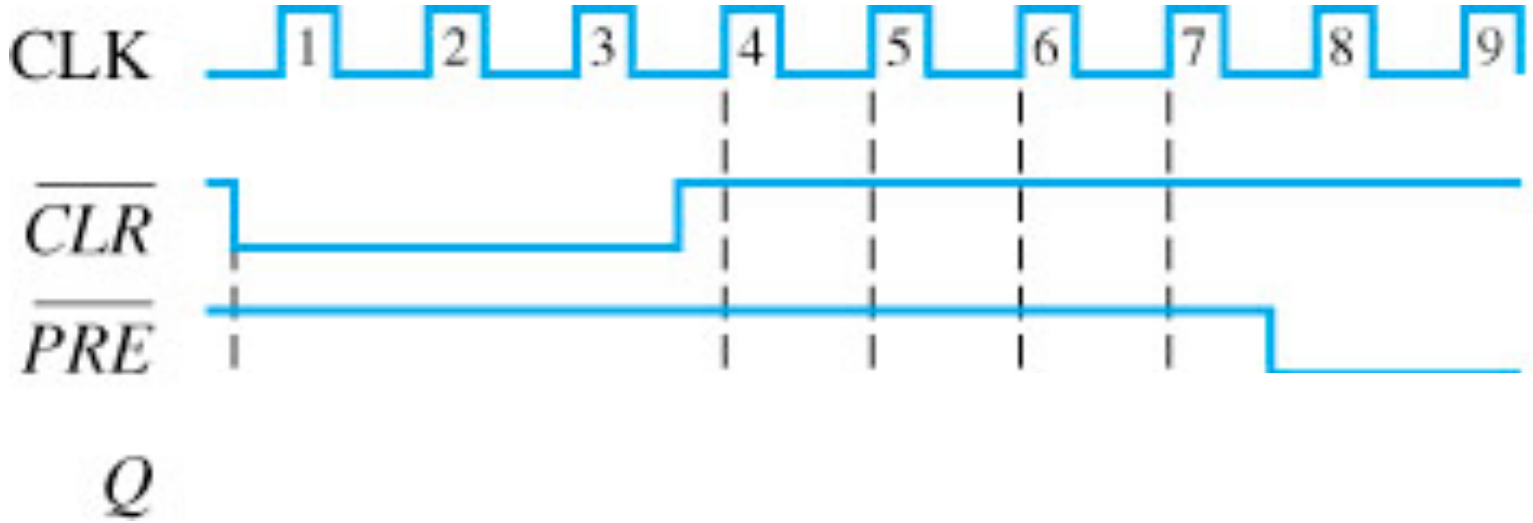
clk pulse	$\overline{PRE}$	$\overline{CLR}$	J	K	FF	Comment
1,2,3	0	1	1	1	SET	JK inputs - dont care
4,5,6, 7	1	1	1	1	Toggle	Synchronous mode.
8,9	1	0	1	1	RESET	JK inputs - dont care

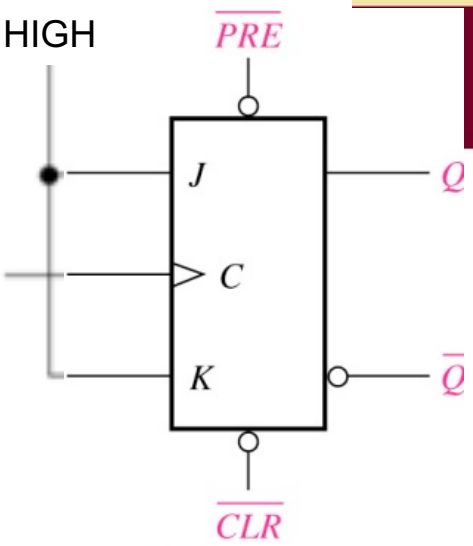
Positive or negative triggered?

Exercise 7.3: $\overline{PRE}$ and $\overline{CLR}$

Find the waveform for Q.

Assume that Q is initially LOW.

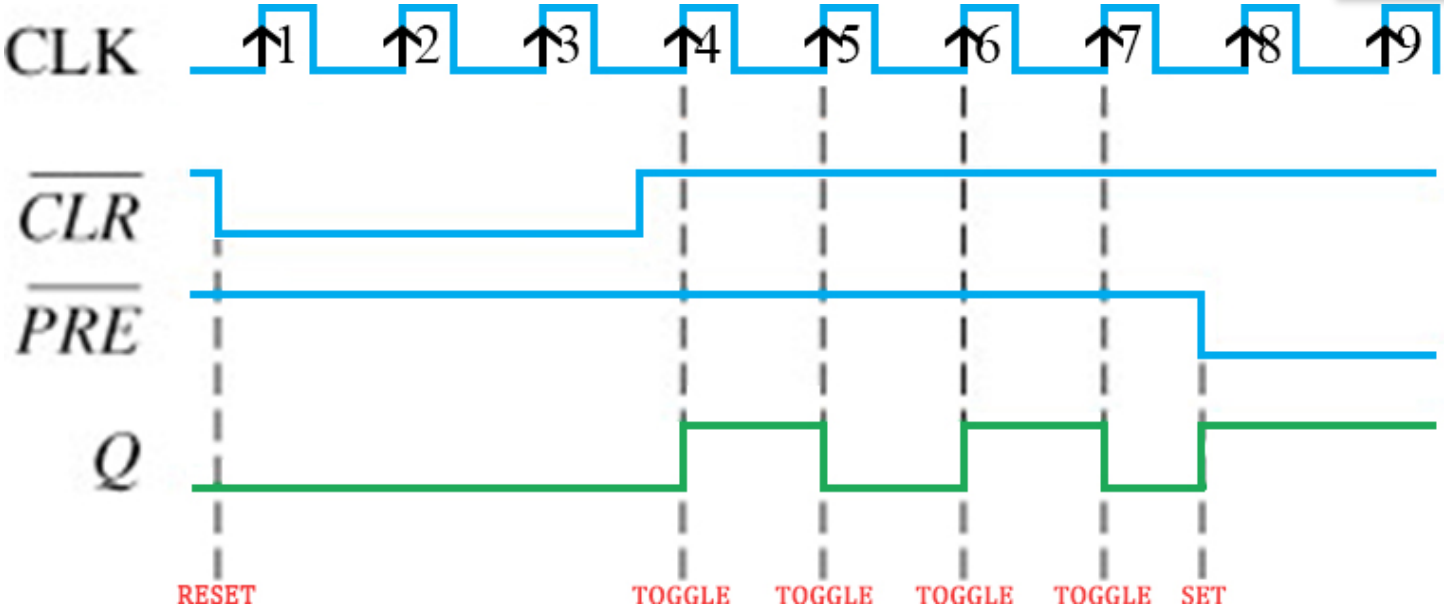




Positive triggered

Note:
When J=K=1, it works as T flip-flop

Solution:



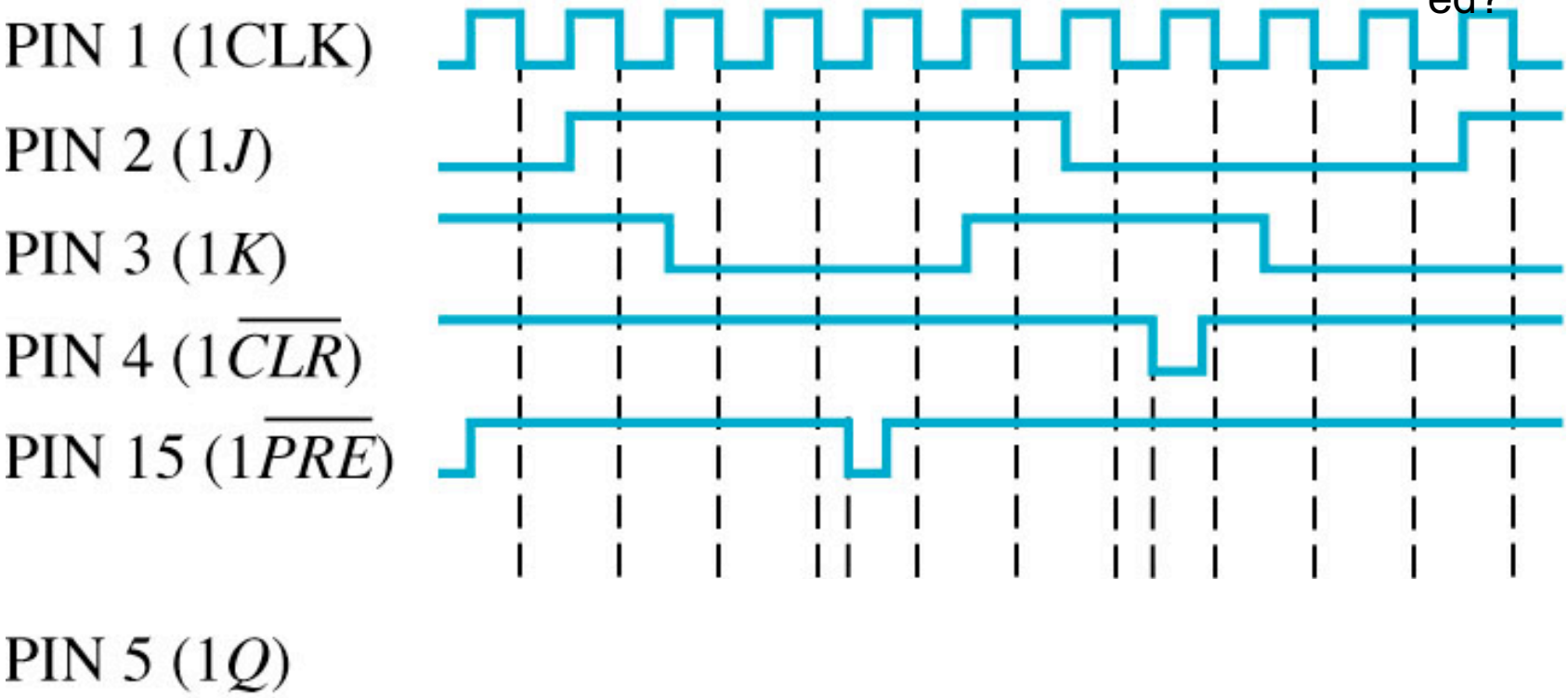
Extra

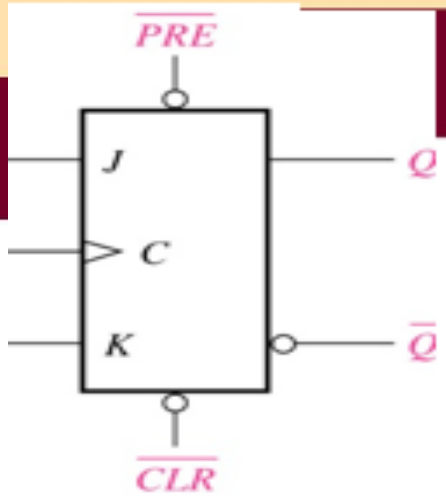
Positive or negative triggered?

Exercise 7.4: $\overline{PRE}$ and $\overline{CLR}$

Find the waveform for Q.

Assume that Q is initially HIGH.

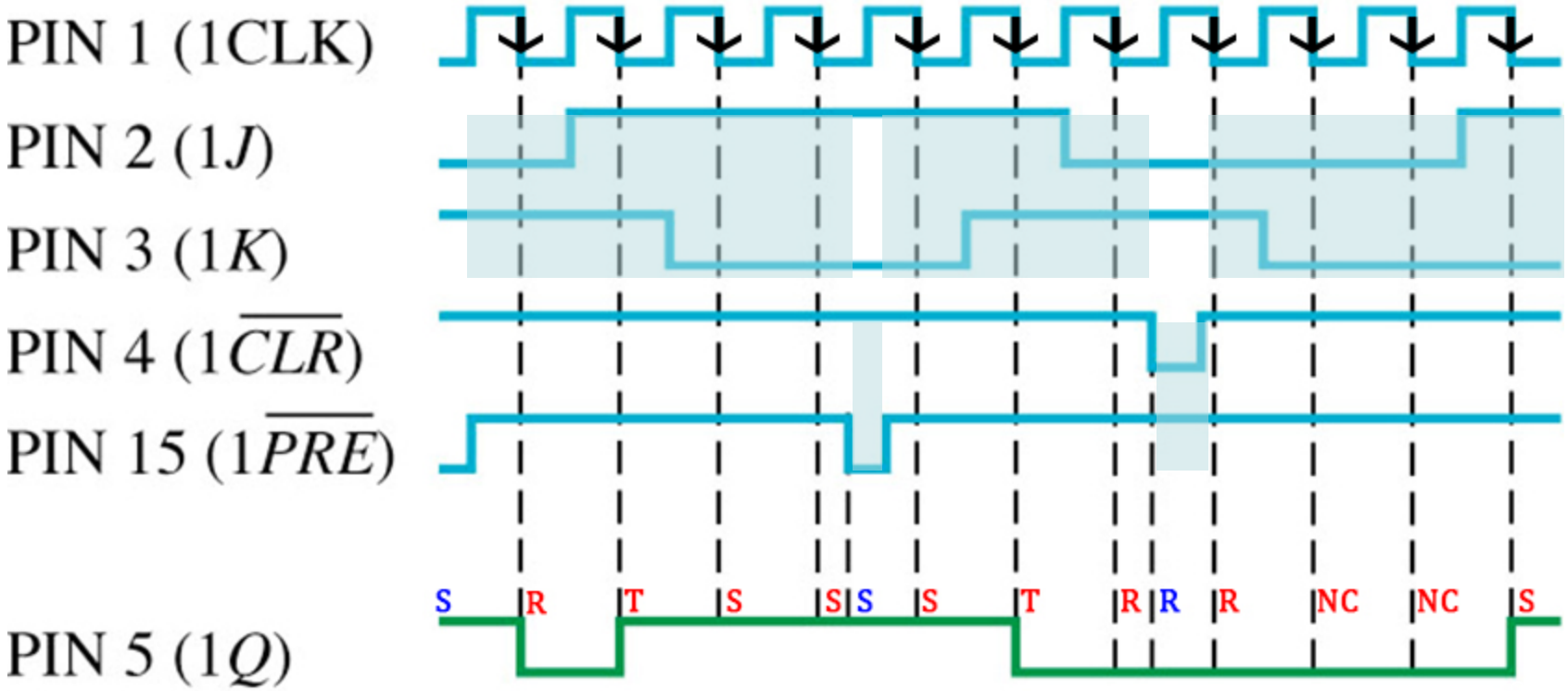




Note:
When J=K=1, it works as T flip-flop

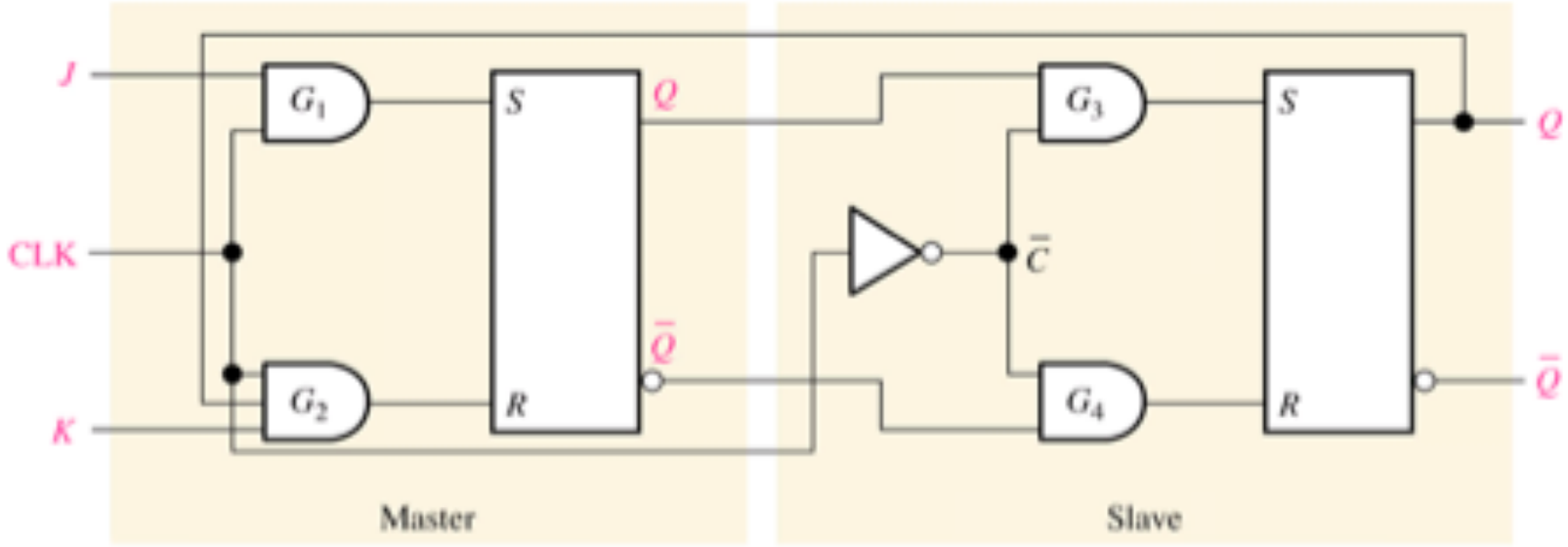
Negative trigger ed
Input Flip-flop, Q

Solution:



Extra notes :
Master Slave Flip Flops (JK Example)

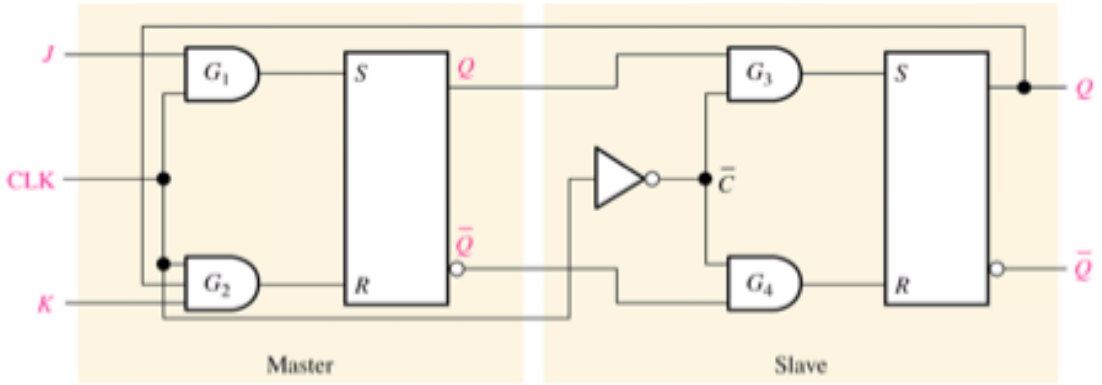
- This type of Flip-flop is already obsolete, the mention here is for the sake of completeness
- You must know it exist, where you might find in the old circuit board.



There are 2 sections called as :

Master section - a) External JK input, b) A gated latch

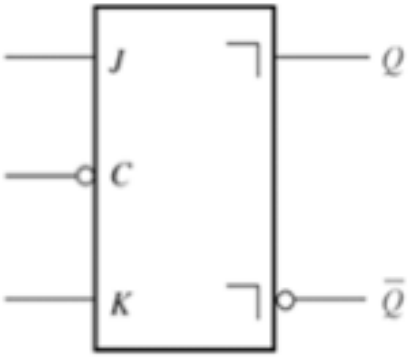
Slave section - a) Inputs = outputs of Master, b) Inverted clock pulse



Master-slave flip-flop:

- Another class of flip-flop is the pulse-triggered or master-slave. These flip-flops are constructed from two separate flip-flops. The term pulse-triggered means that data are entered into the flip-flop on the leading edge of the clock pulse, but the output does not reflect the input state until the trailing edge of the clock pulse. This is due to the master flip-flop being rising edge triggered and the slave flip-flop being falling edge triggered as illustrated in the above slide.
- A type of clocked flip-flop consisting of master and slave elements that are clocked on complementary transitions of the clock signal.
- Data is only transferred from the master to the slave, and hence to the output, after the master-device outputs have stabilized.
- This eliminates the possibility of ambiguous outputs, which can occur in single-element flip-flops as a result of propagation delays of the individual logic gates driving the flip-flops.

- The logic symbol for the master-slave flip-flop only indicates the initial inputs to the master and the outputs from the slave



Logic symbol for J-K master-slave flip-flop

J	K	C	Q	$\bar{Q}$	Operation
0	0	Pulse	Q_0	$\overline{Q_0}$	Hold (no change)
0	1	Pulse	0	1	Reset
1	0	Pulse	1	0	Set
1	1	Pulse	$\overline{Q_0}$	Q_0	Toggle

Truth table for J-K master-slave flip-flop

- J-K master slave flip-flop have the same characteristic with the edge triggered J-K , the only difference is how it was triggered and when the input evaluated and the effect appear at the output

J	K	C	Q	$\overline{Q}$	Operation
0	0	Pulse	Q_0	$\overline{Q_0}$	Hold (no change)
0	1	Pulse	0	1	Reset
1	0	Pulse	1	0	Set
1	1	Pulse	$\overline{Q_0}$	Q_0	Toggle