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##### SULIT

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UNIVERSITI TEKNOLOGI MALAYSIA

**FINAL EXAMINATION SEMESTER I, 2016 / 2017**

Faculty of

Computing

**SUBJECT CODE :**

**SUBJECT NAME :**

**SECTION :**

**TIME :**

**DATE/DAY :**

**VENUES :**

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**INSTRUCTIONS :**

Answer all questions from **Part A** and **B** in this question booklet. For **Part B**, read the questions carefully and show **ALL** your works in details.

This examination will contribute 35% towards the total marks of 100 points.

**Warning!**

**Students who are caught cheating during the examination will be reported to disciplinary board for action to suspend the student for one or two semesters.**

 **(Please Write Your Lecturer Name And Section In Your Answer Booklet)**

|  |  |
| --- | --- |
| **Name** |  |
| **I/C No.** |  |
| **Year / Course** |  |
| **Section** |  |
| **Lecturer Name** |  |

This question paper consists of \_\_\_\_ ( \_\_ ) printed pages excluding this page.

PART A: 15 OBJECTIVE QUESTIONS [Total mark 15 points]

Answer all the questions. Read each statement carefully. Please answer in Attachment A (page 10).

|  |  |
| --- | --- |
| 1. | One of the parallel adder types that is based on how it handles a carry value is a \_\_\_\_\_ carry adder. |
|  | A) | generation |
|  | B) | look back |
|  | C) | override |
|  | D) | ripple  |
|  |  |  |
| 2. | A decoder uses \_\_\_\_\_\_\_\_\_ gate if we want the output to be HIGH. |
|  | A) | AND |
|  | B) | OR |
|  | C) | NAND |
|  | D) | XNOR |
|  |  |  |
| 3. | Choose the FALSE statement about DEMUX. |
|  | A) | It is also known as a data selector. |
|  | B) | A DEMUX is basically the reverse of the multiplexing function. |
|  | C) | It takes digital information from one line and distributes it to a given number of output lines. |
|  | D) | A decoder can also be used as a DEMUX. |
|  |  |  |
| 4. | Select the CORRECT characteristic of the Figure 1 above. Figure 1 |
|  | A) | It is a negative edge-triggered flip-flop.  |
|  | B) | It is a negative edge-triggered latch. |
|  | C) | It is a positive edge-triggered flip-flop. |
|  | D) | It is a positive edge-triggered latch. |
|  |  |  |
| 5. | Which of the following statements is **FALSE** about the characteristics of sequential and combinational logic circuits?1. Which of the following statements is **FALSE** about characteristic of sequential and combinational logic circuit?
 |
|  | A) | Combinational logic circuit does not contain memory element compared to sequential logic circuit. |
|  | B) | In order to be fully functional, both combinational and sequential logic circuits require input clock triggered. |
|  | C) | Sequential logic circuit considers the previous state output before the current output circuit is produced. |
|  | D) | Sequential logic circuit can be constructed using basic logic gates and memory devices. |
|  |  |  |
| 6. | Which of the following statements is FALSE about a latch and a flip-flop? |
|  | A) | Latch and flip-flop can store binary bit 0 or 1.1. A latch requires a clock input before output latch can be changed
2. A flip-flop output will change according to the input flip-flop at edge triggered clock

A latch output will change according to the input latch at level triggered |
|  | B) | A latch requires a clock input before output latch can be changed. |
|  | C) | A flip-flop output will change according to the input flip-flop at the clock edge triggered. |
|  | D) | A latch output will change according to the input level of the latch. |
|  |  |  |
| 7. | 1. Which of the following statements is **FALSE** about an S-R latch?
 |
|  | A) | It has a SET state. |
|  | B) | It has a RESET state. |
|  | C) | It has a HOLD state. |
|  | D) | It has a TOGGLE state. |
|  |  |  |
| 8. | How many different states does a 3-bit asynchronous counter has? |
|  | A) | 3 C) 8 |
|  | B) | 6 D) 9 |
|  |  |  |
| 9. | What is the state value (in decimal) of Q2, Q1 and Q0 in the following circuit in order to produce a HIGH output at X? |
|  | A) | 5 C) 7 |
|  | B) | 6 D) 8 |
|  |  |  |
| 10. | What is the maximum state of a typical MOD 10 (decade) binary counter? |
|  | A) | 0000 C) 1111 |
|  | B) | 1010 D) 1001 |
|  |  |  |
| 11. | Referring to Figure 2, what is the signal frequencies of X and Y?Figure 2 |
|  | A) | X = 0.25 MHz, Y = 0.125 MHz. |
|  | B) | X = 4 MHz, Y = 2 MHz. |
|  | C) | X = 0.125 MHz, Y = 0.25 MHz. |
|  | D) | X = 2 MHz, Y = 4 MHz. |
|  |  |  |
| 12. | Which of the following statements is TRUE about synchronous counter? |
|  | A) | Synchronous counter can count up and count down simultaneously (with the same clock cycle). |
|  | B) | If synchronous counter is implemented with N flip-flops in its sequential circuit, the number of valid states of the counter is always 2N. |
|  | C) | Synchronous counter can be implemented using D flip-flops, as long as the clock source of the flip flops is taken from the common clock source. |
|  | D) | Synchronous counter can be implemented using any type of flip-flop, as long as the clock source of flip flops is taken from the output of the preceding flip-flops. |
|  |  |  |
| 13. | The following are Shift Registers, EXCEPT: |
|  | A) | SISO Serial In, Serial Out C) SILO Serial In, Last Out |
|  | B) | SIPO Serial In, Parallel Out D) PIPO Parallel In, Parallel Out |
|  |  |  |
| 14. | The following statements are true about Shift Register (SR) EXCEPT:  |
|  | A) | SR stores binary data C) SR consists of several latches |
|  | B) | SR performs data rotate D) SR is used for data transfer |
|  |  |  |
| 15. | A **MOD 10** Ring counter requires \_\_\_\_\_\_\_\_\_\_. |
|  | A) | ten flip-flops C) four flip-flops |
|  | B) | five flip-flops D) eight flip-flops |

PART B: 4 SUBJECTIVE QUESTIONS [Total mark 85 points]

Question 1 [15 Marks]

Answer the following questions about some functions of combinational logic.

(a) A logic symbol of a parallel adder for summing TWO binary numbers is illustrated in Figure 3. If A = 00112 and B = 01102 with the carry in, *C0* = 0, complete Table 1 by reproducing it in your answer booklet. Assume pin label 1 represents LSB. [4M]



Figure 3

Table 1

|  |  |  |  |
| --- | --- | --- | --- |
| *Pin Label (i)* | Input | Carry Out | Sum |
| *Ai* | *Bi* | *Ci* | *i* |

(b) Draw the logic circuit for a binary decoder to detect the binary code 10010 which produces an active-LOW output. Assume the inputs are represented as. [3M]

(c) Given an active HIGH 7-segment display in Figure 4 displaying a digital number from a decoder that based on the BCD value, fill in Table 2. Reproduce Table 2 in your answer booklet. [4M]



Figure 4

Table 2

|  |  |  |
| --- | --- | --- |
| BCD Input | Segment Output | Display |
| *A* | *B* | *C* | *D* | *a* | *b* | *c* | *d* | *e* | *f* | *g* |
|  |  |  |  |  |  |  |  |  |  |  | 4 |
|  |  |  |  |  |  |  |  |  |  |  | 7 |
| 1 | 0 | 0 | 1 |  |  |  |  |  |  |  | 9 |

(d) Figure 5 (in page 11) shows the waveforms of data-input  and data-select  applied to a multiplexer. Complete Figure 5 by drawing the waveform output of ***X*** in relation to the inputs. Label each segment of output ***X*** with the correct data input selection. [4M]

**Question 2 [15 Marks]**

(a) Figure 6 shows a basic circuit of a latch. Answer the following based on the circuit.



Figure 6

1. Complete the following truth table with initial values of  and are bit 1 and 0. [4M]

|  |  |  |
| --- | --- | --- |
| Input | Output | State |
| A | B |  |  |
| 0 | 0 |  |  |  |
| 0 | 1 |  |  |  |
| 1 | 0 |  |  |  |
| 1 | 1 |  |  |  |

(ii) What type of latch is represented by the circuit in Figure 6? [1M]

(b) Referring to Figure 7 in page 12, complete the output ***Q*** for a Gated -  latch. Label each state that occurs for each transition in the timing diagram. [3M]

(c) Referring to Figure 8, answer the following questions. Assume Q is initially low.



$$\overbar{Q}$$

$$Q$$

 Figure 8

(i) Draw output $\overbar{Q}$ in the timing diagram at page 12. [3M]

(ii) List the input priority of the flip-flop from the highest to the lowest. [2M]

(d) Draw the implementation of negative edge T flip-flop by using JK flip-flop. [2M]

**Question 3 [40 Marks]**



Figure 9: Asynchronous binary counter

1. Based on Figure 9, draw the State Diagram for the counter by using binary representation. [4M]
2. Redesign Figure 9, by considering new requirements as follows:
* 3-bit count up ripple counter with Modulus-5;
* using J-K Flip-Flop and
* with negative edge triggered clock. [6M]

 (c) Rolek Corp is designing its new 2-bit binary counter. The state diagram of the counter is given in Figure 10:



Figure 10: State Diagram for 2-bit Rolek binary synchronous counter

Using T flip-flops, design the sequential logic circuit of the latest Rolek binary counter as specified above, by answering all questions below.

(i) Complete the following Next State and Transition Table. [8M]

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | Present State | Next State | FF1 | FF0 |
| m | Q1 | Q0 | Q1 | Q0 | T1 | T0 |

(ii) Get the optimized SOP Boolean expressions using K-Map. [4M]

(iii) Draw the complete final circuit design. [3M]

(d) For the sequential circuit shown in Figure 11, answer the following questions:



Figure 11: Sequential Circuit

(i) Derive the next-state equations for each flip-flop and output Y. [3M]

(ii) Produce the next state table. [8M]

(iii) Draw the state diagram. [4M]

**Question 4 [15 Marks]**

(a) Initially at t0, a 5-bit SIPO shift register is cleared. Then, at **t1** the data word **1910** is serially entered. **LSB** is shifted in first.

(i) Draw the circuit for a 5-bit SIPO using D flip-flop. [3M]

(ii) What are the content of the SIPO shift register at **t3**? Show your works in a table form.

 [3M]

(iii) At what clock cycle can all the input data be read at the output and state the output

 [2M]

(b) Answer the following questions based on a Johnson counter.

(i) Draw the logic diagram for a MOD 8 Johnson counter. [3M]

(ii) Write the counting sequence in a table form. Initially the content of all flip-flops are binary ‘0’. [4M]

**All the best!!! Show ALL your works.**

**ATTACHMENT A**

|  |  |
| --- | --- |
| **Name** |  |
| **Matric No.**  |  |
| **Lecturer** | **Dr. Foad | Dr. Ismail | Dr. Raja Zahilah** **Mr. Muhalim | Ms Rashidah | Ms. Marina** |

|  |  |
| --- | --- |
| Objectives | **/15** |
| Question 1 | **/15** |
| Question 2 | **/15** |
| Question 3 | **/40** |
| Question 4 | **/15** |
| **Total** | **/100** |

# PART A (OBJECTIVE)

*Mark your answer clearly.*

*Example*: =A= =B= =C= =D=

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **1.** | =A= =B= =C= =D= |  |  |  |
| **2.** | =A= =B= =C= =D= |  |  |  |
| **3.** | =A= =B= =C= =D= |  |  |  |
| **4.** | =A= =B= =C= =D= |  |  |  |
| **5.** | =A= =B= =C= =D= |  |  |  |
| **6.** | =A= =B= =C= =D= |
| **7.** | =A= =B= =C= =D= |
| **8.** | =A= =B= =C= =D= |
| **9.** | =A= =B= =C= =D= |
| **10.** | =A= =B= =C= =D= |
| **11.** | =A= =B= =C= =D= |
| **12.** | =A= =B= =C= =D= |
| **13.** | =A= =B= =C= =D= |
| **14.** | =A= =B= =C= =D= |
| **15.** | =A= =B= =C= =D= |

**ATTACHMENT B**

Answer for Question 1 (d)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| *D0* |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| *D1* |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| *D2* |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| *D3* |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| *S0* |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| *S1* |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| ***X*** |  |  |  |  |  |  |  |  |

Figure 5

Answer for Question 2 (b)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|   |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| EN |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| State |   |  |  |  |  |  |  |  |  |

Figure 7

Answer Question 2 (c)(i)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| $$CLK$$ |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| $$\overbar{PRE}$$ |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| $$\overbar{CLR}$$ |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| $$J$$ |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| $$K$$ |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| $$\overbar{Q}$$ |  |  |  |  |  |  |  |