UTM
UNIVERSITI TEKNOLOGI MALAYSIA

FINAL EXAMINATION
SEMESTER I 2010/2011

SUBJECT CODE	:	**SCR1013**
SUBJECT NAME	:	**DIGITAL LOGIC**
YEAR/COURSE	:	**SCR / SCV / SCI / SCJ / SCD**
DURATION	:	**2 HOURS 30 MINUTES**
DATE	:	
VENUE	:	

INSTRUCTIONS TO CANDIDATES:

1. Please FILL in your particulars in the answer booklet.
2. The paper consists of two parts: PART A and PART B.
3. Part A has 20 questions. Answer ALL questions of PART A in the objective answer sheet on page 14
4. Part B has 3 questions. Question marked with  need to be answered on Part B Answer sheet on page 15 to 17. Answer ALL other questions of PART B in the given answer booklet.

Name	
Matric No.	
Year/Course	* 1 2 3 4 / SCR / SCV / SCI / SCJ
Section	* 01 02 03 04 05 06
Lecturer's Name	* EN. MOHD FO'AD / EN. ABD. BAHRIM / EN. ISMAIL FAUZI

This booklet consist of 17 pages including this page

PARTB: SUBJECTIVE QUESTIONS

Answer all questions on the answer book provided.

1. a) Two binary numbers A and B are given as, $A_2\ A_1\ A_0 = 101$ and $B_2\ B_1\ B_0 = 110$.

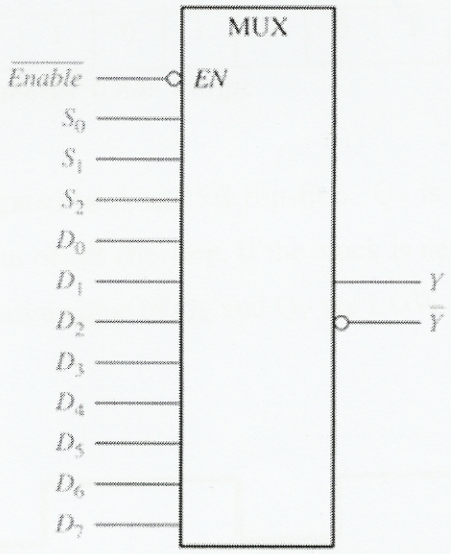
   a) Draw the block diagram of parallel adder to solve the equation X = A + B. [4M]

   b) Label the diagram with appropriate value of inputs and output. Indicate the MSB and LSB. [3M]

   c) What is the value of X in binary? [1M]

   Note: MSB = Most Significant Bit, LSB = Least Significant Bit.

b) 74LS151 IC is a 1 of 8 Multiplexer and its symbol is shown in the figure below.



i) What is the purpose of a multiplexer? [1M]

ii) Pins of the IC are categorised into 4 categories such as Enable Pin, Data Selector Pin, Input Data Pin and Output Data Pin.
Complete the table below by write-in all of 13 pin labels from figure above into its correct category. [3M]

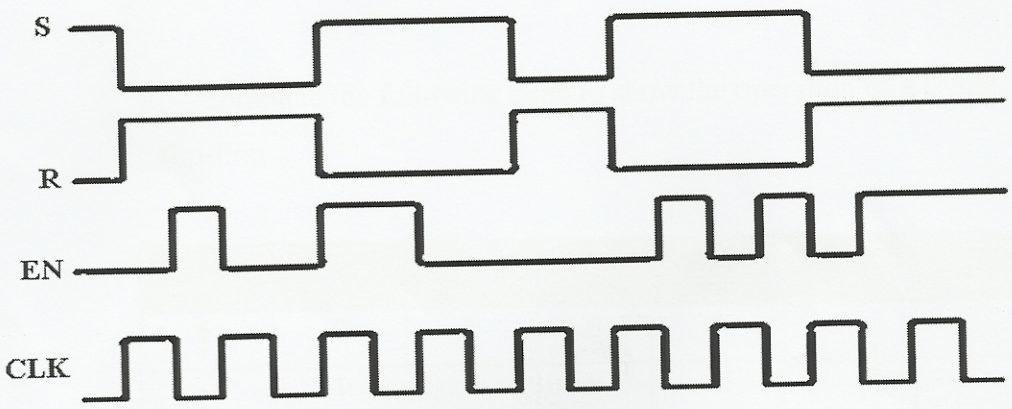
Pin Category	Label
Enable Pin	$\overline{EN}$
Output Data Pin	
Data Selector Pin	
Input Data Pin	

iii) Complete the table below. [5M]

$\overline{EN}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	S_2	S_1	S_0	Y	$\overline{Y}$
0	0	1	0	1	1	1	1	1	0	1	1		
0	1	0	1	0	1	1	0	0	1	1	0		
0	0	1	1	1	0	1	0	1	1	1	1		
1	0	1	1	0	0	1	1	0	0	1	0		
0	0	1	1	0	1	1	0	1	1	0	1		

Note: Hi-Z = neither 0 nor 1 logic

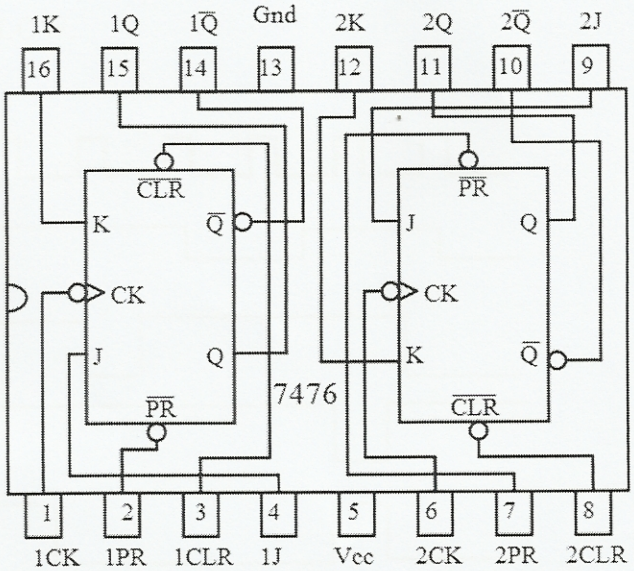
2. a) You are given SR gated latch and SR flip-flop. Q_X is the output of SR gated latch and Q_Y is the output of SR flip-flop. If the clock is negative edge triggered, draw Q_X and Q_Y. The initial value of Q_X and Q_Y are LOW. [6M]



Qx

Qy

b) You are given IC 74LS76 as follows:



i) List the Asynchronous and Synchronous inputs. Arrange the priority execution based on the listed input. [3M]

ii) Using single JK flip-flop, draw the circuit for the following. [6M]

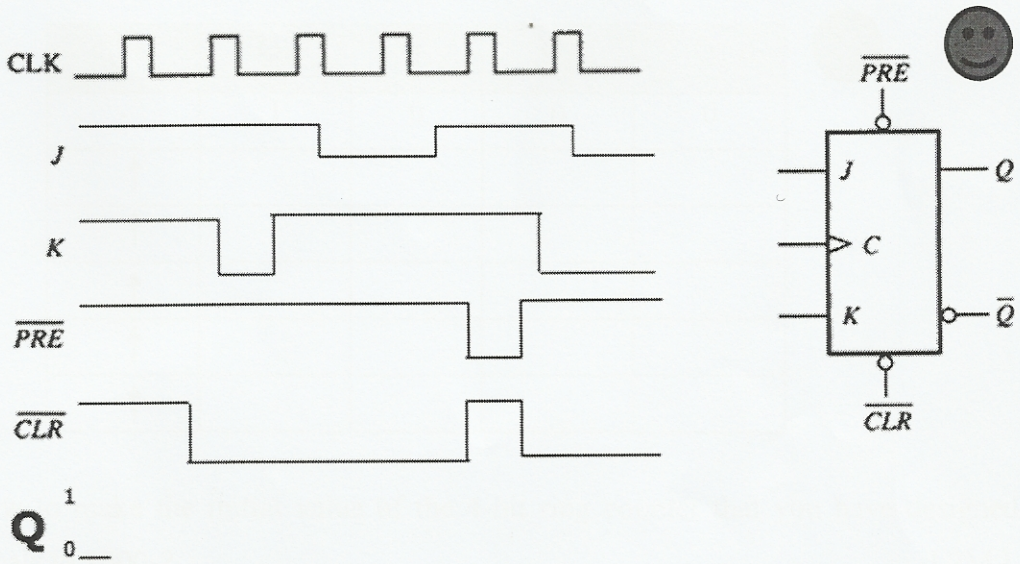
i. D flip-flop

ii. T flip-flop

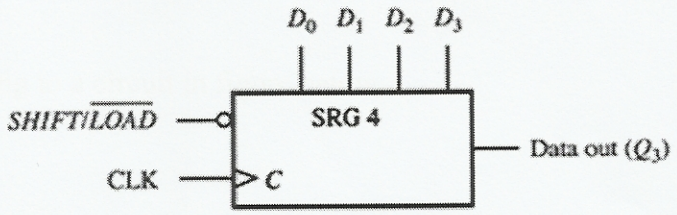
iii. Complete the following table to show the operation of a D and T flip-flop

CLK	$\overline{PRE}$	$\overline{CLR}$	D	T	Q_D	Q_T
↑	0	1	0	0		
↑	1	1	0	1		
↑	1	0	1	0		
↑	1	1	1	1		

iii) Determine the **Q waveform** relative to the clock if the signals shown in the following figure are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW. [5M]



3. Questions referring to a shift register below.



a) What is the name of the shift register? [1M]

b) If a nibble data 1101 is to be loaded and shifted by the circuit, complete the following table. Initial value of $Q_3 = 0$. [4M]

SHIFT / LOAD	CLK	D_0	D_1	D_2	D_3	Q_3
0	-					
1	↑					
1	↑					
1	↑					

4. a) Design a 4-bit ring counter using JK flip-flop. [4M]

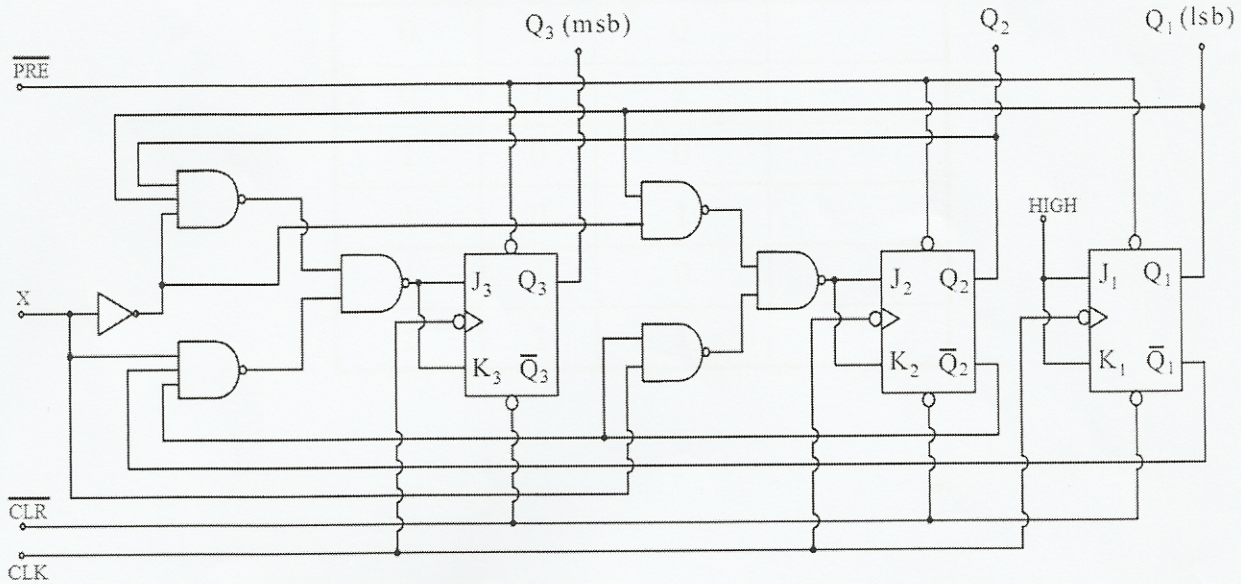
b) Show the output of the 4-bit ring counter that you have designed in the following table. [5M]

CLK	Q_3	Q_2	Q_1	Q_0
-	1	0	0	0
↑				
↑				
↑				
↑				
↑				

c) How to make the initial value of the 4-bit ring counter that you have designed equals to 1000_2? [2M]

d) Draw the state diagram of the designed ring counter and determine its MOD. [4M]

5. Questions referring to a circuit in figure below.



a) How to make the initial value of the output $Q_3Q_2Q_1$ equals to 0? [1M]

b) If the propagation delay of a NAND gate is 20ns, an inverter 10ns and JK flip-flop 40ns, determine the maximum frequency of the clock to guarantee the proper counting sequence. [3M]

c) Draw the state diagram

i) for **three states only** starting from state 000_2 when X = 0. [6M]

ii) for **three states only** starting from state 101_2 when X = 1. [6M]

6 a) Comparing a synchronous counter to an asynchronous counter

i) What is the difference between a synchronous counter and an asynchronous counter? [1M]

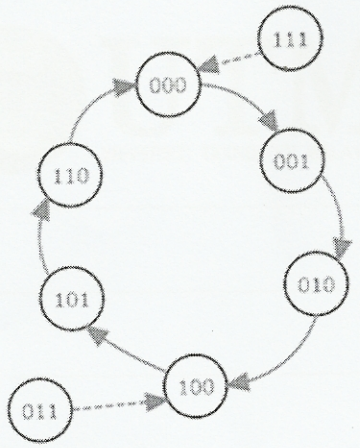
ii) Give one advantage of a synchronous counter. [1M]

b) i) Fill in the Next State column in the table below [2M]

ii) Use the completed table, produce an Excitation table for JK flip-flop. [3M]

FF State		Present State	Next State
J	K	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

c) i) Design a synchrous counter using JK flip-flop that will have a state diagram as in figure below. *Show all your design steps.* [10M]



ii) Add a switch to your designed circuit from (5.c.i) and label it as RESET. Show the connection of the switch so that the counter will move to state 110_2 when RESET switch is pressed. [3M]