CONFIDENTIAL

FINAL EXAMINATION SEMESTER I 2013/2014

SUBJECT CODE : SCSR1013

SUBJECT TITLE : DIGITAL LOGIC

YEAR/COURSE :

DURATION :

DATE :

VENUE :

STRUCTURED QUESTIONS (100 MARKS)

(INSTRUCTION: Please answer ALL questions in the space provided.)

QUESTION 1 (15 Marks)

(a) Determine the sum generated by the 3-bit parallel adder in Figure 1 by completing the values in Table 1 for input A and B equal to 101_2 and 110_2 are being added. [4 marks]

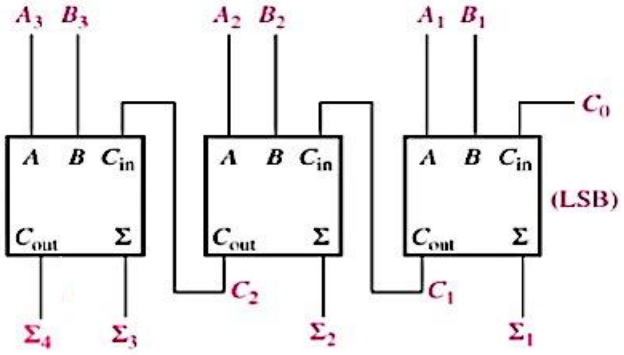


Figure 1

Table 1

Label	A_1	A_2	A_3	B_1	B_2	B_3	C_0	C_1	C_2	$\sum_1$	$\sum_2$	$\sum_3$	$\sum_4$
Value (binary)													

(b) Identify the comparator inputs and outputs when the binary numbers of A and B are applied as shown in Figure 2. Complete Table 2. [5 marks]

Table 2

Symbol	Value (Binary)
A	
B	
x	
y	
z	

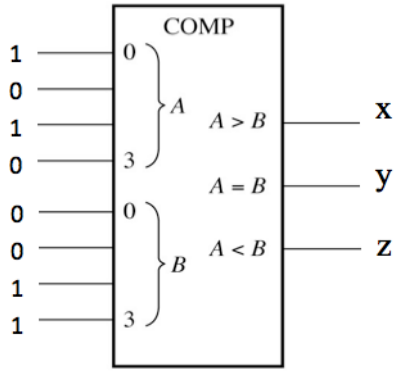


Figure 2

(c) Based on Figure 3, the data-input, D_i (i = 0, 1, 2, 3) and data-select, S_j (j = 0, 1) waveforms are applied to the multiplexer.

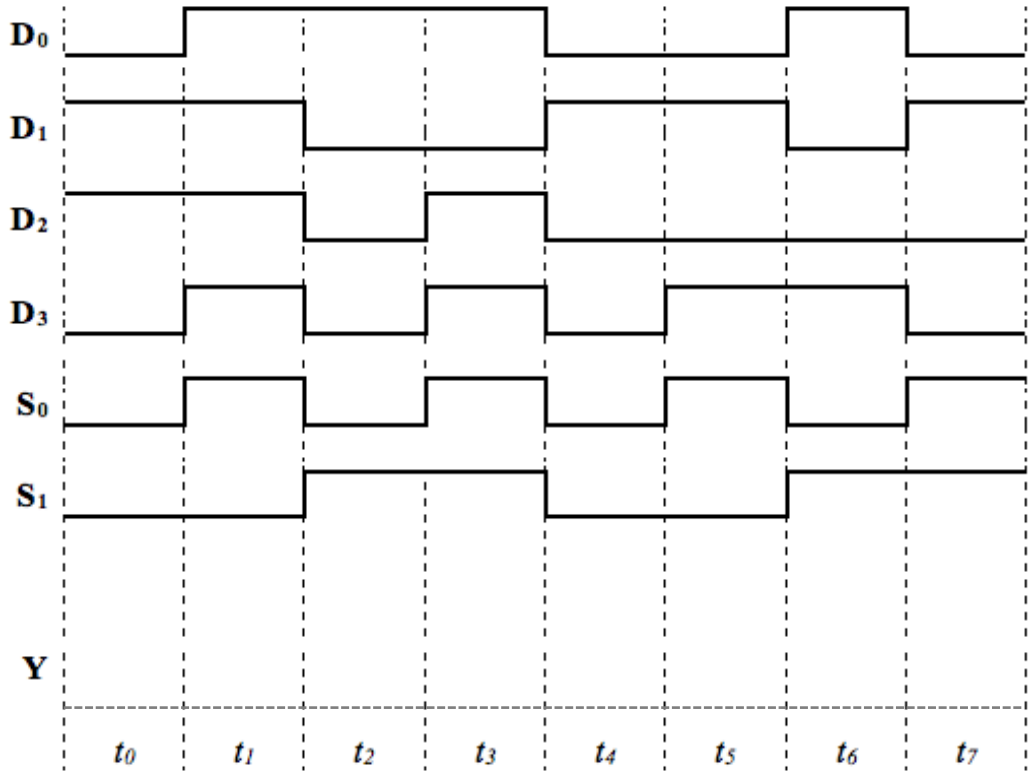


Figure 3

i. Identify the selection line (D_i) at t_0 until t_7 by filling in Table 3. [2 marks]

Table 3

Time	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7
Selection line, D_i								

ii. Draw the output waveform Y in Figure 3. [4 marks]

QUESTION 2 (20 Marks)

(a) Referring to Figure 4, answer the questions below.

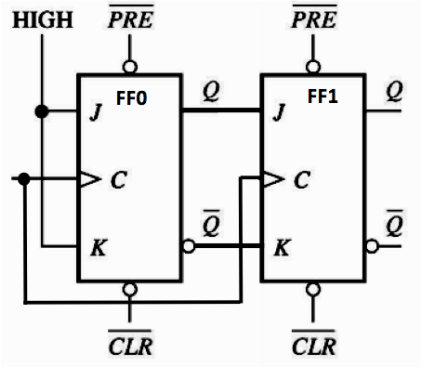


Figure 4

i. What are the possible values of the signals to activate the asynchronous operation? [2 marks]

ii. JK flip-flop is a universal flip-flop, which can be configured to work as different flip-flops. What type of flip-flop do FF1 and FF0 represent? Write your answers and provide justification in Table 4. [5 marks]

Table 4

Flip-flop	Type	Justification
FF1		
FF0		

iii. Fill in Table 5 with the appropriate inputs according to the flip-flop priority operation. [2 marks]

Table 5

Priority	Input(s)
Highest	
Lowest	

iv. Complete the values in Table 6 after 3 clock cycles for the given conditions. The initial value of Q_{FF0} is 0. Justify your answer. [5 marks]

Table 6

FF0		FF1		CLOCK	Q_{FF0}	Q_{FF1}
$\overline{PRE}$	$\overline{CLR}$	$\overline{PRE}$	$\overline{CLR}$			
1	0	1	1			

Justification:

(b) Draw the output, Q of the different latches and flip-flop in Figure 5. Assume positive-edge clock. [6 marks]

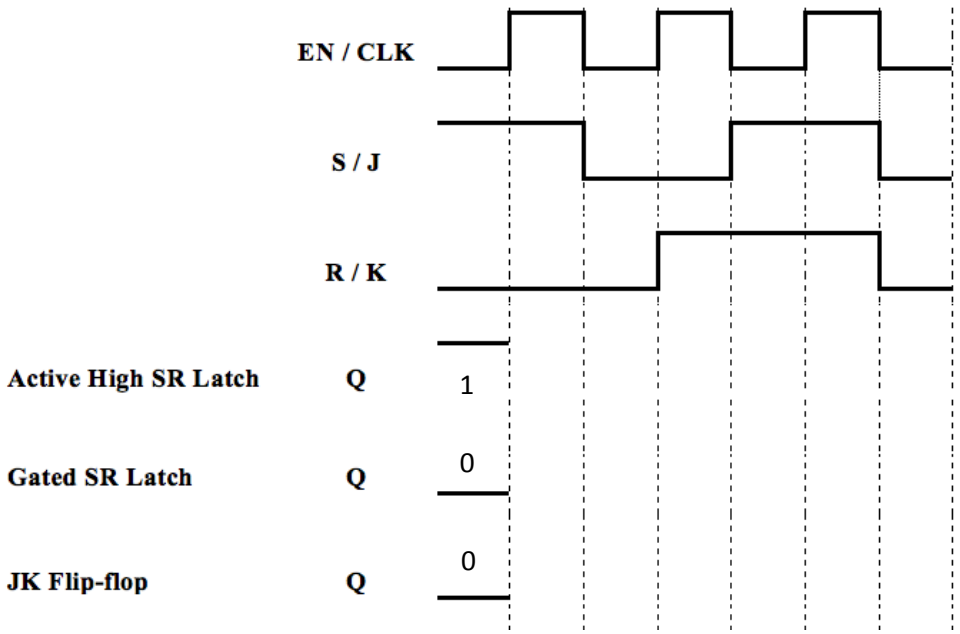


Figure 5

QUESTION 3 (20 Marks)

Answer the following questions based on Figure 6.

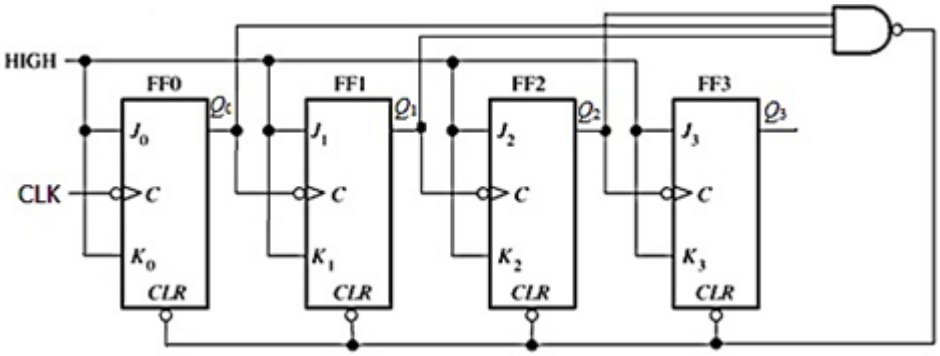


Figure 6

(a) Draw the complete timing diagram for ten clock pulses in Figure 7. Initial value for $Q_3 = Q_2 = Q_1 = Q_0 = 0$. [4 marks]

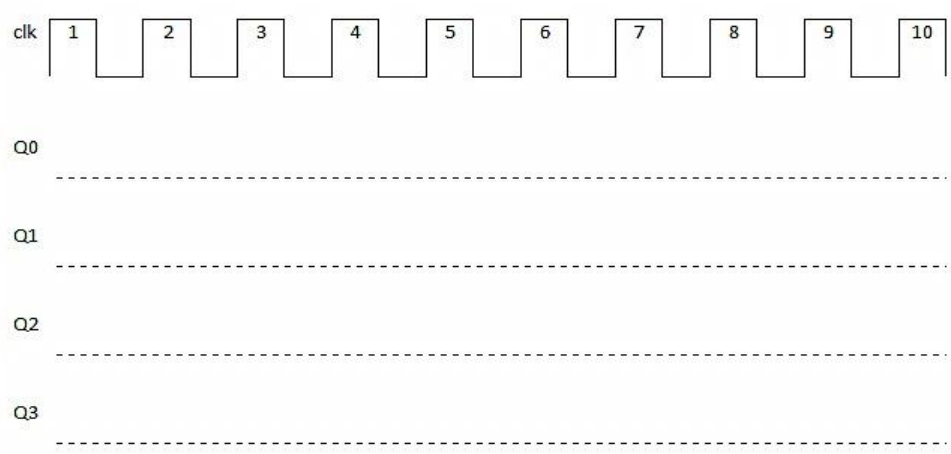


Figure 7

(b) Determine whether the counter is asynchronous or synchronous. Justify. [3 marks]

Type of counter:

Justification:

(c) Is the counter count-up or count-down? [1 mark]

(d) What is the minimum and maximum number that can be counted by the counter based on **ONLY** four flip-flops? [2 marks]

(e) What is the purpose of the NAND gate in Figure 6? [2 marks]

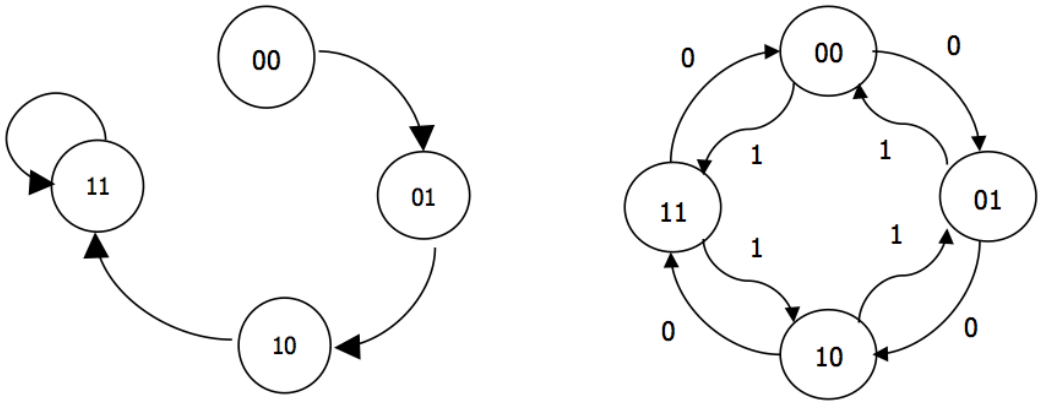
(f) What is the actual modulus (MOD) for the counter? [2 marks]

(g) From your answer in 3(f), draw the state diagram for the counter. [4 marks]

(h) Based on your answers, comment on the efficiency of the counter design. [2 marks]

QUESTION 4 (30 Marks)

(a) Give **TWO** characteristics of each counter in Table 7 shown by the state diagram in Figure 8. [2 marks]



(a) (b)

Figure 8

Table 7

Figure 8	Characteristic 1	Characteristic 2
(a)		
(b)		

(b) Complete the next state table for D and T flip-flops in Table 8 and Table 9. [2 marks]

Table 8

Present State		Next State		D flip-flop transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	D_1	D_0
1	0	0	1		
0	1			1	0

Table 9

Present State		Next State		T flip-flop transition	
Q_1	Q_0	Q_{1+}	Q_{0+}	T_1	T_0
1	1	0	1		
		0	0	0	1

(c) A two bit sequential circuit counter has an input *X*. The characteristic of the counter operates according to the transition state value in Table 10. Answer the following questions based on Table 10.

Table 10

Input	**Present State**		**Next State**		**JK FF Transition**			
X	Q_1	Q_0	Q_{1+}	Q_{0+}	J_1	K_1	J_0	K_0
0	0	0	0	0				
0	0	1	0	1				
0	1	0	1	0				
0	1	1	1	1				
1	0	0	0	1				
1	0	1	1	0				
1	1	0	1	1				
1	1	1	0	0				

i. Draw a complete state diagram. [3 marks]

ii. Complete all the values in Table 10 if JK flip-flops are used in the synchronous counter design. [8 marks]

iii. Using K-map, find the optimized Boolean equations for all the input JK flip-flops. [4 marks]

iv. Draw the final circuit of the counter design. [3 marks]

(d) Analyze the cascaded counter circuit in Figure 9. If the input frequency of the counter is 1 KHz, calculate the output frequency of MOD 2 and MOD 10 (i.e. f_0 and f_2). [2 marks]

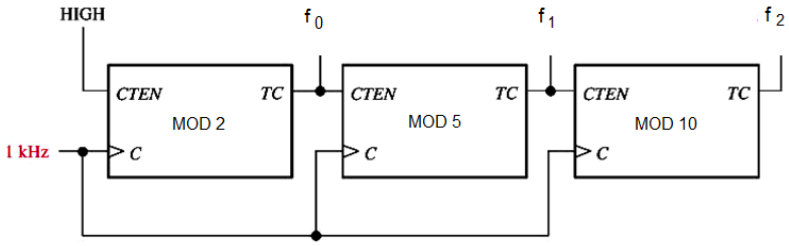


Figure 9

(e) Analyze the synchronous counter circuit in Figure 10.

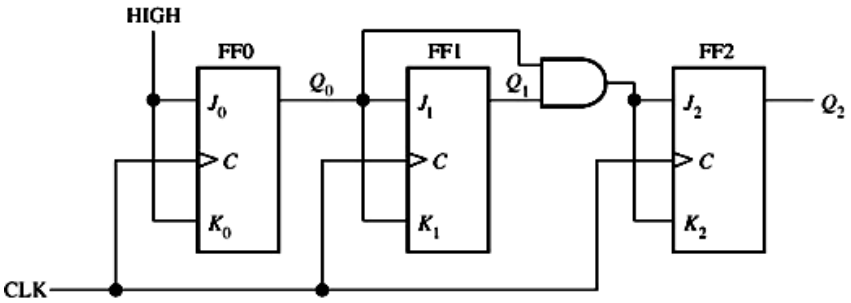


Figure 10

i. Write Boolean equations for all the inputs of JK flip-flops. [1.5 marks]

ii. Based on the Boolean equations in (i), write the Boolean equations for the next state value for Q_0, Q_1 and Q_2. [3 marks]

iii. Calculate the next state for the current state value given in Table 11. Use your answers in question (ii). [1.5 marks]

Table 11

Current State	**Next State**
$Q_2\ Q_1\ Q_0 = 100_2$	

QUESTION 5 (15 Marks)

(a) Figure 11 shows a shift register using type JK storage element. Answer the following questions.

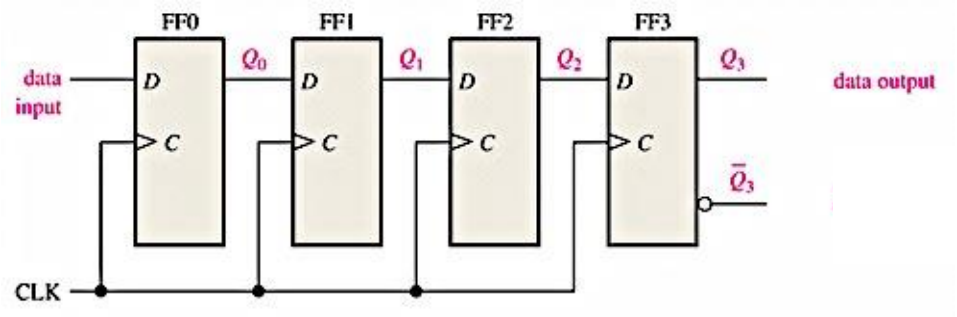


Figure 11

i. What is the type of the shift register? [1 mark]

ii. Draw the flip-flops output in Figure 12 for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s). [4 marks]

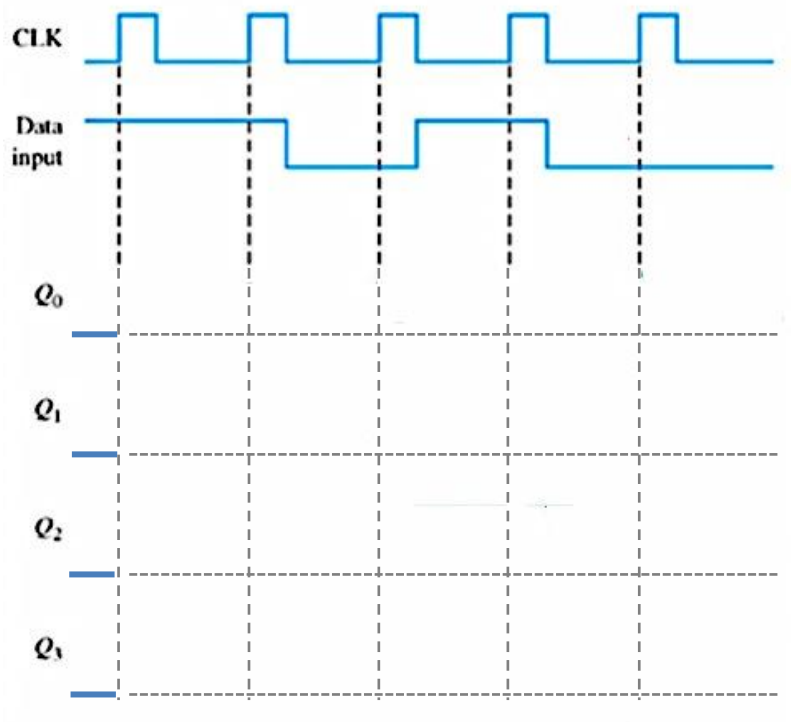


Figure 12

(b) Figure 13 shows a shift register counter. Answer the following questions.

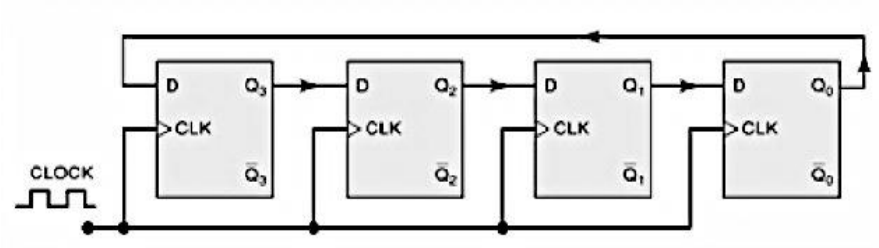


Figure 13

i. Complete the truth table in Table 12 for the operation of the shift register counter. Determine how many states the counter has? [5 marks]

Table 12

Clock	**Q_3**	**Q_2**	**Q_1**	**Q_0**
↑	1	0	1	1
↑				
↑				
↑				
↑				

Number of state: ……..…..

ii. Modify the circuit in Figure 13, so that it becomes a 3-bit *Johnson counter*. Draw the complete circuit. [3 marks]

iii. What is the MOD of the new modified counter in (ii)? [2 marks]