SULIT

UTM UNIVERSITI TEKNOLOGI MALAYSIA
Fakulti Sains Komputer & Sistem Maklumat
UNIVERSITI PENYELIDIKAN

FINAL EXAMINATION SEMESTER I 2012/2013

SUBJECT CODE : SCR1013 / SCSR1013

SUBJECT TITLE : DIGITAL LOGIC

COURSE : SCSR / SCSV / SCSI / SCSJ / SCSD

DURATION : 3 HOURS

DATE :

PLACE :

INSTRUCTIONS TO CANDIDATES:

1) Please FILL in your particulars in the space provided below.
2) Answer ALL questions in space provided in the question paper.
3) This questions paper consists of Part A and Part B. Part A will contribute 35 marks while Part B contributes 65 marks.

Name	
Matric No.	
Course	* SCSR / SCSV / SCSI / SCSJ / SCSD
Section	* 01 02 03 04 05 06 07 08
Lecturer's Name	

THIS PAPER CONTAINS 23 PAGES NOT INCLUDING THIS COVER PAGE.

PART A: OBJECTIVE QUESTIONS [35 marks]

Instruction: Answer ALL questions and mark your answer in answer sheet on page 11 and 12. Each question from 1 to 20 contributes 1 mark while question 21 to 30 contributes 1.5 marks.

1. Product of Sum (POS) expressions can be implemented using _____ circuit.
   A) AND-OR logic
   B) AND-OR-Invert logic
   C) AND-XOR logic
   D) AND-Invert logic

2. Choose the **TRUE** statement.
   A) $\overline{\bar{A} + B} = AB$
   B) $\overline{A\bar{B}} = AB$
   C) $\overline{\bar{A}\bar{B}} = AB$
   D) $\overline{\bar{A} + \bar{B}} = AB$

3. Circuit in Figure 1 is equivalent to which gate?

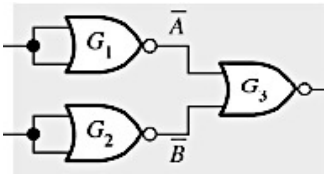


Figure 1

   A) OR
   B) XOR
   C) AND
   D) NOT

4. If $X = \bar{A}B + CD$, X is equivalent to:
   A) $\overline{\overline{A\bar{B}}.\overline{C\bar{D}}}$
   B) $\overline{\bar{A}\bar{B}.\overline{C\bar{D}}}$
   C) $\overline{\overline{A\bar{B}} + \overline{C\bar{D}}}$
   D) $\overline{\bar{A}\bar{B} + CD}$

5. The addition of an inverter to an SR flip flop creates _____.

   A) JK flip flop

   B) D flip flop

   C) T flip flop

   D) Master slave flip flop

6. A flip flop that can be built from JK flip flop by connecting J and K to the same node is _____.

   A) SR flip flop

   B) JK flip flop

   C) T flip flop

   D) D flip flop

7. The difference between SR flip flop and JK flip flop is SR has _____while JK doesn't.

   A) Hold state

   B) Toggle state

   C) Invalid state

   D) Clock

8. T flip flop has only 2 states, which are _____.

   A) Set and Reset

   B) Hold and Toggle

   C) Set and Toggle

   D) Reset and Toggle

9. Which of the following function can be used to detect whether a car exceed the speed limit on a highway?

   A) Parity generator

   B) Comparator

   C) Encoder

   D) Multiplexer

10. What is the output of the priority decoder in Figure 2 if the input is HIGH at 8, 6, 3 and 1 and all other input are LOW?

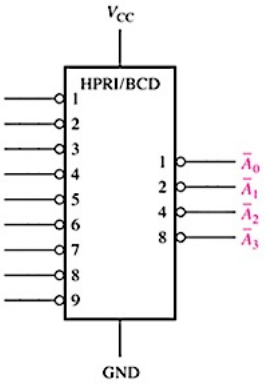


Figure 2

A) 1000_2

B) 0110_2

C) 1111_2 to indicate an error

D) 0000_2 to indicate an error

Questions 11 and 12 referring to circuit in Figure 3.

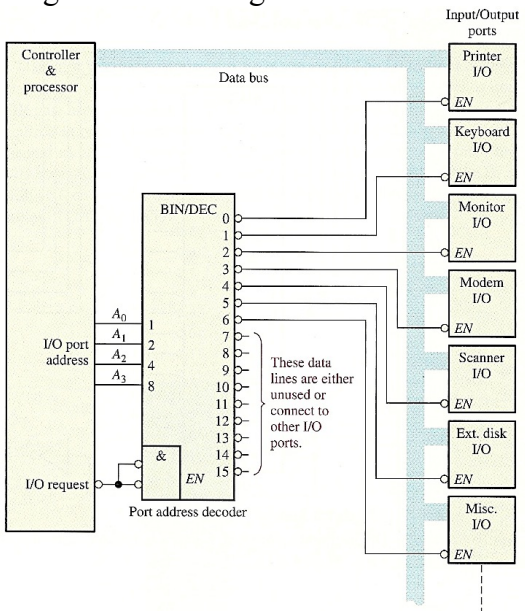


Figure 3

11. What is the function of IC labeled as BIN/DEC in Figure 3?

A) Encoder

B) DeMultiplexer

C) Code converter

D) Decoder

12. What is the value of $A_3A_2A_1A_0$ to select the Scanner if I/O request equals to 0 in Figure 3?

A) 0100_2

B) 0110_2

C) 1001_2

D) 0011_2

13. The counter is used for the following examples **EXCEPT**:

A) To count the number of times that some event take place.

B) To convert a binary to decimal value.

C) To generate a timing signal.

D) To generate clocks with different frequencies.

14. Figure 4 shows timing diagram for an asynchronous counter using J-K flip flop. Choose the **FALSE** statement describing the counter with Q_0 initially LOW.

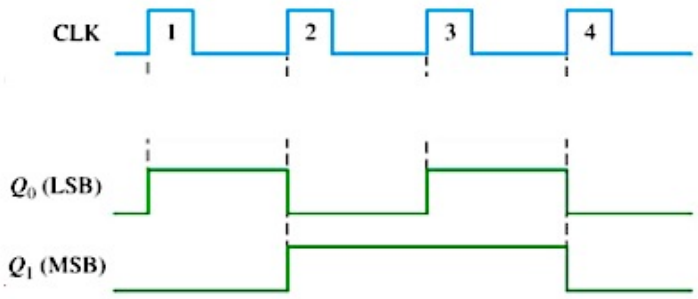


Figure 4

A) The counting sequence is unidirection up.

B) The type of J-K flip flops used is positive edge.

C) Q_1 is complement when Q_0 = HIGH after next clock edge.

D) It is a MOD-2 counter.

15. Figure 5 illustrates state diagram for a synchronous counter using T flip flop. When $T_1 = 0$ and $T_0 = 1$, which state transition will occur?

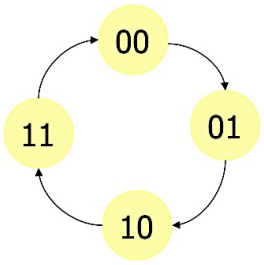


Figure 5

A) 00 → 01 and 01 → 10

B) 10 → 11 and 11 → 00

C) 01 → 10 and 11 → 00

D) 00 → 01 and 10 → 11

16. Two cascaded decade counters is shown in Figure 6. Choose the **FALSE** statement about the counter.

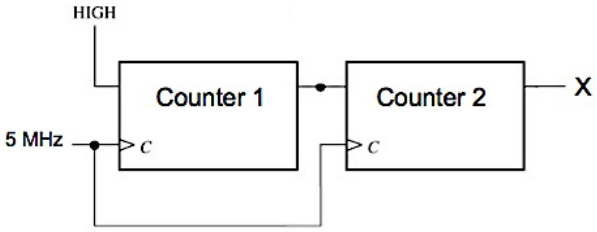


Figure 6

A) The counter performs as frequency divider.

B) Total flip flop used is 4.

C) It also knows as modulus-100 cascaded counter.

D) To obtain X = 0.005 MHz, the circuit needs one more similar counter to be cascaded.

17. Which of the following is not categorized as shift register?

A) Serial In / Serial Out

B) Serial In / Parallel Out

C) Parallel In / Parallel Out

D) Serial In Shift Left/ Serial Out Shift Right

18. The group of bits 10110101_2 is serially shifted (LSB first) into an eight bit parallel output shift register with an initial state of 11100100_2. After two clock pulses the register contains _____.

A) 01011110_2

B) 10110101_2

C) 01111001_2

D) 00101101_2

19. A MOD-10 Johnson counter requires _____.

A) 10 flip-flops

B) 4 flip-flops

C) 5 flip-flops

D) 12 flip-flops

20. To serially shift a byte of data into a shift register, there must be _____.

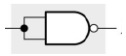
A) 1 clock pulse.

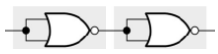
B) 1 load pulse.

C) 8 clock pulses.

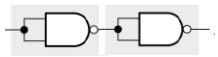
D) 1 clock pulse for each bit 1 in the data.

21. Choose the correct implementation of an inverter.

i. 

ii. 

iii. 

iv. 

A) i and ii.

B) i, ii and iii.

C) i and iii.

D) iv only.

22. Choose the **FALSE** statement about dual symbols.

i. The dual symbol for NAND gate is Negative OR.

ii. The dual symbol for NOR gate is Negative AND.

iii. Dual symbol is needed to simplify the "reading" of the schematic.

iv. None of the above.

A) i and ii.

B) i, ii and iii.

C) iii only.

D) iv only.

23. Choose the **TRUE** statement of Gated SR latch.

i. It's output change at the edge of the clock

ii. ENABLE pin has a higher priority than pin S and R.

iii. It has CLK to control its operation.

iv. If EN = 1, the output will change immediately according to input S and R.

A) ii and iv.

B) i, ii and iii.

C) iii only.

D) iv only.

24. Choose the **TRUE** characteristics for asynchronous input of a flip flop.

i. Clock has the highest priority than asynchronous input $\overline{PRE}$ and $\overline{CLR}$.

ii. If $\overline{CLR}$ = 0, reset the output to '0'.

iii. If $\overline{PRE}$ = LOW, reset the output to LOW.

iv. Asynchronous input $\overline{PRE}$ and $\overline{CLR}$have the highest priority than Clock.

A) i and ii.

B) ii and iv.

C) i and iii.

D) iii and iv.

25. Circuit in Figure 7 is using a Full Adder (FA). Choose the **TRUE** statement about the circuit.

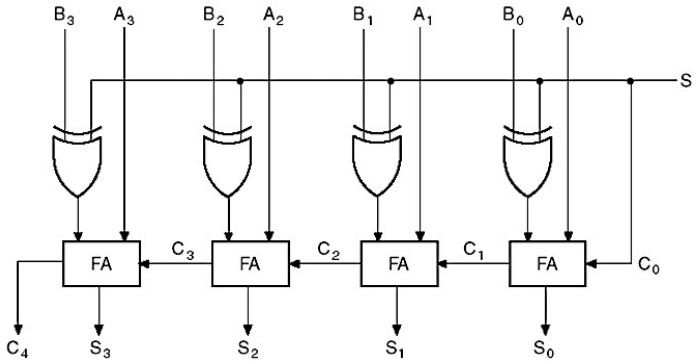


Figure 7

i. It can add two 4 bits numbers.

ii. If S HIGH, B will be subtracted from A.

iii. The arithmetic uses a 1's complement.

iv. XOR always function as an inverter in the circuit.

A) i and ii.

B) i,ii and iii.

C) iii and iv.

D) i,ii, iii and iv.

26. Which function can be used to route a signal from one place to the other?

i. Multiplexer.

ii. DeMultiplexer.

iii. Decoder.

iv. Code converter.

A) i and ii.

B) i, ii and iii.

C) iii and iv.

D) All of the above.

27. Figure 8 illustrates a decoder that connected to an asynchronous counter using D flip flop. Choose the **TRUE** statements about the counter.

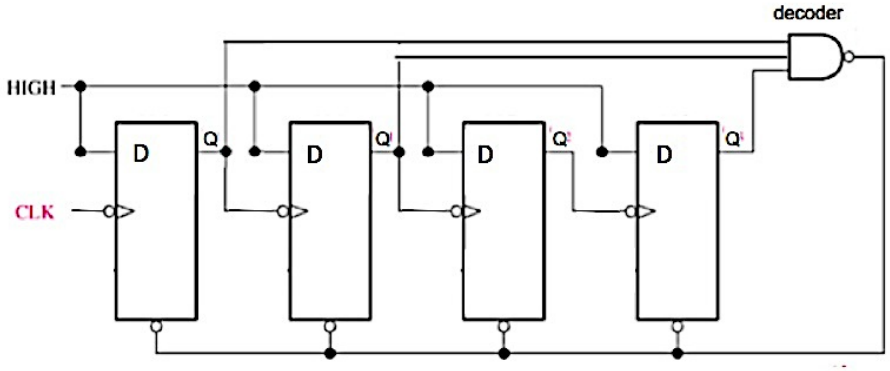


Figure 8

i. It is a count down counter.
ii. The decoder will reset the counter when its input is 1011_2.
iii. The $\overline{CLR}$ input will reset when output of the decoder is 1.
iv. The counter will have eleven states.

A) i, iii and iv.
B) ii and iv.
C) i and iii.
D) i, ii, iii, and iv.

28. Choose the **TRUE** statements about shift register.

i. Two functions of a shift register are data storage and data movement.
ii. A shift register can have both parallel and serial outputs.
iii. All shift registers are defined by specified sequences.
iv. In a serial shift register, several data bits are entered at the same time.

A) i and ii.
B) ii and iii.
C) i, iii and iv.
D) i and iv.

29. Figure 9 illustrates a 2-bits up-down synchronous counter using D flip flop with an input X. When X = 0, the counter will count up. Choose the **TRUE** statements about the counter.

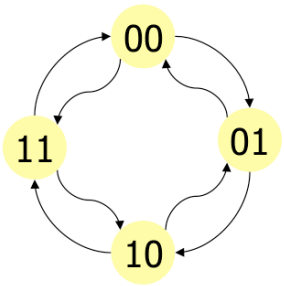


Figure 9

i. Assume the present state is 00, the state after the input sequence of X = {1, 1, 0} is 01.
ii. If X = 1, the next state for 10 is 11.
iii. Assume the present state is 01, the state after the input sequence of X = {0, 1, 0} is 10.
iv. If X = 0, the next state for 11 is 10.

A) i and iii only.
B) ii and iv only.
C) iii only.
D) i, ii, and iv only.

30. Choose the **FALSE** statements about shift register.

i. The Johnson counter is a special type of shift register.
ii. The mod of an 8-bits Ring counter is 8.
iii. A Ring counter uses 1 flip flop for each state in its sequence.
iv. A shift register can be used as a time delay device.

A) i and ii.
B) ii and iii.
C) i, iii and iv.
D) None of the above.

ANSWER SHEET FOR SECTION A (1)

NAME :			
MATRIC NO.:		**SECTION :**	

Example: =A=  =C= =D=

1)	=A=	=B=	=C=	=D=
2)	=A=	=B=	=C=	=D=
3)	=A=	=B=	=C=	=D=
4)	=A=	=B=	=C=	=D=
5)	=A=	=B=	=C=	=D=
6)	=A=	=B=	=C=	=D=
7)	=A=	=B=	=C=	=D=
8)	=A=	=B=	=C=	=D=
9)	=A=	=B=	=C=	=D=
10)	=A=	=B=	=C=	=D=
11)	=A=	=B=	=C=	=D=
12)	=A=	=B=	=C=	=D=
13)	=A=	=B=	=C=	=D=
14)	=A=	=B=	=C=	=D=
15)	=A=	=B=	=C=	=D=
16)	=A=	=B=	=C=	=D=
17)	=A=	=B=	=C=	=D=
18)	=A=	=B=	=C=	=D=
19)	=A=	=B=	=C=	=D=
20)	=A=	=B=	=C=	=D=

ANSWER SHEET FOR SECTION A (2)

NAME :			
MATRIC NO.:		**SECTION :**	

Example: =A=  =C= =D=

21)	=A=	=B=	=C=	=D=
22)	=A=	=B=	=C=	=D=
23)	=A=	=B=	=C=	=D=
24)	=A=	=B=	=C=	=D=
25)	=A=	=B=	=C=	=D=
26)	=A=	=B=	=C=	=D=
27)	=A=	=B=	=C=	=D=
28)	=A=	=B=	=C=	=D=
29)	=A=	=B=	=C=	=D=
30)	=A=	=B=	=C=	=D=

PART B: STRUCTURED QUESTIONS [65 marks]

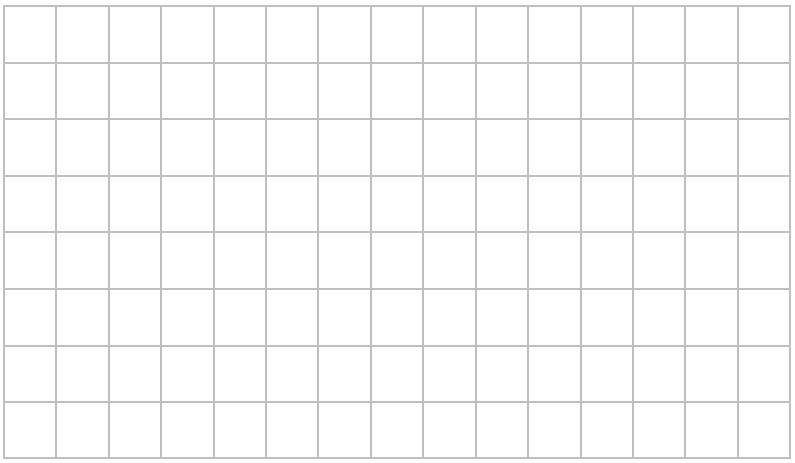
Instruction: Answer ALL questions in this question booklet.

QUESTION 1 (15 marks)

(a) A circuit is required to detect whether the number of 0's at the input is more than the number of 1. There are 4 inputs to the circuit and it will produce a logic 1 if the number of 0's at the input is more than the number of 1's (e.g: 0010_2 – three 0's and one 1). The circuit will never have an input where the number of 1's is equal to the number of 0's. Design the circuit by doing the following steps.

i) Produce a truth table. [5 marks]

ii) Draw the K-Map and get the simplified Boolean expression. [5 marks]



iii) Draw the circuit using basic gates. [2 marks]

iv) Convert the circuit in 1(a)iii) to NAND gates only. [3 marks]

QUESTION 2 (10 marks)

(a) The following questions refer to Figure 10.

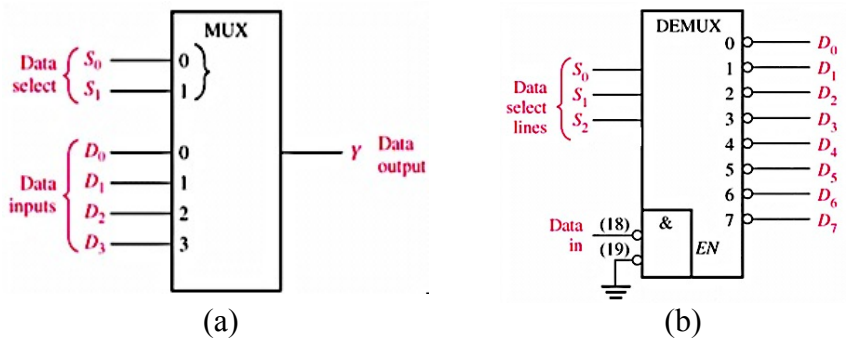


Figure 10

i) In Figure 10(a), assume $D_3D_2D_1D_0$ always equals to 1101_2. Determine Y if S_1S_0 change from 11_2 → 10_2 → 01_2→ 00_2 by completing the following table. [2 marks]

$S_1S_0 = 11_2$	$S_1S_0 = 10_2$	$S_1S_0 = 01_2$	$S_1S_0 = 00_2$
Y =	Y =	Y =	Y =

ii) In Figure 10(a), if S_1S_0 always equals to 01_2, what is the output of Y if binary stream for $D_0 = 1011_2$, $D_1 = 0000_2$, $D_2 = 1100_2$ and $D_3 = 1010_2$. [1 mark]

iii) Draw the connection from Figure 10(a) to Figure 10(b) so that data from MUX can be sent to DeMUX. Show your connection on Figure 10. [1 mark]

iv) If S_1S_0 of MUX = 01_2 and $S_2S_1S_0$ of DeMUX are 101_2, determine which data are sent to which output. [1 mark]

(b) i) Design and draw a 3-bit unsigned parallel adder using full adder. [3 marks]

ii) On the circuit shows the value at the input and output while adding two numbers which the value are A = 101_2 and B = 110_2. [2 marks]

QUESTION 3 (10 marks)

The following questions refer to Figure 11.

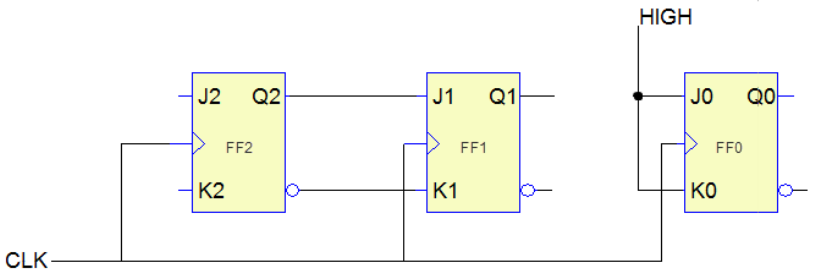


Figure 11

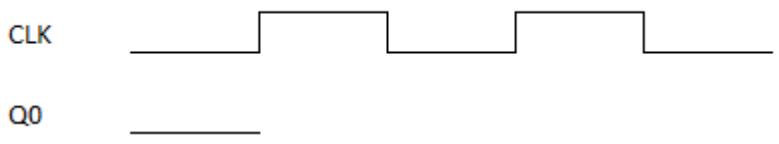
(a) JK flip-flop is a universal flip-flop which can be configured as the other flip-flop. What type of flip-flop for FF1 and FF0 produced by the connection? Justify your answer.

[2 marks]

(b) If $J_2 = 1$, $K_2 = 1$ and initial value for $Q_2Q_1Q_0 = 110$, what will be the value of $Q_2Q_1Q_0$ after 2 clock cycles. Justify your answer.

[3 marks]

(c) Complete the timing diagram for Q_0. [1 mark]



(d) A modification of clock as in Figure 12 is connected to all clock input of all flip-flops.

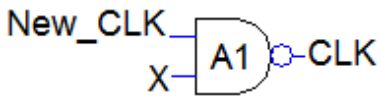
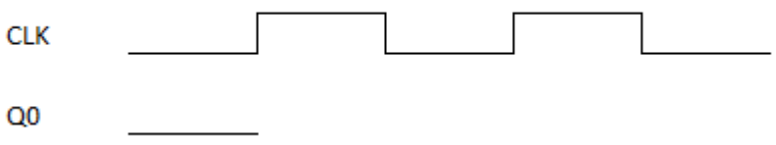


Figure 12

i) If $J_2 = 0$, $K_2 = 1$ and initial value for $Q_2Q_1Q_0 = 101$, what will be the value of $Q_2Q_1Q_0$ after 2 clock pulses when X = 0. Justify your answer. [3 marks]

ii) Complete the timing diagram for Q_0 after clock modification as in Figure 12 when the value of X = 1. [1 mark]



QUESTION 4 (20 marks)

(a) Given a propagation delay of a mod 32 asynchronous recycle up counter using JK flip flop is 50 ns. Answer the following questions.

i) How many flip-flops used in the circuit? [2 marks]

ii) What is the maximum operating frequency? [2 marks]

(b) Figure 13 shows design of a 3-bit synchronous counter using JK flip-flop with negative edge triggered based on the state diagram. Answer the following questions.

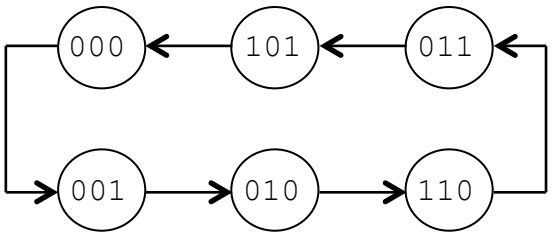


Figure 13

i) Generate the transition table for the counter. [5 marks]

ii) Create the K-map to determine the Boolean expression for each flip-flop. [6 marks]

iv) Draw the implementation of the counter design. Show all inputs and outputs connection clearly. [4 marks]

v) Name the type of counting sequence for this counter. [1 mark]

QUESTION 5 (10 marks)

(a) The shift register in Figure 14 has parallel data input $D_3D_2D_1D_0 = 0111_2$. Develop the data-output waveform in relation to the inputs.

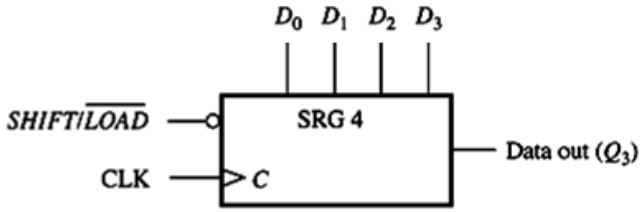
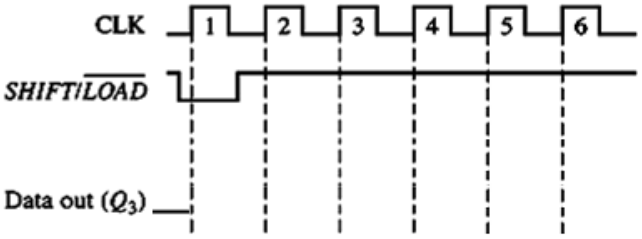


Figure 14

i) What is the function of $SHIFT/\overline{LOAD}$? [1 mark]

ii) Assume the initial value of Q_3 is 0, complete the timing diagram for Q_3. [2 marks]



(b) Given a positive edge JK flip-flop.

i) Design and draw a 4-bit Ring counter. [3 marks]

ii) Draw state diagram of the designed Ring counter. [2 marks]

iii) Modify the counter circuit so that it has a double number of states without adding additional flip-flop. Show the circuit. [2 marks]

------- End of Question -------

GOOD LUCK !