CONFIDENTIAL

UTM
UNIVERSITI TEKNOLOGI MALAYSIA
Faculty of Computing

TEST 2

SEMESTER I 2017/2018

SUBJECT CODE	:	SCSR 1013
SUBJECT TITLE	:	DIGITAL LOGIC
DATE	:	24 November 2017
TIME/DURATION	:	9:00am – 11:15am [2 HOURS 15 MINS]
VENUE	:	DK1, 2, 3, L50
MARKS/PERCENTAGE	:	100 MARKS [25%]

INSTRUCTIONS TO CANDIDATES:

1. There are 2 PARTS. Answer ALL questions in the answer booklet, EXCEPT;
2. Answer question 1 (c) in Part B in this question booklet.

Name			
Matric No.			
Year/Programme		**Section**	
Lecturer (CIRCLE)	FIROZ | HAZINAH | MARINA MOHD FO'AD | MUHALIM | RAJA ZAHILAH		

This questions paper consists of (7) printed pages front and back, EXCLUDING this page.

PART A

1. Which basic logic gate whose output is the complement of the input?
   A. NOT gate
   B. NAND gate
   C. OR gate
   D. AND gate

2. Which logic gate will have a HIGH output when any of its inputs is HIGH?
   A. NOR gate
   B. OR gate
   C. AND gate
   D. NOT gate

3. What is the Boolean expression for a three-input AND gate?
   A. $X = A + B + C$
   B. $X = A – B – C$
   C. $X = A \cdot B \cdot C$
   D. $X = A \$ B \$ C$

4. Logically, the output of a NOR gate would have the same Boolean expression as _____.
   A. an inverter immediately followed by an AND gate
   B. an inverter immediately followed by an OR gate
   C. a NAND gate immediately followed by an inverter
   D. an OR gate immediately followed by an inverter

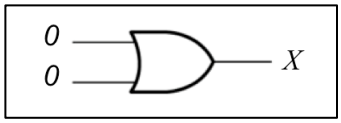
5. For a three-input NOR gate, what is the only condition of inputs A, B and C that will make the output HIGH?
   A. $A = 0, B = 0, C = 0$
   B. $A = 1, B = 1, C = 1$
   C. $A = 1, B = 0, C = 0$
   D. $A = 0, B = 0, C = 1$

6. Which of the expressions below expresses the commutative law of multiplication?
   A. $A + B = B + A$
   B. $AB = B + A$
   C. $AB = BA$
   D. $AB = A / B$

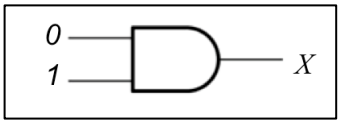
7. Which of the expressions below expresses the distributive law?
   A. $(A + B) + C = A + (B + C)$
   B. $A(B + C) = AB + AC$
   C. $A + (B + C) = AB + AC$
   D. $A(BC) = (AB) + C$

8. Which of the following diagram proves the Boolean Algebra rule $A + \overline{A} = 1$?

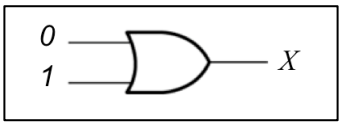
A.



C.



B.



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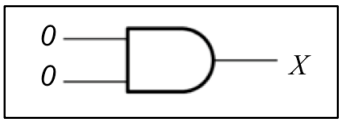


9. Which Boolean Algebra rule is false?
   A. A + 0 = A
   B. A + 1 = 1
   C. A . A = 1
   D. A . 1 = A

10. Simplify the expression $\overline{\overline{(AB)} + C}$ using DeMorgan's Theorems.
   A. $(A + B)C(A + B)C$
   B. $\overline{\overline{AB} + C}$
   C. $AB\overline{C}$
   D. $AB + \overline{C}$

11. Choose the expression that is not in standard form.
   A. $\overline{A}B\overline{C}D$
   B. $\overline{A}BC + A\overline{B}C$
   C. $(\overline{A} + B)(A + \overline{B})(\overline{A} + B)$
   D. $(A + B + \overline{C})(A + \overline{B} + D)$

12. Which of the following terms is a standard SOP form?

A. $(A+B+\overline{C}+D)$

B. $A\overline{B}CD+\overline{ABCD}$

C. $(A+B+\overline{C}+D)(\overline{A}+\overline{B}+\overline{C}+\overline{D})$

D. $A\overline{B}CD+ABCD$

13. Which binary value does not match any of the product term in $ABC\overline{D}+A\overline{B}\overline{C}D+\overline{A}B\overline{C}D$?

A. 1110_2

B. 1001_2

C. 0101_2

D. 0110_2

14. Which POS expression match the binary value of *001*?

A. $AB\overline{C}$

B. $\overline{A}\overline{B}C$

C. $A+B+\overline{C}$

D. $\overline{A}+\overline{B}+C$

15. Which term is represented in $\sum_{ABC}(0,3,5,7)$?

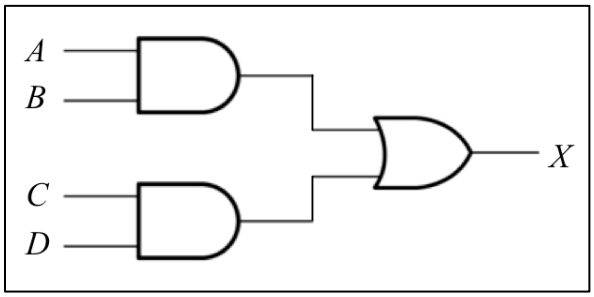
A. $\overline{A}\overline{B}C$

B. $A\overline{B}C$

C. $\overline{A}+B+\overline{C}$

D. $\overline{A}+\overline{B}+\overline{C}$

16. Choose the true statement about the AND-OR logic diagram.



A. It produces a SOP output expression.

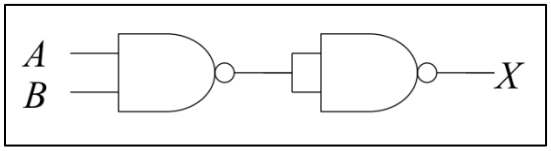
B. It produces a POS output expression.

C. The output *X* is HIGH if both inputs *A* and *C* are HIGH.

D. The output *X* is only HIGH when all inputs are HIGH.

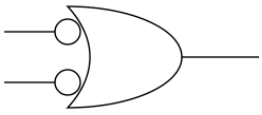
17. If an inverter is added to the output *X* of an AND-OR logic circuit, it will produce a _____.
    A. POS for *X*
    B. SOP for *X*
    C. POS for $\overline{X}$
    D. SOP for $\overline{X}$

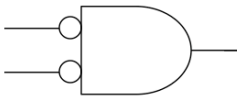
18. This logic symbol can function as a/an _____ gate.

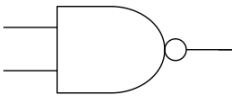


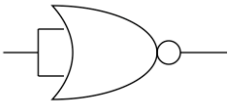
    A. NAND
    B. NOT
    C. OR
    D. AND

19. Which of the following logic symbol can be represented as an appropriate dual symbol for a NAND gate?

A. 

C. 

B. 

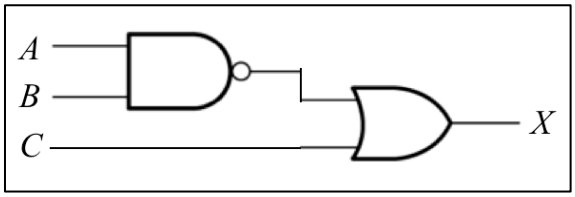
D. 

20. The appropriate dual symbol for a NOR gate is known as _____.
    A. negative-OR
    B. inverter
    C. bubble
    D. negative-AND

PART B

QUESTION 1 [20 MARKS]

a) Given the following logic circuit:

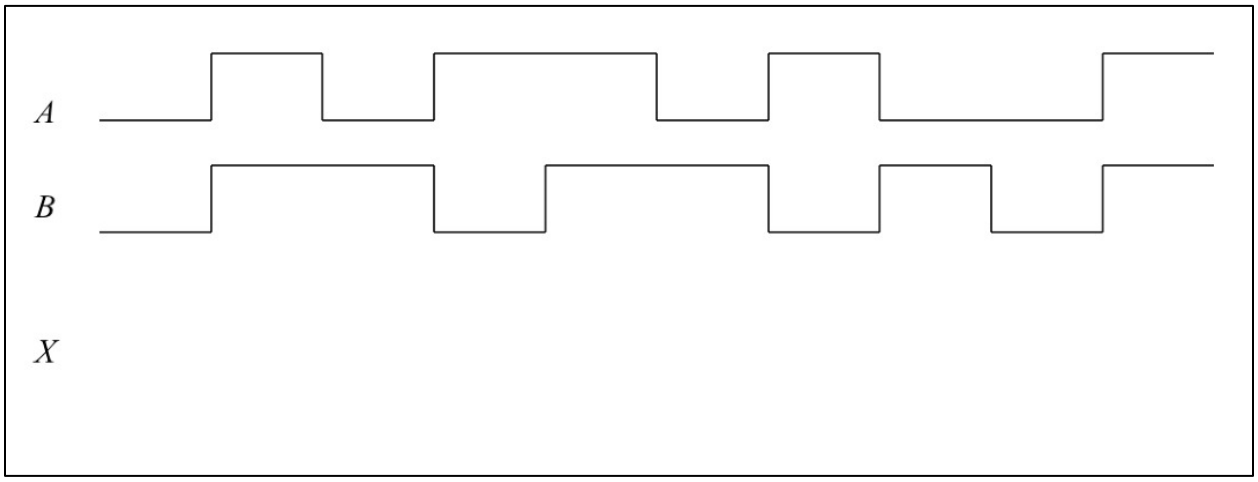


(i) Identify the two logic gates used in the circuit. [1m]

(ii) Get the Boolean expression for *X*. [2m]

b) Give the complete truth table for XOR gate with 2 inputs and 1 output. [3m]

c) Determine the XNOR gate output for the following input waveforms. Draw the timing diagram of the output *X* in the figure. [5m]
[Note: Answer this question in the diagram below.]



d) Using Boolean Algebra, simplify the following expressions.

(i) $(A + C)\left(AD + A\overline{D}\right) + AC + C$ [4m]

(ii) $\overline{A}\,\overline{B}\,C + \left(\overline{A + B + \overline{C}}\right) + \overline{A}\,\overline{B}\,\overline{C}\,D$ [5m]

QUESTION 2 [30 MARKS]

a) Convert the expression to its standard form. [4m]

$$X = (A + B + \overline{D})(\overline{A} + \overline{C})$$

b) Given the expression $X = \tilde{O}_{ABC}(2,3,4,7)$;

(i) Construct the truth table for *X*. [5m]

(ii) Write the complete standard POS Boolean expression for *X*. [3m]

(iii) Write the complete standard SOP Boolean expression for *X*. [3m]

(iv) Construct the complete Karnaugh Map (K-Map) for the expression for *X*. [3m]

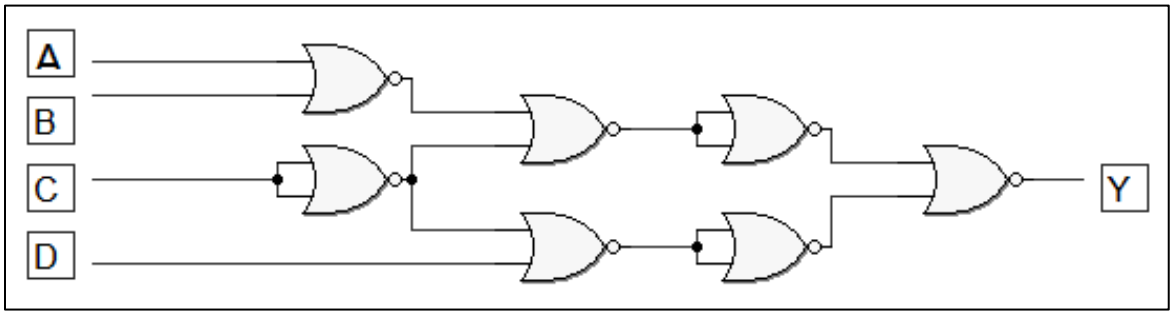
c) Given the expression $Y = \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}CD + \overline{A}B\overline{C}D + \overline{A}BC\overline{D} + \overline{A}BCD + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D$;

(i) Produce the simplified SOP expression using K-Map. [6m]

(ii) Redraw the K-Map to include the "don't care" conditions, $d(10,11,12,13,14,15)$ and produce the new simplified SOP expression. [6m]

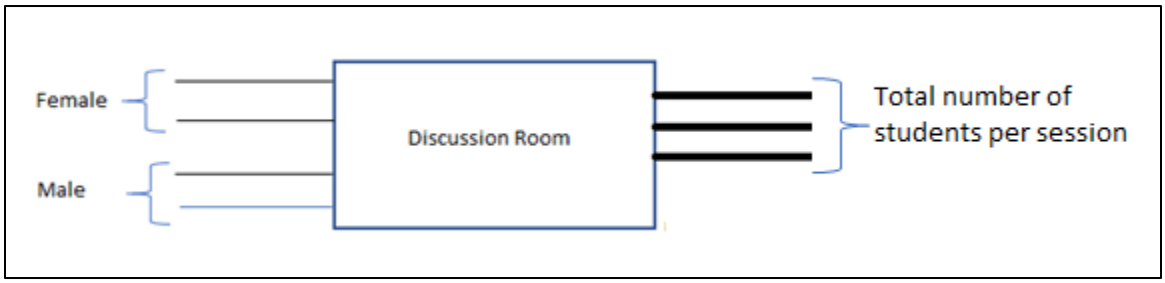
QUESTION 3 [30 MARKS]

a) Redraw the logic diagram for the circuit below using the appropriate dual symbols to produce a circuit with the minimum number of basic gates only. [5m]



b) A small discussion room with one table and five chairs is opened for students daily. For each session, maximum of 3 female and maximum of 3 male students can enter the room. The rules for using the room is as follows:

- The room cannot be empty because there are always students waiting to use the room.
- Single female student cannot enter the room.
- Number of students allowed per session is minimum 2 and maximum 5.



(i) Design a combinational logic circuit to calculate the total number of students in each session. Implement the circuit using the minimum number of NAND gates only. [22m]
Hint: Please use 3-input gates where possible.

(ii) List down all the combinations of student's formation allowed for each session. [3m]