SULIT

Faculty of Computing

UNIVERSITI TEKNOLOGI MALAYSIA

FINAL EXAMINATION SEMESTER I, 2016 / 2017

SUBJECT CODE :

SUBJECT NAME :

SECTION :

TIME :

DATE/DAY :

VENUES :

INSTRUCTIONS :

Answer all questions from **Part A** and **B** in this question booklet. For **Part B**, read the questions carefully and show **ALL** your works in details.

This examination will contribute 35% towards the total marks of 100 points.

Warning!
Students who are caught cheating during the examination will be reported to disciplinary board for action to suspend the student for one or two semesters.

(Please Write Your Lecturer Name And Section In Your Answer Booklet)

Name	
I/C No.	
Year / Course	
Section	
Lecturer Name	

This question paper consists of ____ (__) printed pages excluding this page.

PART A: 15 OBJECTIVE QUESTIONS [Total mark 15 points]

Answer all the questions. Read each statement carefully. Please answer in Attachment A (page 10).

1. One of the parallel adder types that is based on how it handles a carry value is a _____ carry adder.

   A) generation
   B) look back
   C) override
   D) ripple

2. A decoder uses _____ gate if we want the output to be **HIGH**.

   A) AND
   B) OR
   C) NAND
   D) XNOR

3. Choose the **FALSE** statement about **DEMUX**.

   A) It is also known as a data selector.
   B) A DEMUX is basically the reverse of the multiplexing function.
   C) It takes digital information from one line and distributes it to a given number of output lines.
   D) A decoder can also be used as a DEMUX.

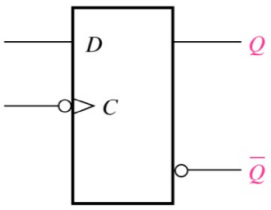
4. 

Figure 1

   Select the **CORRECT** characteristic of the Figure 1 above.

   A) It is a negative edge-triggered flip-flop.
   B) It is a negative edge-triggered latch.
   C) It is a positive edge-triggered flip-flop.
   D) It is a positive edge-triggered latch.

5. Which of the following statements is **FALSE** about the characteristics of sequential and combinational logic circuits?

A) Combinational logic circuit does not contain memory element compared to sequential logic circuit.

B) In order to be fully functional, both combinational and sequential logic circuits require input clock triggered.

C) Sequential logic circuit considers the previous state output before the current output circuit is produced.

D) Sequential logic circuit can be constructed using basic logic gates and memory devices.

6. Which of the following statements is **FALSE** about a latch and a flip-flop?

A) Latch and flip-flop can store binary bit 0 or 1.

B) A latch requires a clock input before output latch can be changed.

C) A flip-flop output will change according to the input flip-flop at the clock edge triggered.

D) A latch output will change according to the input level of the latch.

7. Which of the following statements is **FALSE** about an S-R latch?

A) It has a SET state.

B) It has a RESET state.

C) It has a HOLD state.

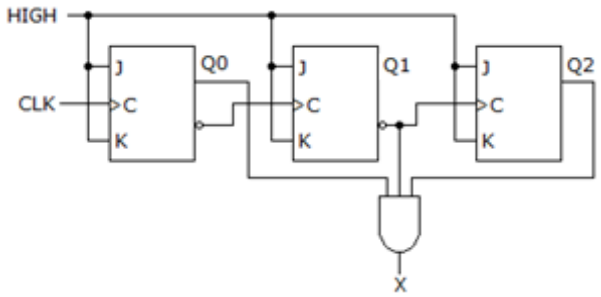
D) It has a TOGGLE state.

8. How many different states does a 3-bit asynchronous counter has?

A) 3 C) 8

B) 6 D) 9

9. What is the state value (in decimal) of Q2, Q1 and Q0 in the following circuit in order to produce a **HIGH** output at **X**?



A) 5 C) 7

B) 6 D) 8

10. What is the maximum state of a typical MOD 10 (decade) binary counter?

A) 0000
B) 1010
C) 1111
D) 1001

11.

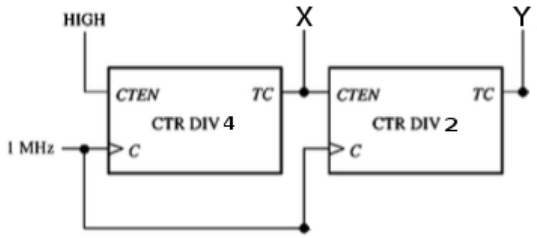


Figure 2

Referring to Figure 2, what is the signal frequencies of X and Y?

A) X = 0.25 MHz, Y = 0.125 MHz.
B) X = 4 MHz, Y = 2 MHz.
C) X = 0.125 MHz, Y = 0.25 MHz.
D) X = 2 MHz, Y = 4 MHz.

12. Which of the following statements is **TRUE** about synchronous counter?

A) Synchronous counter can count up and count down simultaneously (with the same clock cycle).
B) If synchronous counter is implemented with N flip-flops in its sequential circuit, the number of valid states of the counter is always 2^N.
C) Synchronous counter can be implemented using D flip-flops, as long as the clock source of the flip flops is taken from the common clock source.
D) Synchronous counter can be implemented using any type of flip-flop, as long as the clock source of flip flops is taken from the output of the preceding flip-flops.

13. The following are Shift Registers, **EXCEPT**:

A) SISO Serial In, Serial Out
B) SIPO Serial In, Parallel Out
C) SILO Serial In, Last Out
D) PIPO Parallel In, Parallel Out

14. The following statements are true about Shift Register (SR) **EXCEPT**:

A) SR stores binary data
B) SR performs data rotate
C) SR consists of several latches
D) SR is used for data transfer

15. A **MOD 10** Ring counter requires _____.

A) ten flip-flops
B) five flip-flops
C) four flip-flops
D) eight flip-flops

PART B: 4 SUBJECTIVE QUESTIONS [Total mark 85 points]

Question 1 [15 Marks]

Answer the following questions about some functions of combinational logic.

(a) A logic symbol of a parallel adder for summing TWO binary numbers is illustrated in Figure 3. If A = 0011_2 and B = 0110_2 with the carry in, C_0 = 0, complete Table 1 by reproducing it in your answer booklet. Assume pin label 1 represents LSB. [4M]

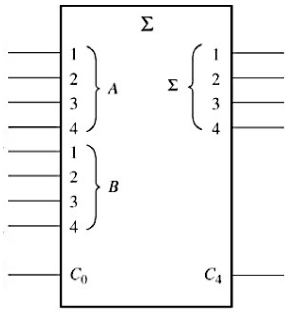


Figure 3

Table 1

Pin Label (i)	Input		Carry Out	Sum
	A_i	B_i	C_i	Σ_i

(b) Draw the logic circuit for a binary decoder to detect the binary code 10010 which produces an active-LOW output. Assume the inputs are represented as $A_4A_3A_2A_1A_0$. [3M]

(c) Given an active HIGH 7-segment display in Figure 4 displaying a digital number from a decoder that based on the BCD value, fill in Table 2. Reproduce Table 2 in your answer booklet. [4M]

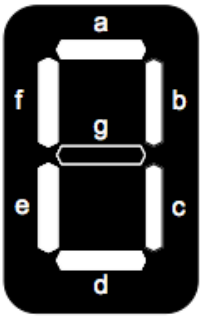


Figure 4

Table 2

BCD Input				Segment Output							Display
A	*B*	*C*	*D*	*a*	*b*	*c*	*d*	*e*	*f*	*g*	
											4
											7
1	0	0	1								9

(d) Figure 5 (in page 11) shows the waveforms of data-input D_i and data-select S_i applied to a multiplexer. Complete Figure 5 by drawing the waveform output of ***X*** in relation to the inputs. Label each segment of output ***X*** with the correct data input selection. [4M]

Question 2 [15 Marks]

(a) Figure 6 shows a basic circuit of a latch. Answer the following based on the circuit.

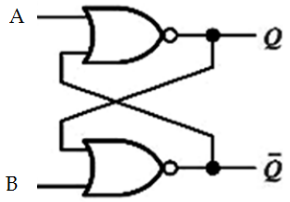


Figure 6

(i) Complete the following truth table with initial values of Q and $\overline{Q}$ are bit 1 and 0. [4M]

Input		Output		State
A	B	Q	$\overline{Q}$	
0	0			
0	1			
1	0			
1	1			

(ii) What type of latch is represented by the circuit in Figure 6? [1M]

(b) Referring to Figure 7 in page 12, complete the output $\boldsymbol{Q}$ for a Gated $\overline{S}$ - $\overline{R}$ latch. Label each state that occurs for each transition in the timing diagram. [3M]

(c) Referring to Figure 8, answer the following questions. Assume Q is initially low.

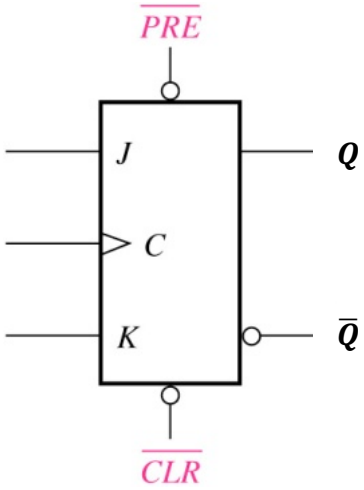


Figure 8

(i) Draw output $\overline{\boldsymbol{Q}}$ in the timing diagram at page 12. [3M]

(ii) List the input priority of the flip-flop from the highest to the lowest. [2M]

(d) Draw the implementation of negative edge T flip-flop by using JK flip-flop. [2M]

Question 3 [40 Marks]

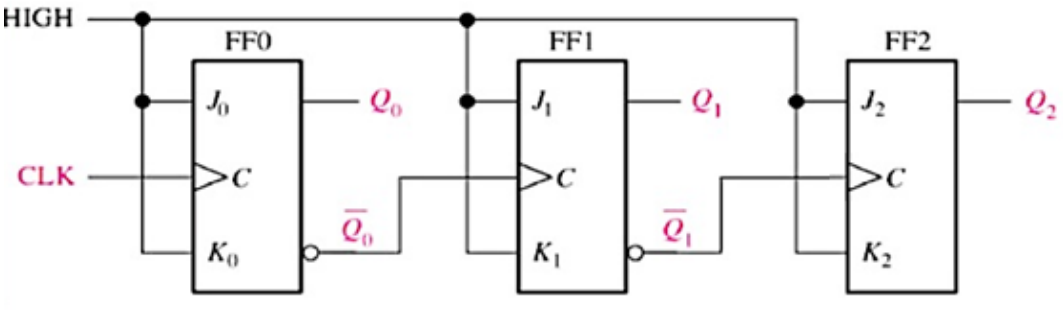


Figure 9: Asynchronous binary counter

(a) Based on Figure 9, draw the State Diagram for the counter by using binary representation. [4M]

(b) Redesign Figure 9, by considering new requirements as follows:

- 3-bit count up ripple counter with Modulus-5;
- using J-K Flip-Flop and
- with negative edge triggered clock. [6M]

(c) Rolek Corp is designing its new 2-bit binary counter. The state diagram of the counter is given in Figure 10:

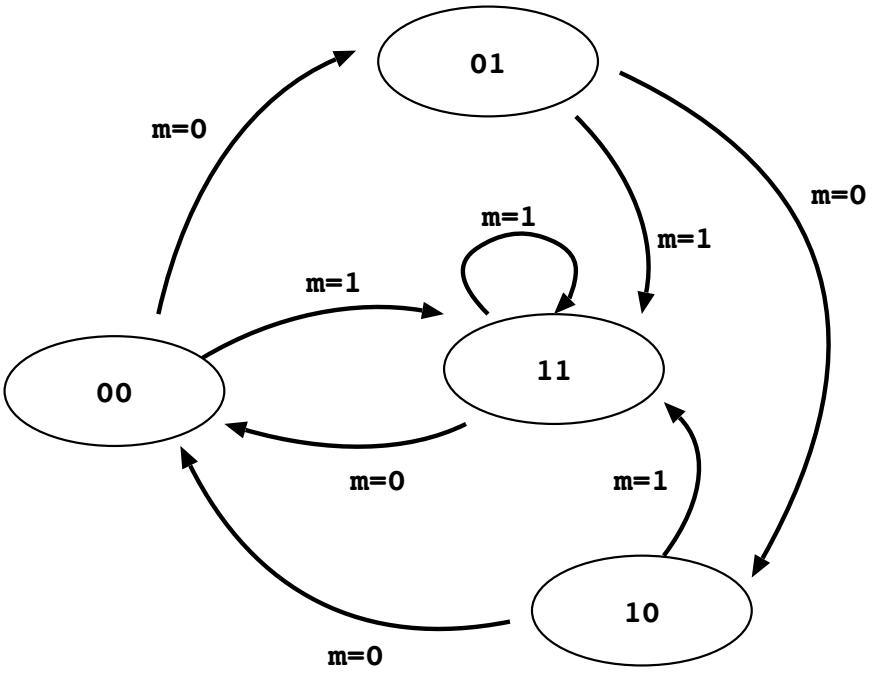


Figure 10: State Diagram for 2-bit Rolek binary synchronous counter

Using T flip-flops, design the sequential logic circuit of the latest Rolek binary counter as specified above, by answering all questions below.

(i) Complete the following Next State and Transition Table. [8M]

Input	Present State		Next State		FF_1	FF_0
m	Q_1	Q_0	Q_1	Q_0	T_1	T_0

(ii) Get the optimized SOP Boolean expressions using K-Map. [4M]

(iii) Draw the complete final circuit design. [3M]

(d) For the sequential circuit shown in Figure 11, answer the following questions:

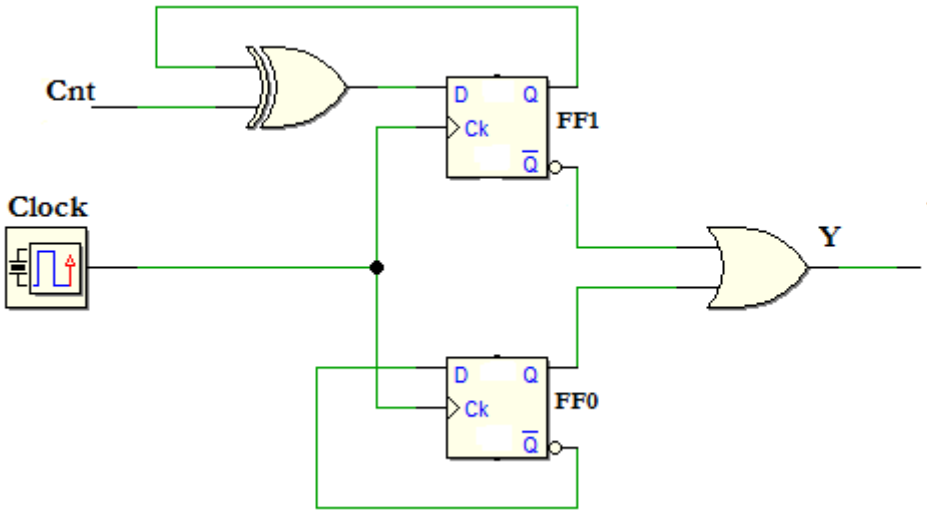


Figure 11: Sequential Circuit

(i) Derive the next-state equations for each flip-flop and output Y. [3M]

(ii) Produce the next state table. [8M]

(iii) Draw the state diagram. [4M]

Question 4 [15 Marks]

(a) Initially at t_0, a 5-bit SIPO shift register is cleared. Then, at $\mathbf{t_1}$ the data word $\mathbf{19_{10}}$ is serially entered. **LSB** is shifted in first.

(i) Draw the circuit for a 5-bit SIPO using D flip-flop. [3M]

(ii) What are the content of the SIPO shift register at $\mathbf{t_3}$? Show your works in a table form. [3M]

(iii) At what clock cycle can all the input data be read at the output and state the output [2M]

(b) Answer the following questions based on a Johnson counter.

(i) Draw the logic diagram for a MOD 8 Johnson counter. [3M]

(ii) Write the counting sequence in a table form. Initially the content of all flip-flops are binary '0'. [4M]

All the best!!! Show ALL your works.

ATTACHMENT A

Name	
Matric No.	
Lecturer	**Dr. Foad | Dr. Ismail | Dr. Raja Zahilah** **Mr. Muhalim | Ms Rashidah | Ms. Marina**

Objectives	**/15**
Question 1	**/15**
Question 2	**/15**
Question 3	**/40**
Question 4	**/15**
Total	**/100**

PART A (OBJECTIVE)

Mark your answer clearly.

Example: =A= =B= =C= =D=

1. =A= =B= =C= =D=

2. =A= =B= =C= =D=

3. =A= =B= =C= =D=

4. =A= =B= =C= =D=

5. =A= =B= =C= =D=

6. =A= =B= =C= =D=

7. =A= =B= =C= =D=

8. =A= =B= =C= =D=

9. =A= =B= =C= =D=

10. =A= =B= =C= =D=

11. =A= =B= =C= =D=

12. =A= =B= =C= =D=

13. =A= =B= =C= =D=

14. =A= =B= =C= =D=

15. =A= =B= =C= =D=

ATTACHMENT B

Answer for Question 1 (d)

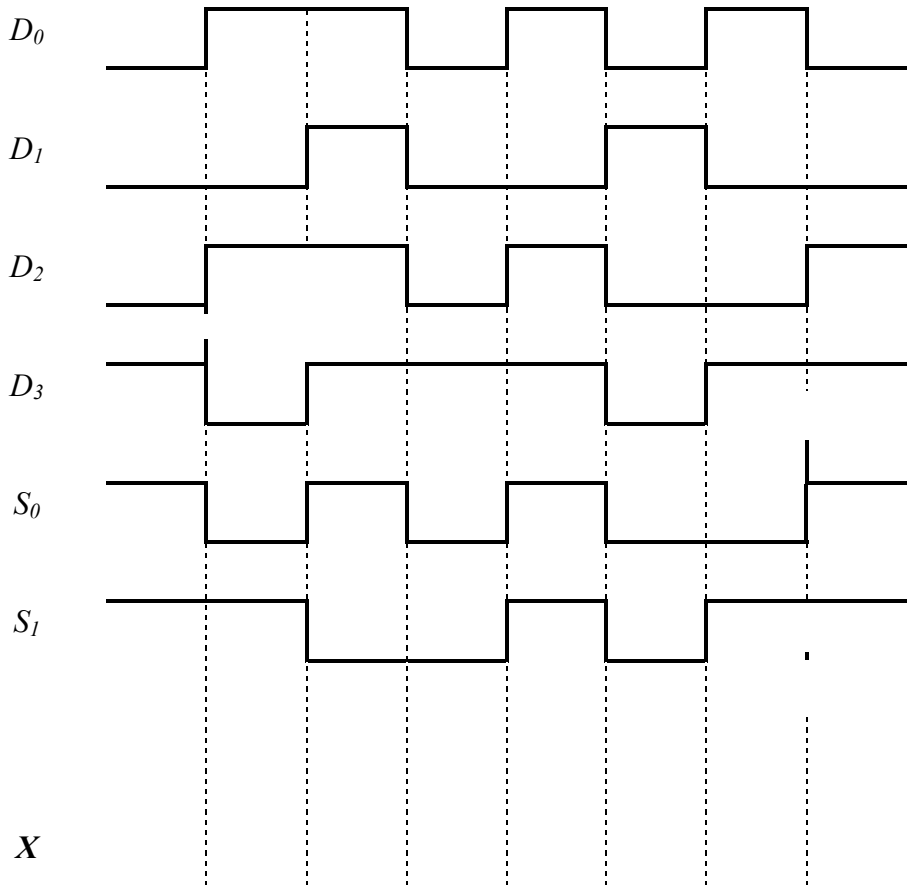


Figure 5

Answer for Question 2 (b)

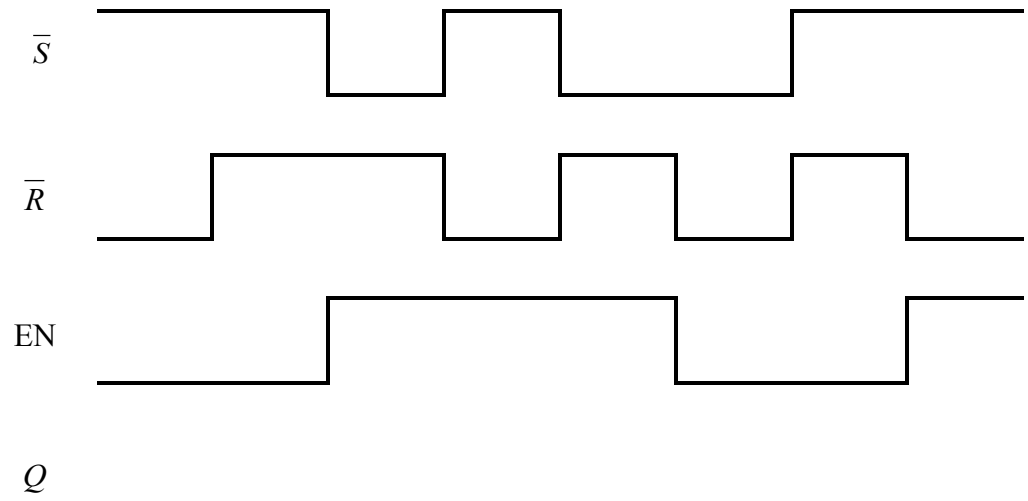


Figure 7

Answer Question 2 (c)(i)