SUBJECT CODE	:	SCSR1013
SUBJECT NAME	:	DIGITAL LOGIC
DURATION	:	**2 HOURS 45 MINUTES**

(Instructions to Candidates) :

1. Please answer PART A in the OBJECTIVE ANSWER SHEET given in PAGE 6 of this question booklet.
2. Please answer Questions 2 (a, b, c) and 5 (c) of PART B in the TIMING DIAGRAMS in this question booklet.
3. Please answer ALL OTHER questions of PART B in the ANSWER BOOKLET given.

THIS QUESTION PAPER CONSISTS OF THIRTEEN (13) PRINTED PAGES NOT INCLUDING THIS FRONT PAGE

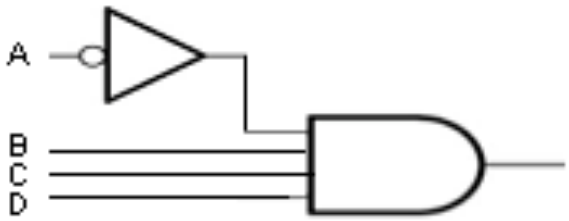
PART A: 20 OBJECTIVE QUESTIONS [20 MARKS]

INSTRUCTION: Answer PART A in the OBJECTIVE ANSWER SHEET given in PAGE 6.

1. Which of the following is NOT a type of Adder?
   A. Half
   B. Full
   C. Regulator
   D. Parallel

2. Which of the following functions can be used to detect whether your bank account balance is ZERO?
   A. Parity generator
   B. Multiplexer
   C. Comparator
   D. Encoder

3. When the output is active-HIGH for the decoding gate shown below, what is the binary code appearing on the inputs? The MSB is A.



   A. 1110
   B. 0111
   C. 1100
   D. 1000

4. _____ reduces the number of bits needed to represent given information.
   A. Parity Checker
   B. Parity Generator
   C. Decoder
   D. Encoder

5. MUX is also known as _____.

   A. data distributor

   B. data selector

   C. adder

   D. decoder

6. Which of the following is NOT a latch?

   A. S-R latch

   B. J-K latch

   C. Gated S-R latch

   D. Gated D latch

7. The invalid state for S-R latch occurs when S and R are _____.

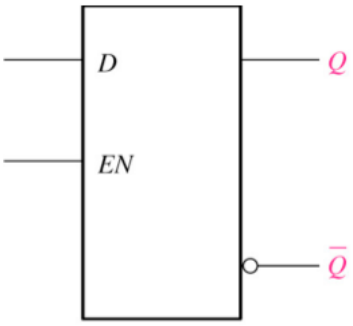
   A. both high

   B. both low

   C. S = high, R = low

   D. S = low, R = high

8. The figure below shows what type of temporary storage device?



   A. D flip flop

   B. Gated-D latch

   C. Gated S-R latch

   D. C-D flip flop

9. Which flip-flop is versatile and widely used?

   A. Edge-triggered D

   B. S-R

   C. J-K

   D. T

10. Choose the CORRECT statement.

   A. Synchronous counter has clocks from the same source.

   B. Synchronous counter has clocks from the different sources.

   C. Asynchronous counter has clocks from the same source.

   D. Asynchronous counter doesn't have clock input.

11. For 5-bit counter, what is the range of the count?

   A. 0 to 4

   B. 1 to 5

   C. 0 to 31

   D. 1 to 32

12. Which mod is NOT a truncated sequence?

   A. Mod 8

   B. Mod 9

   C. Mod 10

   D. Mod 11

13. _____ counter goes back to the first count after the maximum count.

   A. A saturated

   B. An infinity

   C. A random

   D. A recycle

14. If a propagation delay of an asynchronous recycle UP counter using FIVE (5) J-K flip-flop is 2 seconds, what is the maximum operating frequency?

A. 0.1 Hz

B. 0.2 Hz

C. 0.5 Hz

D. 2 Hz

15. The table below shows an excitation table for which flip-flop?

Q_{n+1}	Input flip-flop
Q_n	0
$\overline{Q_n}$	1

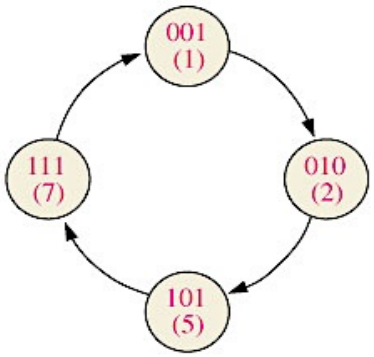
A. D

B. T

C. J-K

D. None of the above

16. Given the state diagram in the figure below, choose the CORRECT statement?



A. The counter is a 2-bit counter.

B. There are 2 valid states.

C. There are 4 invalid states.

D. Total number of states is 16.

17. What is the maximum number of states for two counters, modulus-3 and modulus-4 connected in cascade?

A. 3

B. 4

C. 7

D. 12

18. To serially shift a BYTE of data into a shift register, there must be how many clock pulse(s)?

A. 1

B. 2

C. 3

D. 8

19. A MOD 8 ring counter requires how many flip-flops?

A. 2

B. 4

C. 8

D. 16

20. In the Johnson counter, the _____ is fed back as an input to the first flip-flop.

A. first output

B. first complemented output

C. last output

D. last complemented output

OBJECTIVE ANSWER SHEET FOR PART A

Name			
Matric No.			
Lecturer (Circle)	**MOHD FO'AD FIROZ**	**ISMAIL FAUZI MUHALIM**	**SITI HAJAR MARINA**

INSTRUCTION: MARK YOUR ANSWER CLEARLY

Example: =A= =●= =C= =D=

1. =A= =B= =C= =D=

2. =A= =B= =C= =D=

3. =A= =B= =C= =D=

4. =A= =B= =C= =D=

5. =A= =B= =C= =D=

6. =A= =B= =C= =D=

7. =A= =B= =C= =D=

8. =A= =B= =C= =D=

9. =A= =B= =C= =D=

10. =A= =B= =C= =D=

11. =A= =B= =C= =D=

12. =A= =B= =C= =D=

13. =A= =B= =C= =D=

14. =A= =B= =C= =D=

15. =A= =B= =C= =D=

16. =A= =B= =C= =D=

17. =A= =B= =C= =D=

18. =A= =B= =C= =D=

19. =A= =B= =C= =D=

20. =A= =B= =C= =D=

PART B: SUBJECTIVE QUESTIONS [80 MARKS]

QUESTION 1 [15 MARKS]

a) Two binary numbers are given as, A = $\{A_2A_1A_0\} = 011_2$ and B = $\{B_2B_1B_0\} = 110_2$.

i. Design a parallel adder using Full Adder. Label the diagram with A_0, A_1, A_2, B_0, B_1, B_2, $\sum_0$, $\sum_1$, $\sum_2$, C_{in}, C_{out}, MSB, LSB and GND (ground). [4m]

ii. Perform the arithmetic addition A + B, and label all the values in (i). [3m]

iii. Based on how Full Adder handles the carry bit, list TWO types of parallel adder. [2m]

b) Figure 1 shows the symbol of one of combinational logic functions.

i. Name the combinational logic function X and describe its purpose. [2m]

ii. Reproduce Table 1 in the answer booklet and fill it up with the correct answers. [4m]

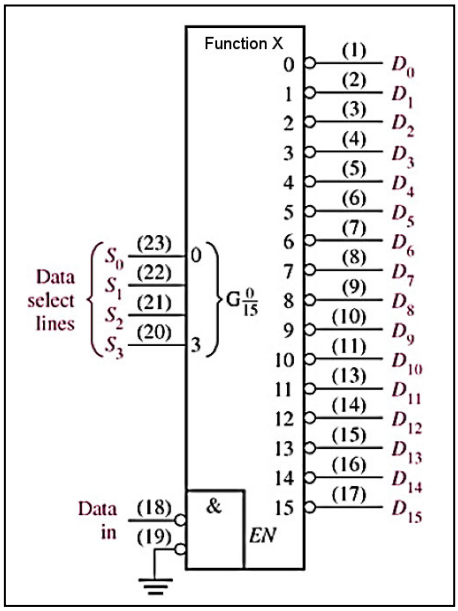


Figure 1: The symbol of combinational logic function X

Table 1

Data In	**S_3**	**S_2**	**S_1**	**S_0**	**Selected Output Pin**	**Output Signal Level**
H	H	H	L	H		
L					D_5	
					D_9	H
	L	H	L	L		L

Note: H = High = 1, L = Low = 0.

QUESTION 2 [15 MARKS]

*** Answer Questions (a), (b) & (c) in the Timing Diagrams of Figures 2 to 4 in this Question Booklet.**

a) Determine the timing diagram in Figure 2 for output Q for $\overline{S} - \overline{R}$ latch. Assume that Q is initially **LOW**. Draw your answer in Figure 2. [3m]

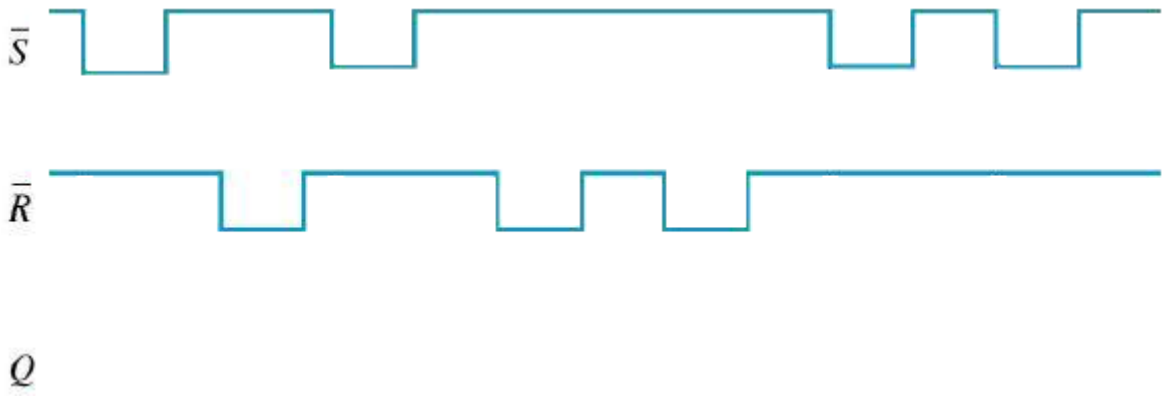


Figure 2: Timing Diagram for $\overline{S} - \overline{R}$ Latch

b) Determine the timing diagram in Figure 3 for output Q for gated S-R latch. Assume that Q is initially **LOW**. Draw your answer in Figure 3. [3m]

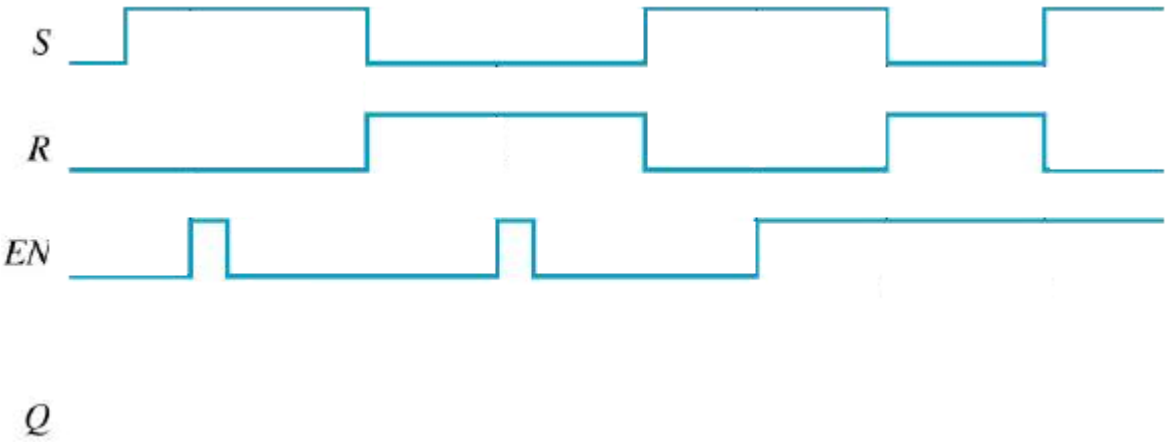


Figure 3: Timing Diagram for Gated S-R Latch

c) Determine output Q in Figure 4 for a positive edge triggered clock J-K flip-flop with $\overline{PRE}$, $\overline{CLR}$, and J, K inputs. Assume that Q is initially **LOW**. Draw your answer in Figure 4. [5m]

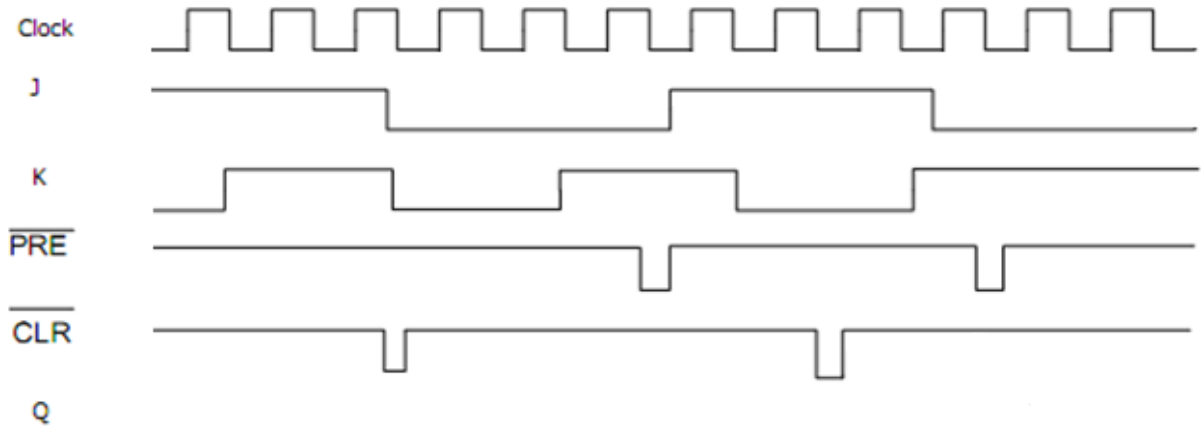


Figure 4: Timing Diagram for a J-K flip-flop

d) Using a positive edge J-K flip flop, built/draw in the ANSWER BOOKLET: [4m]

i. a D flip flop
ii. a T flip flop

~ END OF QUESTION 2 ~

QUESTION 3 [10 MARKS]

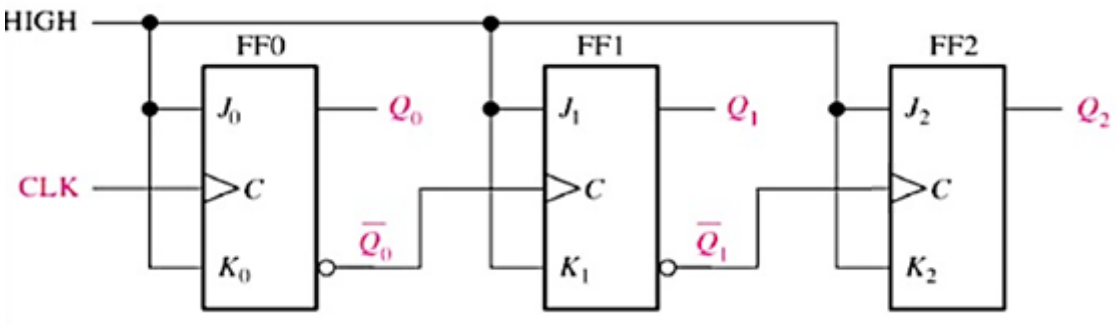


Figure 5: Connection of Logic Symbol for an Asynchronous Binary Counter

a) Based on Figure 5, draw the state diagram for the counter by using binary representation. [4m]

b) Redesign the connection of logic symbol for a:

- 3-bit count UP ripple counter,
- asynchronously clocked (truncated) MODULUS-5
- using J-K flip-flop
- with NEGATIVE edge triggered clock. [6m]

~ END OF QUESTION 3 ~

QUESTION 4 [30 MARKS]

a) Using J-K flip-flops, design a 3-bit up/down synchronous counter based on state diagram shown in Figure 6.

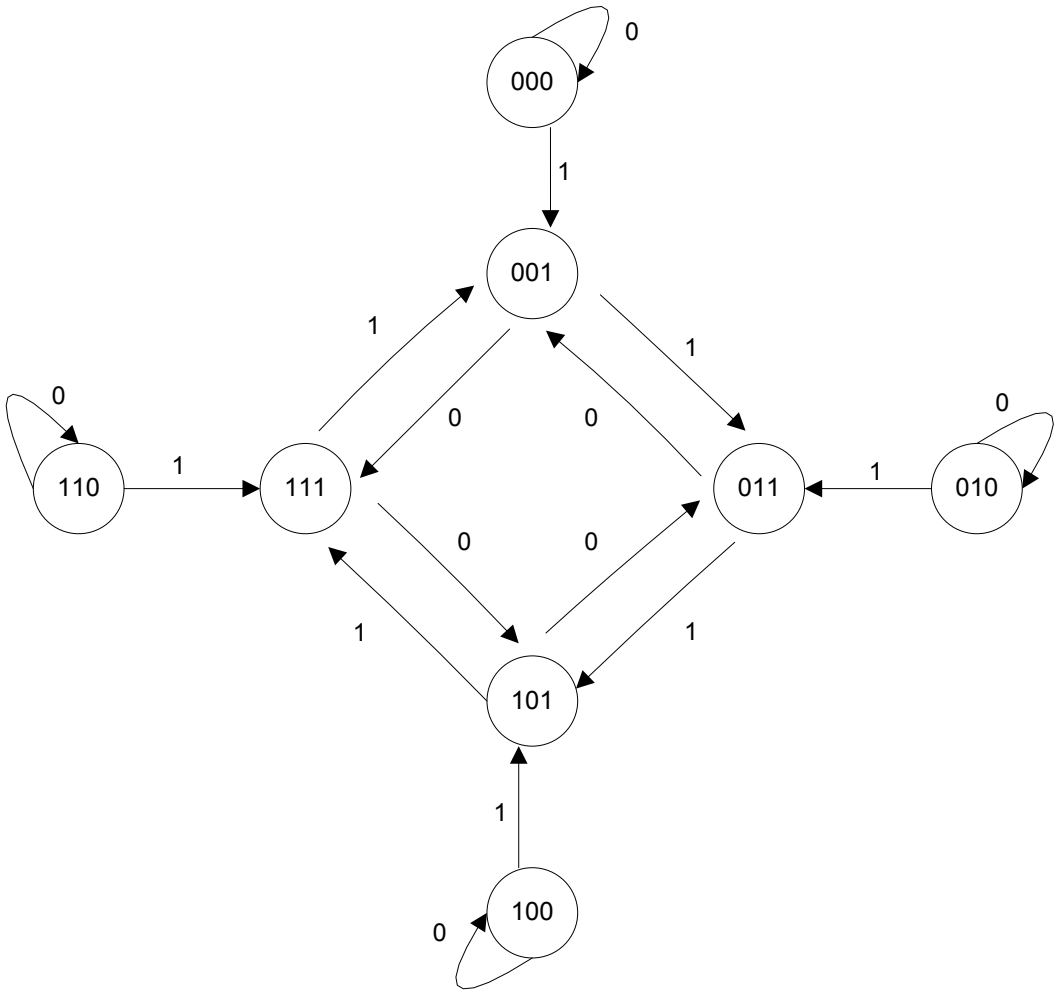


Figure 6: State Diagram for 3-bit Up/Down Synchronous Counter

i. Complete the following Next State and Transition Table. [14m]

Present (Q_n)				Next (Q_n^+)			FF2		FF1		FF0	
X	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0

ii. Get the optimized SOP Boolean expressions using K-Map. [9m]

iii. Draw the complete final circuit design. [3m]

b) Based on the circuit in Figure 7, answer the following:

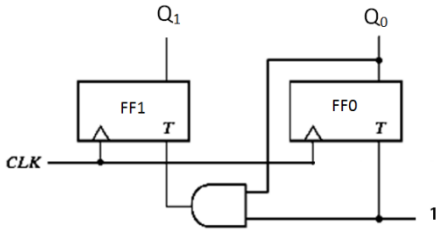


Figure 7

i. Get Boolean expression for the input of T flip-flops of FF1 and FF0. [1m]

ii. From the answer in (i), determine what is the next state if the current state of T flip-flops is $Q_1Q_0 = 10_2$. [3m]

~ END OF QUESTION 4 ~

QUESTION 5 [10 MARKS]

a) By showing every single label (data input/s, data output/s and shift register label), draw logic symbol for the following: [4m]

i. 8-bit PISO shift register.

ii. 6-bit SIPO shift register.

b) Show the output waveform of a 5-bit PISO shift register if the data input entered is $D_4D_3D_2D_1D_0$ =**10011_2**. D_4 represents MSB and it will be shifted out first. Draw your answer in Figure 8. [3m]

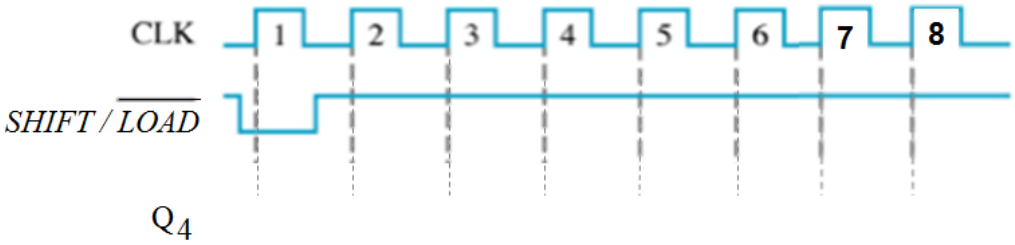


Figure 8: Waveform of PISO Shift Register

c) Table 2 shows the initial output values produced by each flip-flop of the **5-bit Johnson** counter. Complete the counting sequence **upto 6 clock pulses** as in Table 2 in the answer booklet [3m]

Table 2

Clock Pulse	Q_4	Q_3	Q_2	Q_1	Q_0
Initial Condition	0	0	0	0	0

EXTRA DESIGN QUESTION

Question 5 (25M)

You are required to design a security system for an exhibition of an expensive diamond. To protect the diamond on display, only 5 peoples are allowed to view the diamond at one time. There are two sensors, one at the entrance and the other is at the exit as shown in Figure 7. The counter is used to count the number of visitor in the exhibition hall. Whenever a visitor enter at the entrance the sensor will generate a HIGH (logic 1) and the counter will be incremented by one to reflect the number of visitor at the exhibit. If the visitor exited the exhibition hall the sensor will generate a LOW (logic 0) and counter will be decremented by one. Only one visitor can enter or exit at any one time. The entrance will be locked (no visitor allowed to get in) if the number of visitor in the exhibition hall are 5, a new visitor can enter only after at least one of the visitor exited the exhibition hall. Assume visitor cannot enter and exit the exhibition hall at the same time.

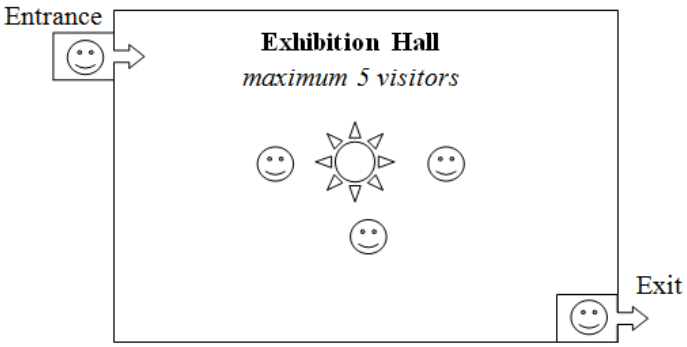


Figure 7

Design the circuit using D flip-flop by doing the following steps:

i) Draw the state diagram.

ii) Produce next state table.

iii) Get the Boolean expression for each input of the flip-flops.

iv) Draw the circuit diagram.

Hint: Design the counter where its count direction is determined by whether a visitor enter or exit the exhibition hall.

(25M)