Extra

Exercise 8b.3: Design 2-bit synchronous counter that using D flip-flop. Show all steps clearly.

Extra

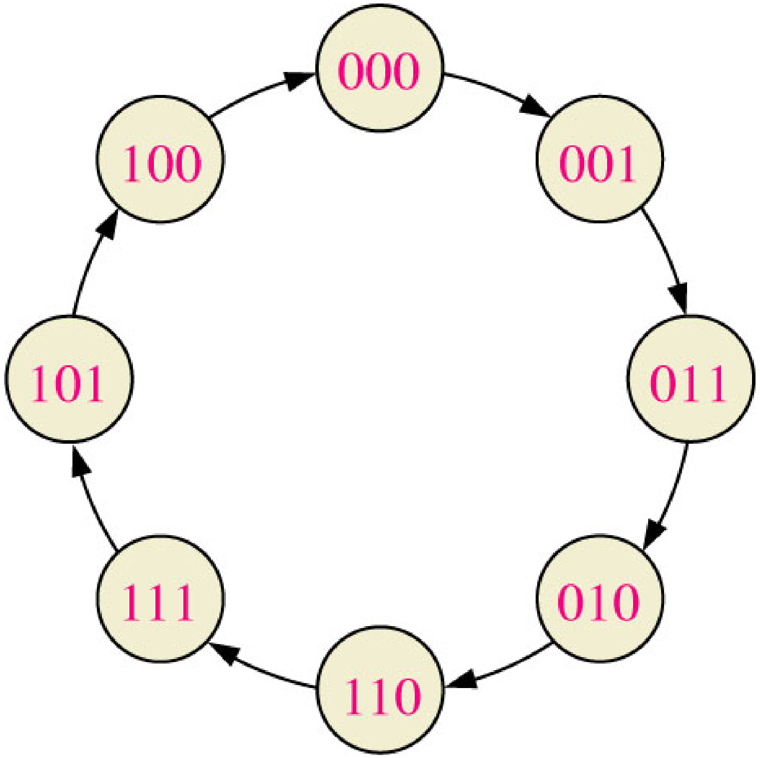
Exercise 8b.5: Design 3-bit synchronous counter that using T flip-flop. Show all steps clearly.

Extra

Exercise 8b.6: Design 4-bit synchronous counter that using J-K flip-flop with negative edge triggered. Show all steps clearly.

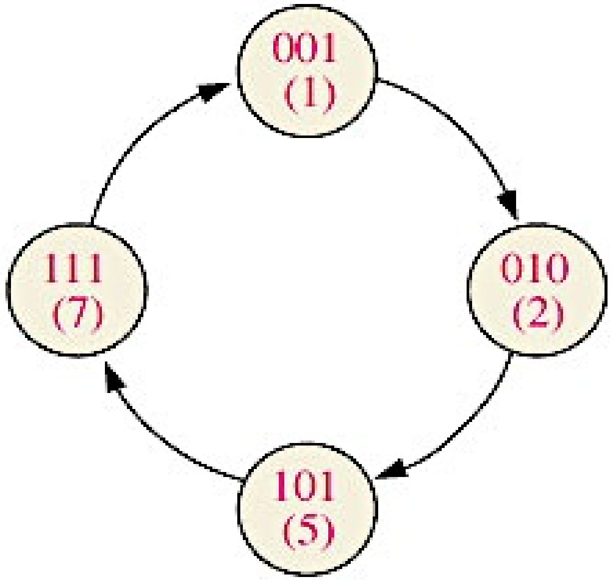
Extra

Exercise 8b.7: Design 3-bit synchronous counter that using J-K flip-flop based on the state diagram below. Show all steps clearly.



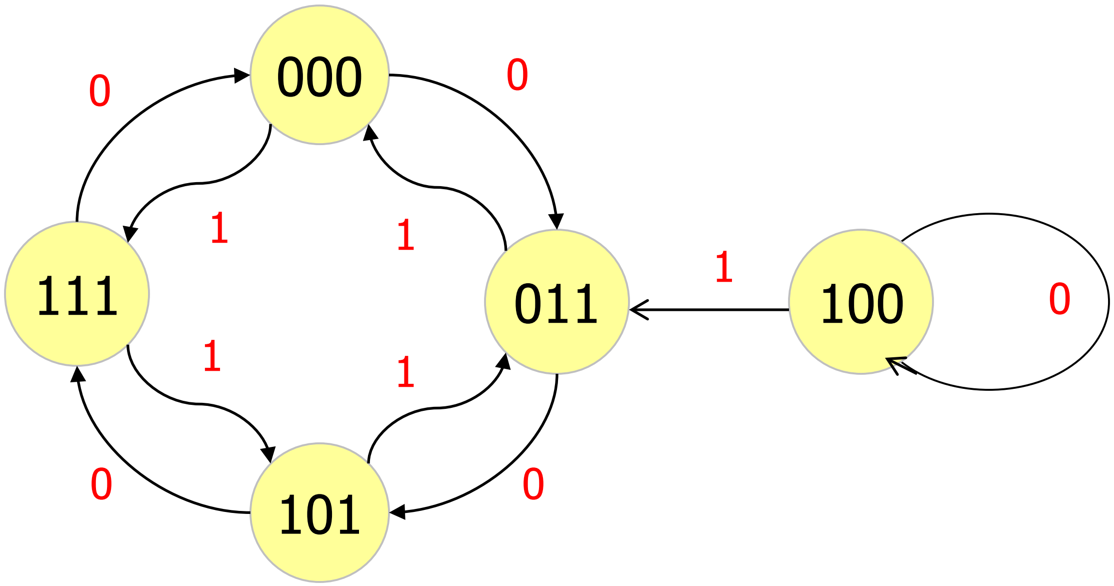
Extra

Exercise 8b.11: Design a counter with the irregular binary count sequence shown in the state diagram below using JK FF.



Extra

Exercise 8b.12: Design a synchronous counter with the irregular binary count sequence shown in the state diagram below using J-K FF.



K-maps: **Exercise 8b.12**:

Extra

XQ₂ \ Q_1Q_0	00	01	11	10
00	0	X	1	X
01	X	X	X	X
11	X	X	X	X
10	1	X	0	X

$$J_2 = X\overline{Q}_1 + \overline{X}Q_1$$

XQ_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	X
01	0	1	X	X
11	1	1	X	X
10	1	X	X	X

$$J_1 = X + \overline{Q}_2 + Q_0$$

XQ_2 \ Q_1Q_0	00	01	11	10
00	1	X	X	X
01	0	X	X	X
11	1	X	X	X
10	1	X	X	X

$$J_0 = X + \overline{Q}_2$$

XQ_2 \ Q_1Q_0	00	01	11	10
00	X	X	X	X
01	0	0	1	X
11	1	1	0	X
10	X	X	X	X

$$K_2 = X\overline{Q}_1 + \overline{X}Q_1$$

XQ_2 \ Q_1Q_0	00	01	11	10
00	X	X	1	X
01	X	X	1	X
11	X	X	1	X
10	X	X	0	X

$$K_1 = \overline{X} + Q_2$$

XQ_2 \ Q_1Q_0	00	01	11	10
00	X	X	0	X
01	X	0	1	X
11	X	0	0	X
10	X	X	0	X

$$K_0 = \overline{X}Q_2Q_1$$

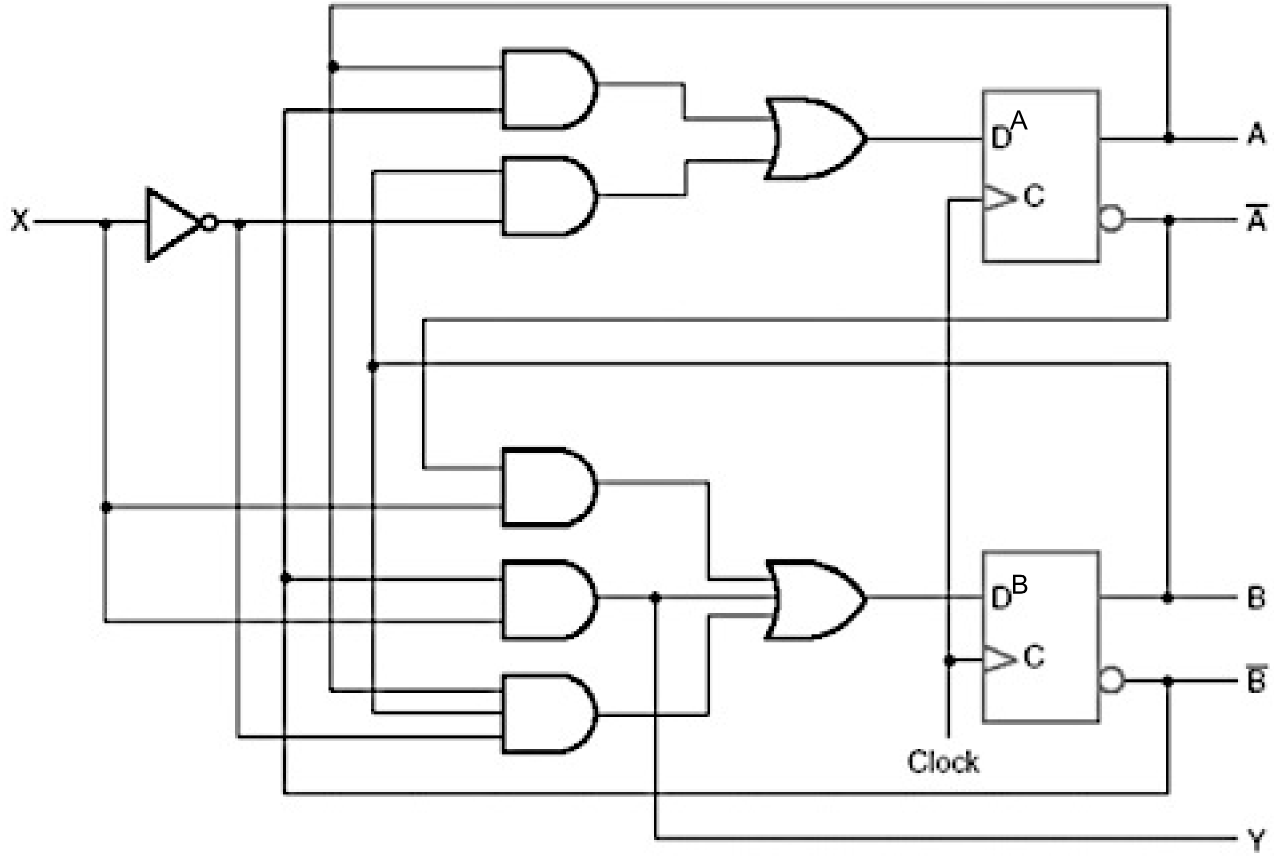
Extra

Exercise 8b.13: Two type of counters, modulus-4 and modulus-8 need to be used to achieve count up to modulus-*n* (*n* CLK).

a) How to cascade the counters to achieve count until 32 CLK (modulus-32)?
b) What is the frequency produced by each counter given an initial frequency as 800MHz?

Extra

Exercise 8b.15: Analysis for the following sequential circuit. Use Method 1. Get state diagram for the sequential



Exercise 8b.16:

Analysis for the following sequential circuit. Use Method 2. Get state diagram for the sequential circuit.

Extra