EXTRA TUTORIAL QUESTIONS FOR COMBINATIONAL LOGIC CIRCUIT DESIGN

QUESTION 1

Class for digital logic will be conducted in two rooms, which are BK1 and BK2. Student can enter either room based on the last **decimal digit (0-9)** of their student ID. The last decimal digit can be represented in 4-bit binary as $\mathbf{b_3b_2b_1b_0}$.

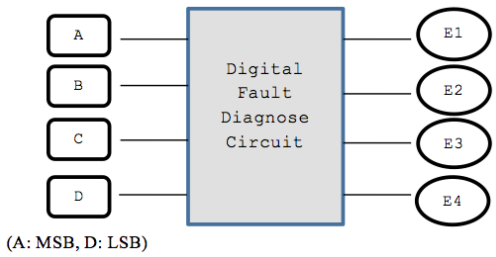
The rules of entering BK1 or BK2 will be determined by the following:

1. Student who can enter BK1 is a student whose last decimal digit ID is **even** and bit b_2 **not equal** to bit b_1.
2. Student who can enter BK2 is a student whose last decimal digit ID is **odd** and bit b_2 **equals** to bit b_1.
3. Other students **are not allowed** to enter BK1 and BK2.

Design a circuit so that by entering the last digit of student ID in binary, the output will lit the LED in front of the room that the students supposed to enter. Draw the final circuit using NAND gates only.

QUESTION 2

A new digital fault diagnoses circuit is requested to be designed for analyzing four bit 2's complement input binary number from sensors A, B, C, and D. Sensor A represents input MSB and sensor D represents input LSB. As shown in the following Figure 4, bit pattern analysis from input sensors A, B, C, and D will trigger four different output errors (active HIGH) of type E1, E2, E3, and E4.



The following rules are used to activate the error's signal type:

RULE 1: *E1 is activated if the input number is positive ODD and the majority of the bits is '0'.*

RULE 2: *E2 is activated if the input number is positive EVEN and the majority of the bits is '0'.*

RULE 3: *E3 is activated if the input number is negative ODD and the majority of the bits is '1'.*

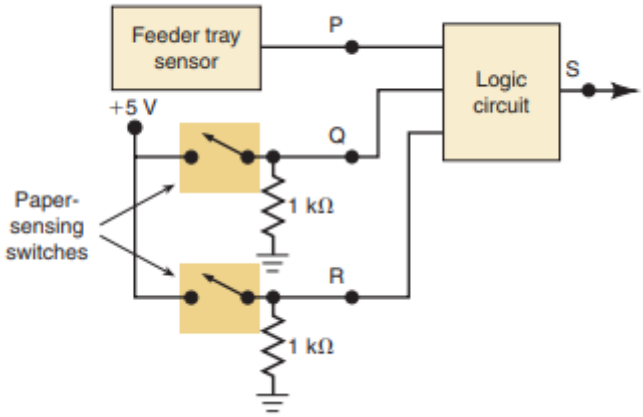
RULE 4: *E4 is activated if the input number is negative EVEN and the majority of the bits is '1'.*

RULE 5: *The output of error signal is invalid if the input has equal bit '0' and bit '1'.*

Design the new digital fault diagnoses circuit by using universal gate NAND only. Draw the final circuit design.

(Note: Positive ODD is positive numbers that are odd and negative EVEN is negative numbers that are even).

QUESTION 3



In a simple copy machine, a stop signal, S, is to be generated to stop the machine operation and energize an indicator light whenever either of the following conditions exists: (1) there is no paper in the paper feeder tray; or (2) the two microswitches in the paper path are activated, indicating a jam in the paper path. The presence of paper in the feeder tray is indicated by a HIGH at logic signal P. Each of the microswitches produces a logic signal (Q and R) that goes HIGH whenever paper is passing over the switch to activate it. Design the logic circuit to produce a HIGH at output signal S for the stated conditions, and implement it using the 74HC00 CMOS quad two-input NAND chip.

QUESTION 4

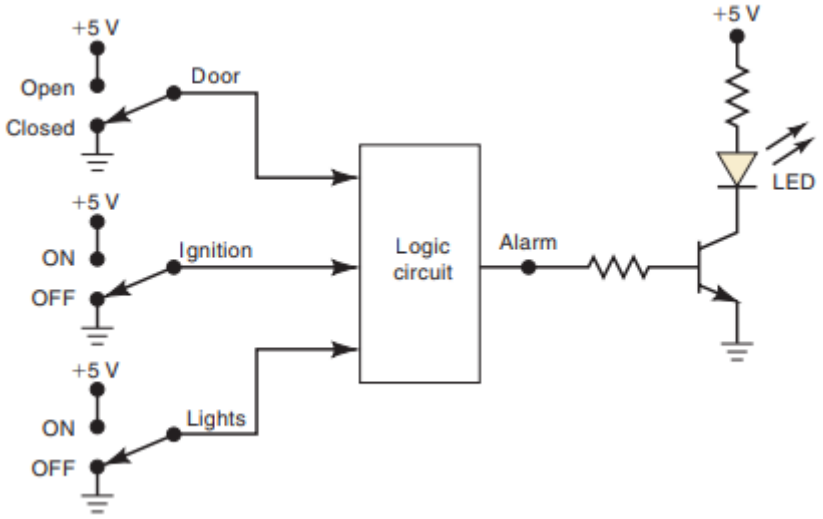


Figure above shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used D D 15 V 15 V Door Ignition 15 V LED Open Closed ON OFF 15 V Lights ON OFF Logic circuit Alarm Figure 4-69 Problem 4-8. to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

■ The headlights are on while the ignition is off.
■ The door is open while the ignition is on.

QUESTION 5

A museum has three rooms, each with a motion sensor (m0, m1, and m2) that outputs 1 when motion is detected. At night, the only person in the museum is one security guard who walks from room to room. Using the combinational design process, create a circuit that sounds an alarm (by setting an out A to 1) if motion is ever detected in more than one room at a time (i.e., in two or three rooms), meaning there must be an intruder(s) in the museum.

QUESTION 6

A paint manufacturer has two tanks with Blue and Red paint. The supervisor would like to monitor the tanks volume such that the system will trigger an alarm when both or any of the tanks volume drops to a level lower than one-quarter full. Level sensors of both tanks will produce a logic LOW if the volume drops below one-quarter full. Alarm will be triggered by a logic HIGH. Draw the complete system, showing the two tanks connected to both gates.

QUESTION 7

Design a combinational logic circuit that calculates the sum of 4 inputs A, B, C and D. The outputs are X and Y, where the maximum number is 3.

QUESTION 8

Design a combinational logic circuit that multiplies 2-bits binary number, AB with another 2-bits binary number CD. The output is 3 bits, XYZ.

QUESTION 9

A four-bit binary number is represented as $A_3A_2A_1A_0$, where A_3, A_2, A_1, and A_0 represent the individual bits and A_0 is equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000.

QUESTION 10

Design a combinational circuit that will produce low signal when the three input bit values produce even parity.