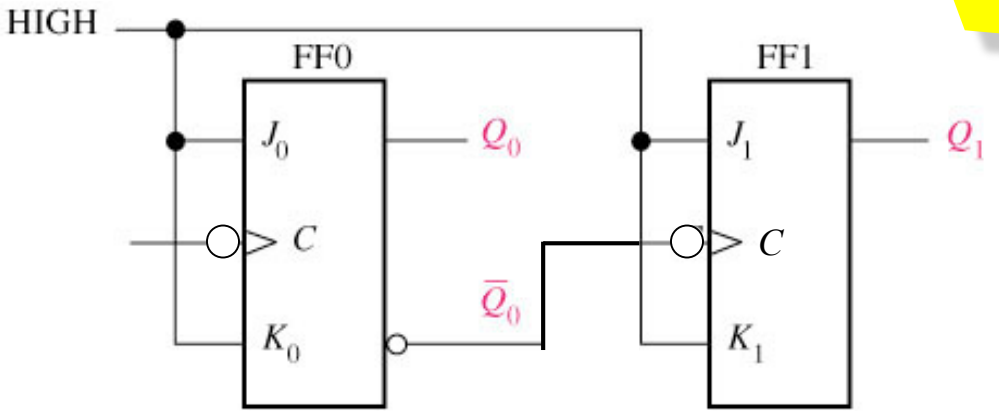
Extra

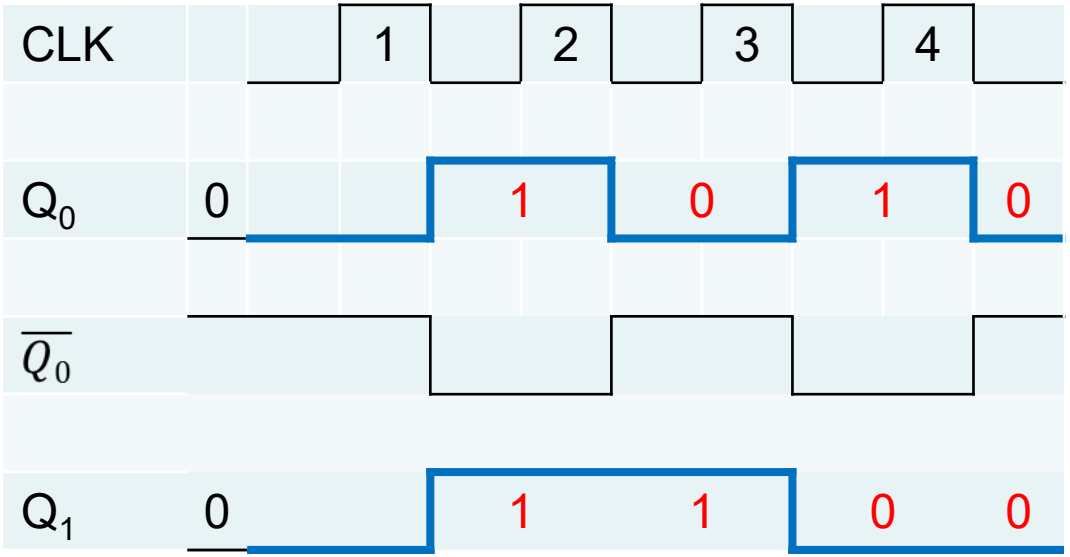
Exercise 8a.2: A 2-bit count down ripple counter is designed using J-K flip-flop with negative edge triggered clock.

a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 4 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.

Solution 8a.2: a) Draw the connection of logic symbol.



b) Draw the waveform outputs for 4 clock cycles.

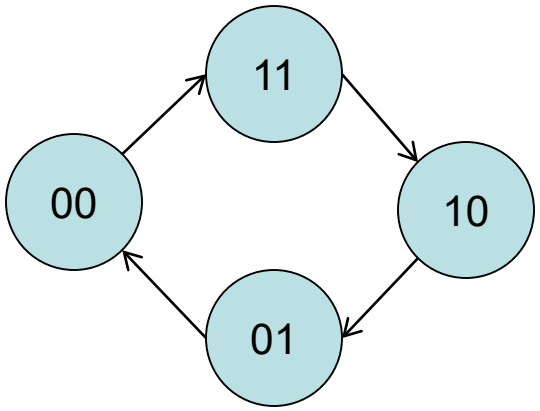


Extra

c) Construct a state table for the counter.

Clock Pulse	Q_1	Q_0
Initial	0	0
1	1	1
2	1	0
3	0	1
4	0	0

d) Draw the state diagram the the counter.



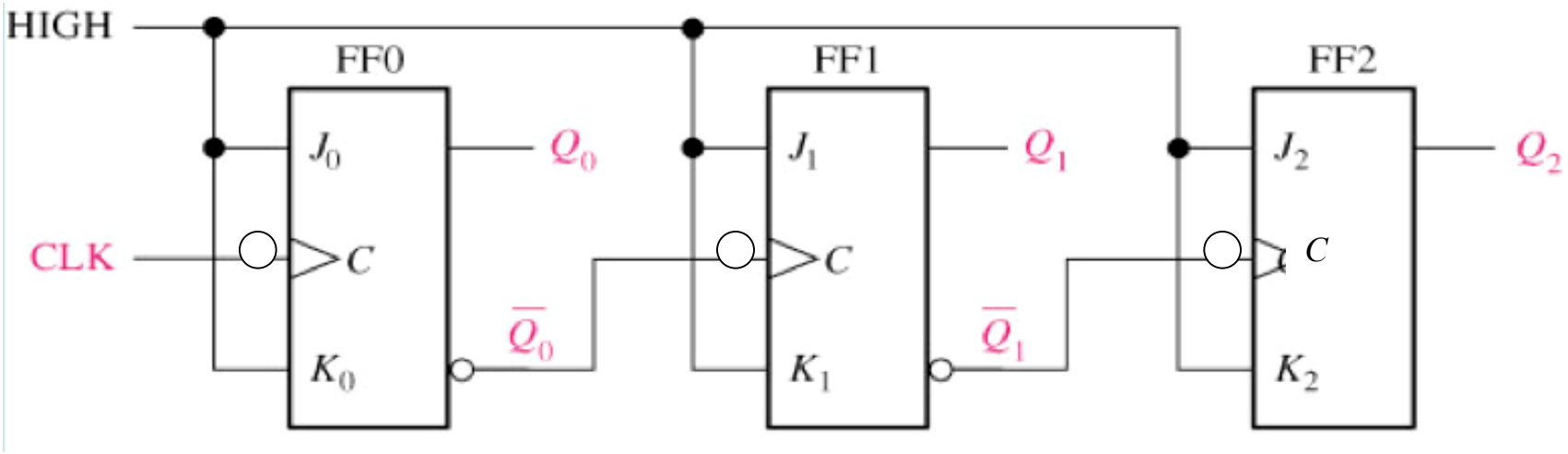
Extra

Exercise 8a.3: A 3-bit count down ripple counter is designed using J-K flip-flop with negative edge triggered clock.

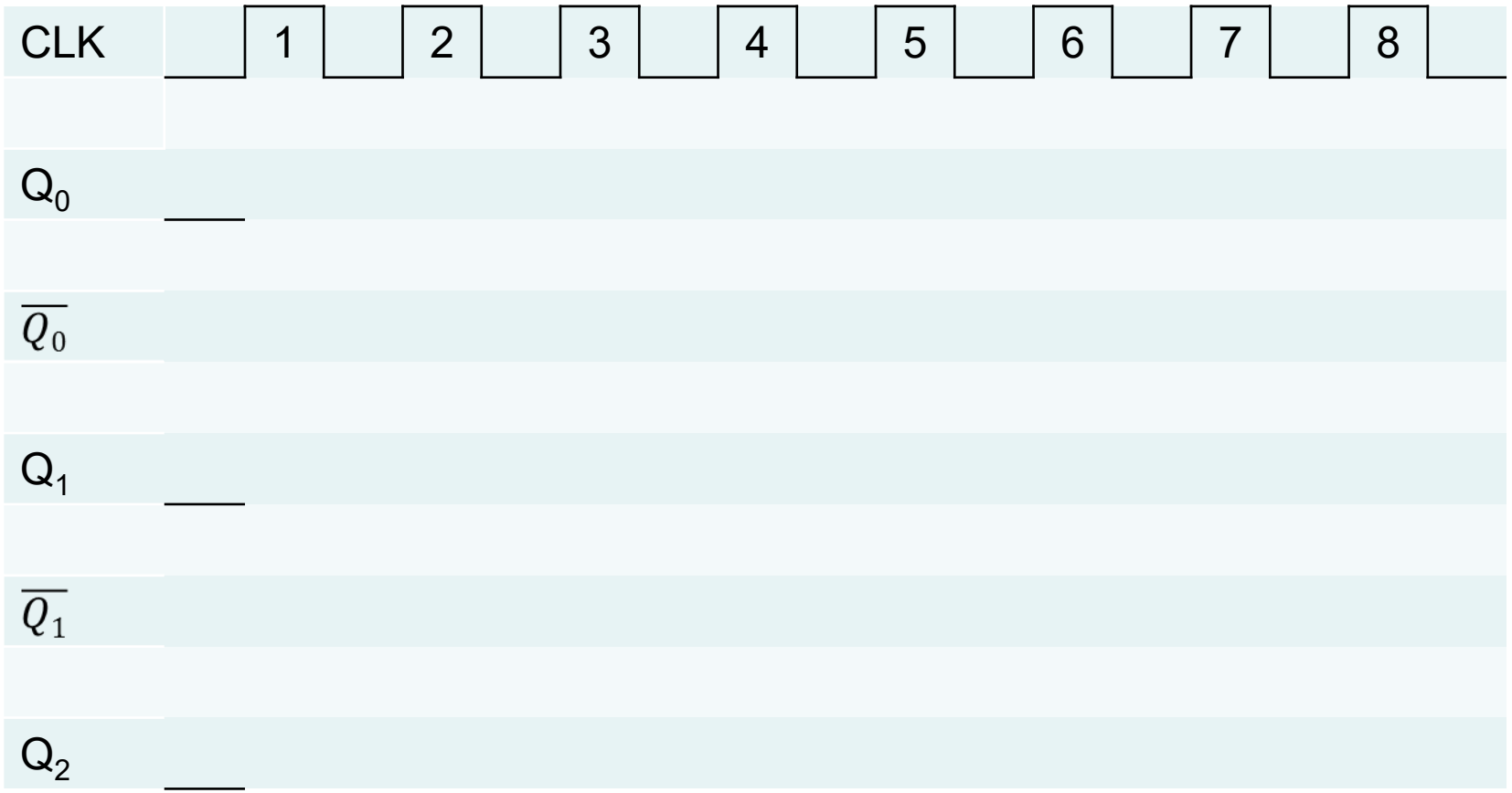
a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 8 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.

Extra

Solution 8a.3: a) Draw the connection of logic symbol.

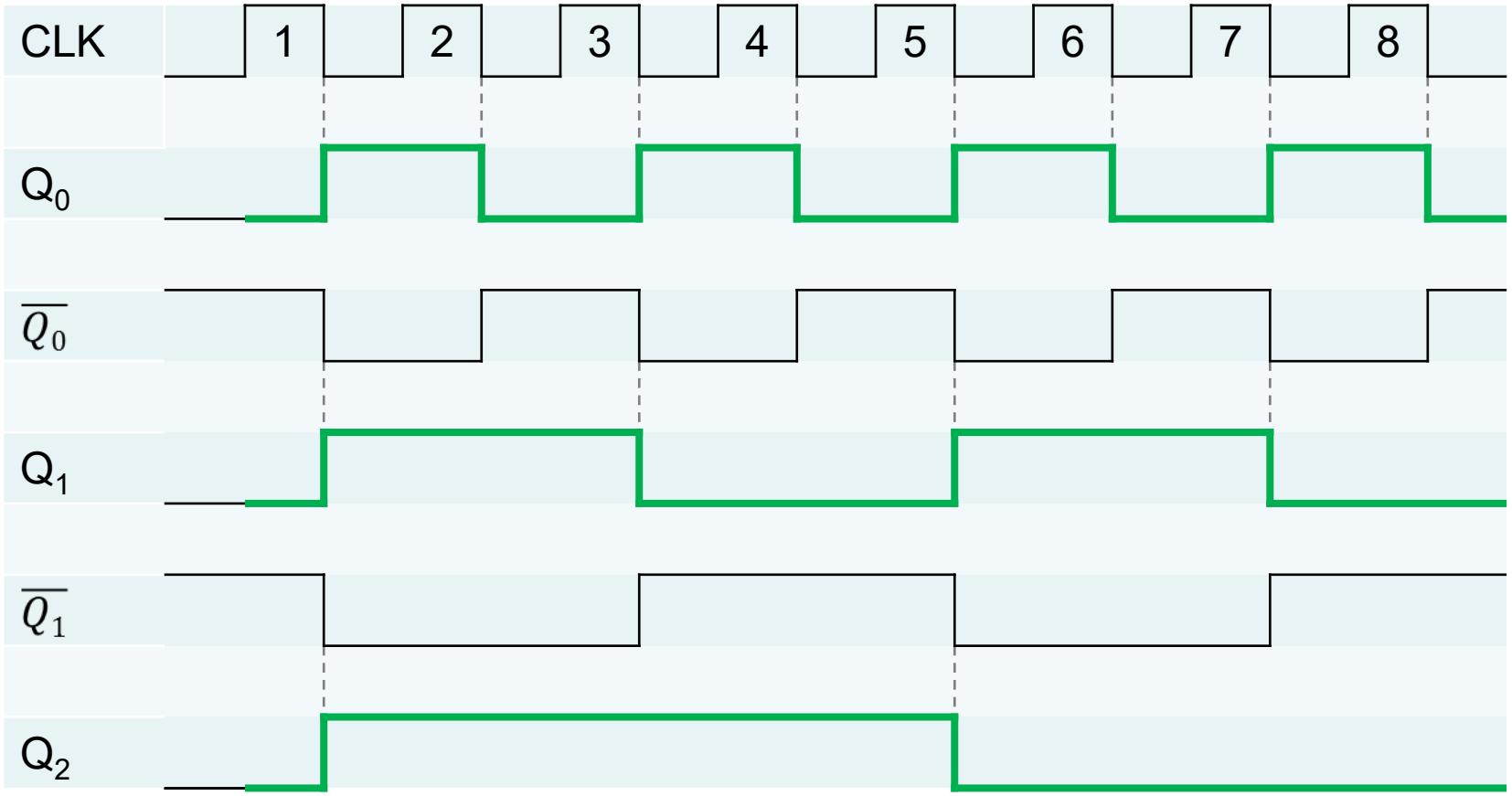


Extra



b) Draw the waveform outputs for 8 clock cycles.

Extra

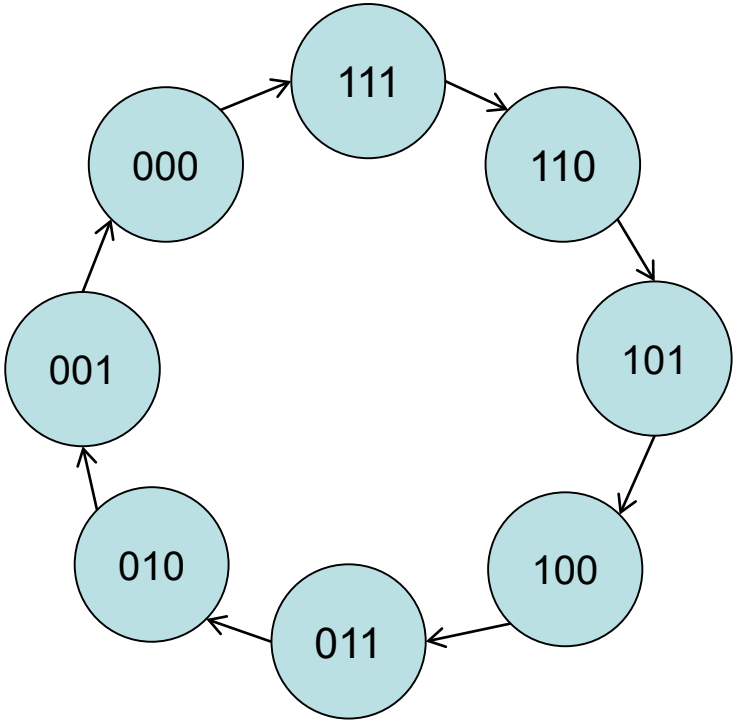


c) Construct a state table for the counter.

Extra

Clock Pulse	Q_2	Q_1	Q_0
Initial	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0

d) Draw the state diagram the counter



Extra

Exercise 8a.4: A 4-bit count down ripple counter is designed using J-K flip-flop with positive edge triggered clock.

a) Draw the connection of logic symbol.
b) Draw the waveform outputs for 8 clock cycles.
c) Construct a state table for the counter.
d) Draw the state diagram the the counter.