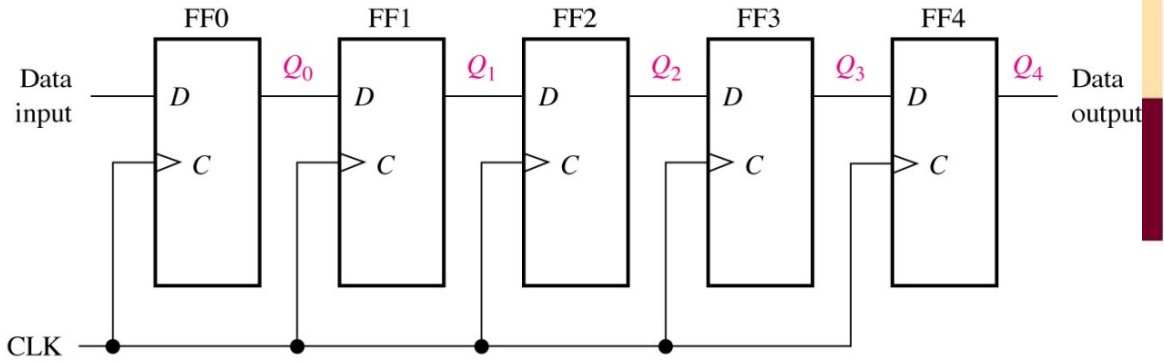


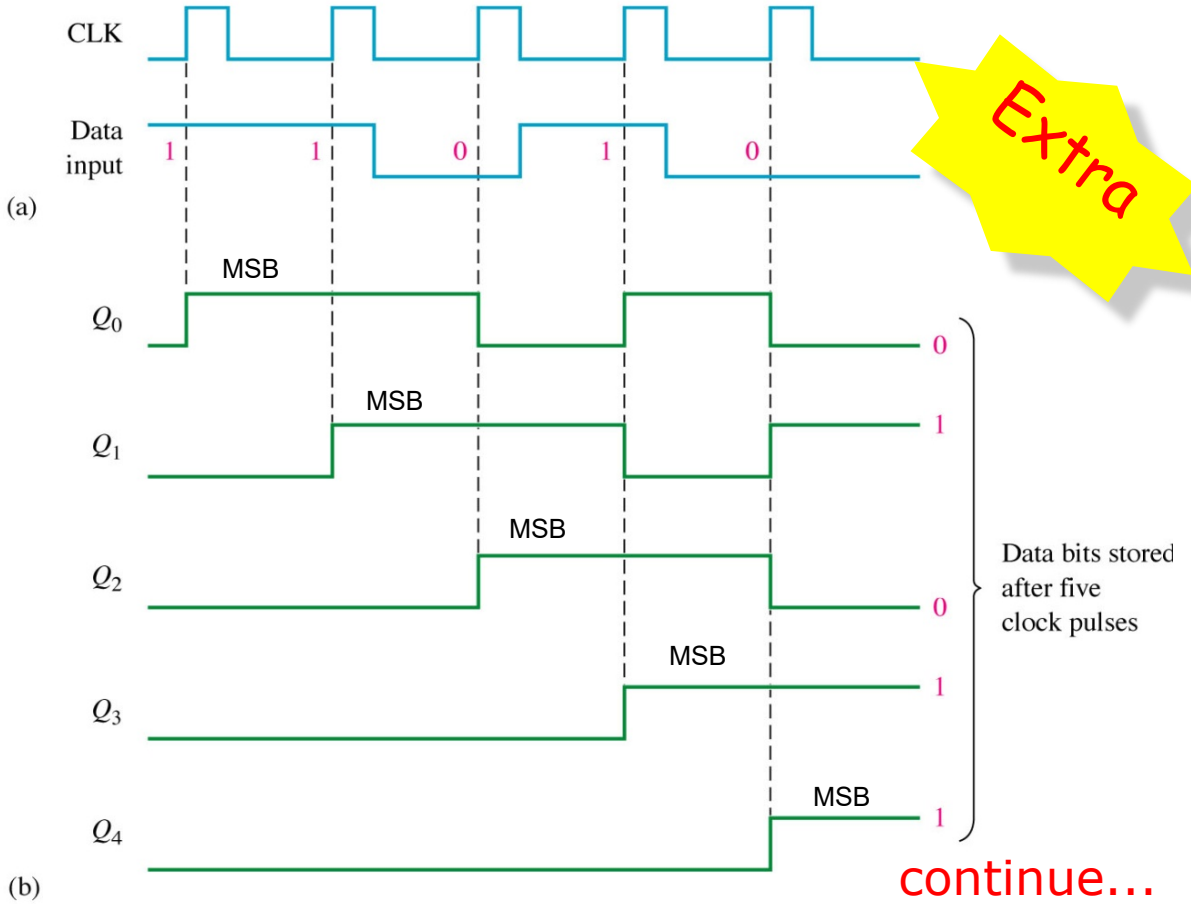
Example 3:

5-bit SISO (Right SR)

Data input: 11010

Initially all FFs are cleared.

MSB are shifted in first.

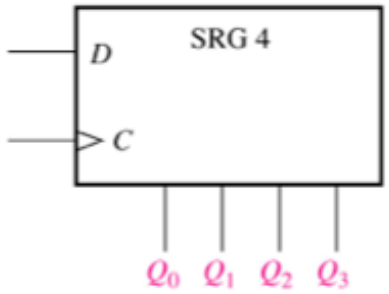


Extra

continue...

Clock, t	FF0	FF1	FF2	FF3	FF4
Initially	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	0	1	1	0	0
4	1	0	1	1	0
5	0	1	0	1	1

Example 4: Show the states of 4-bit SIPO shift register (SRG 4) for the data input **0110 (MSB shifted first)** and clock waveforms. The register initially all is 1s.

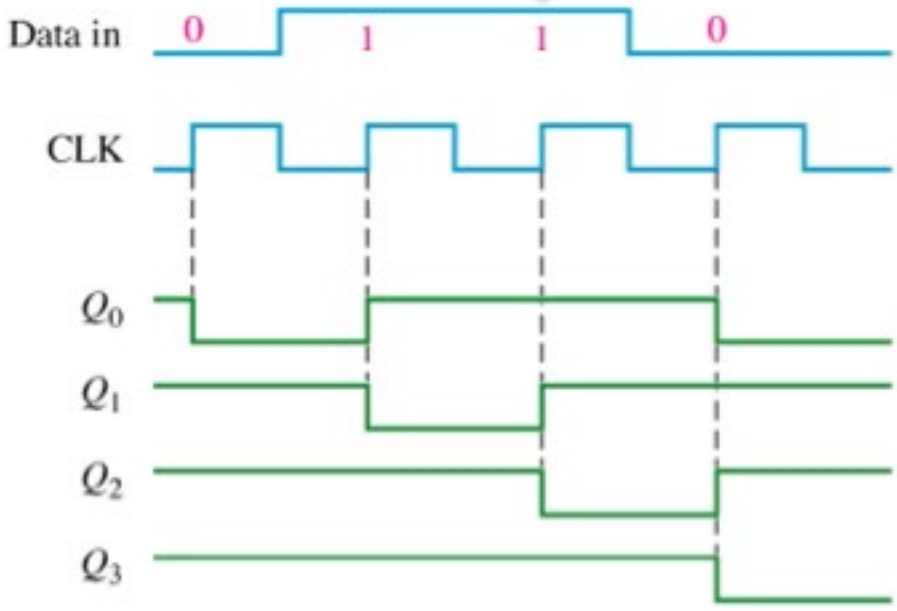


Clock, t	FF0	FF1	FF2	FF3
Initially	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	1	1	0	1
4	0	1	1	0

Q_0 Q_1 Q_2 Q_3

Extra

(a)



(b)

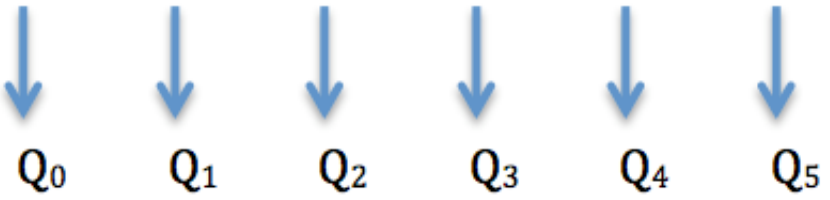
Extra

Exercise 9.1: Show the states of 6-bit SIPO shift register (SRG 6) for the data input **011001** and clock waveforms.

The register initially all is 0s and MSB will enter first.

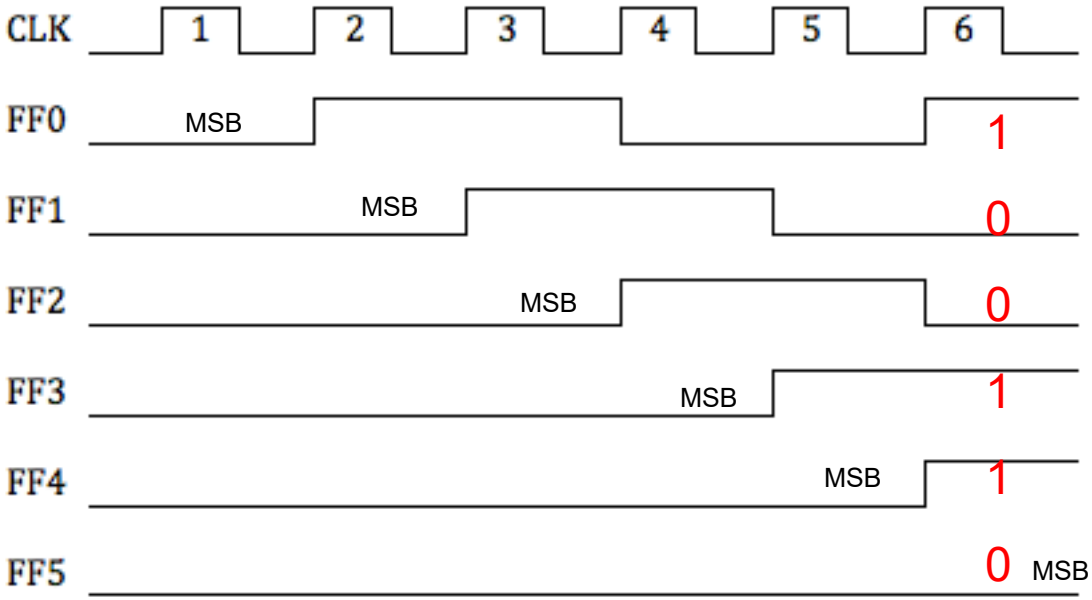
Solution :

Clock, t	FF0	FF1	FF2	FF3	FF4	FF5
Initially	0	0	0	0	0	0
1	0	0	0	0	0	0
2	1	0	0	0	0	0
3	1	1	0	0	0	0
4	0	1	1	0	0	0
5	0	0	1	1	0	0
6	1	0	0	1	1	0



Extra

Clock, t	FF0	FF1	FF2	FF3	FF4	FF5
Initially	0	0	0	0	0	0
1	0	0	0	0	0	0
2	1	0	0	0	0	0
3	1	1	0	0	0	0
4	0	1	1	0	0	0
5	0	0	1	1	0	0
6	1	0	0	1	1	0



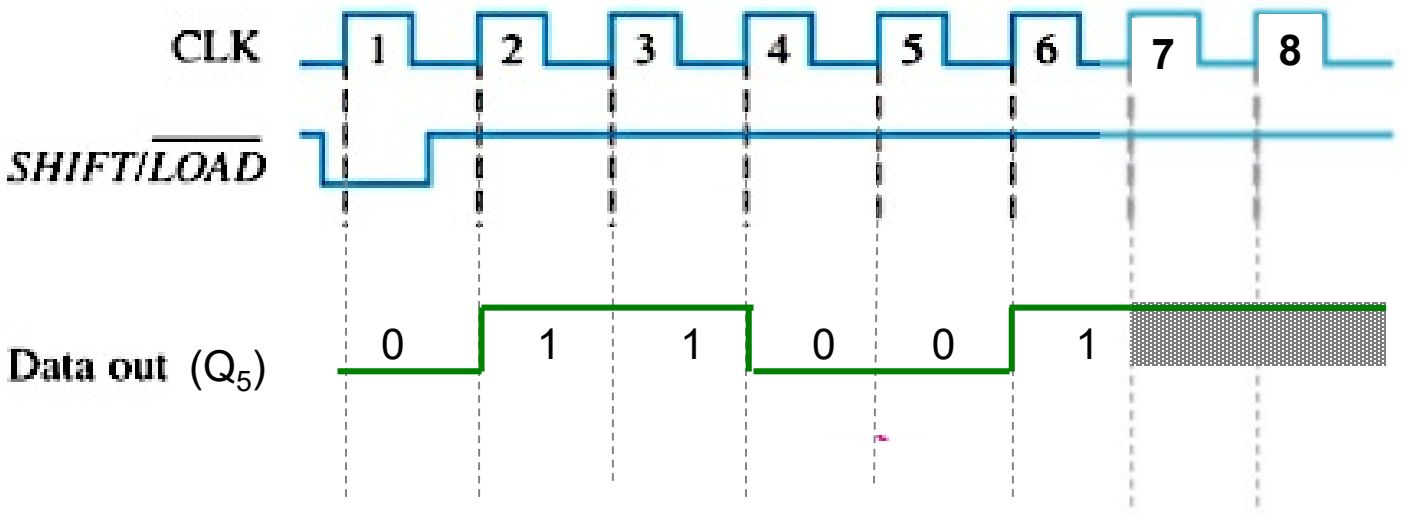
Self-Test:

Generate a table for the data shifting out.

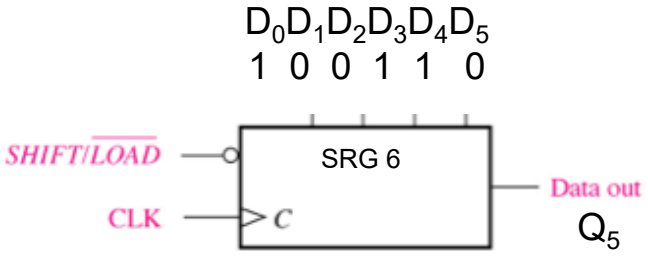
Exercise 9.4: Complete the timing diagram of 6–bit PISO shift register (SRG 6) for the data input 011001 (MSB shifted first).

The register initially all is 0s.

Extra



Solution:



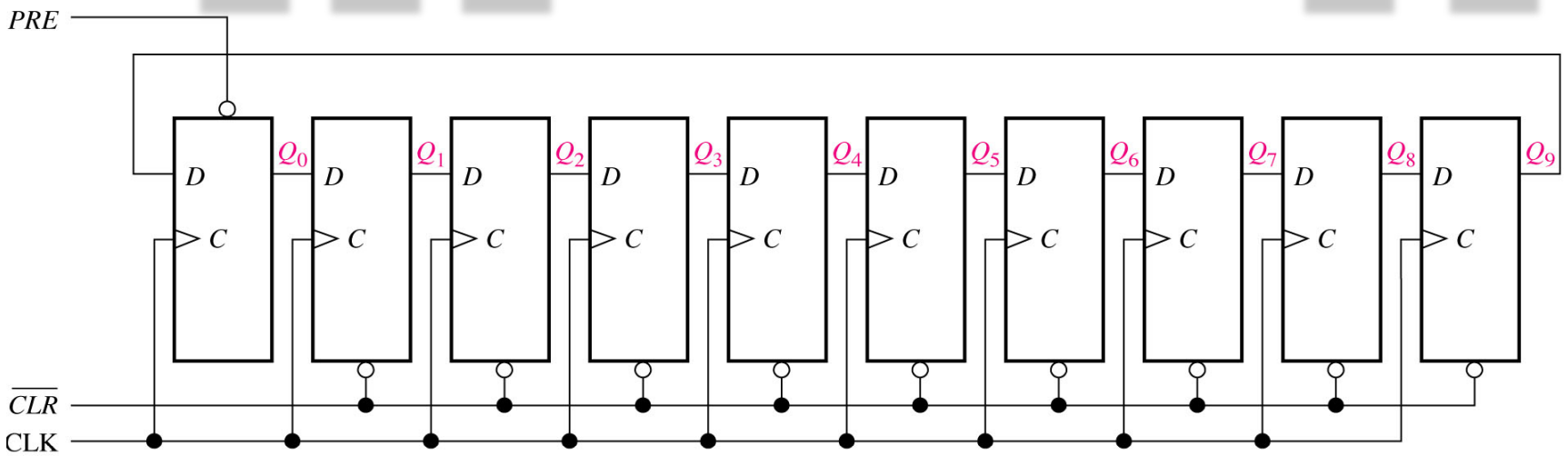
Example 7: If a 10-bit ring counter has the initial state 0000000101, determine the waveform for each of the Q outputs.

Extra

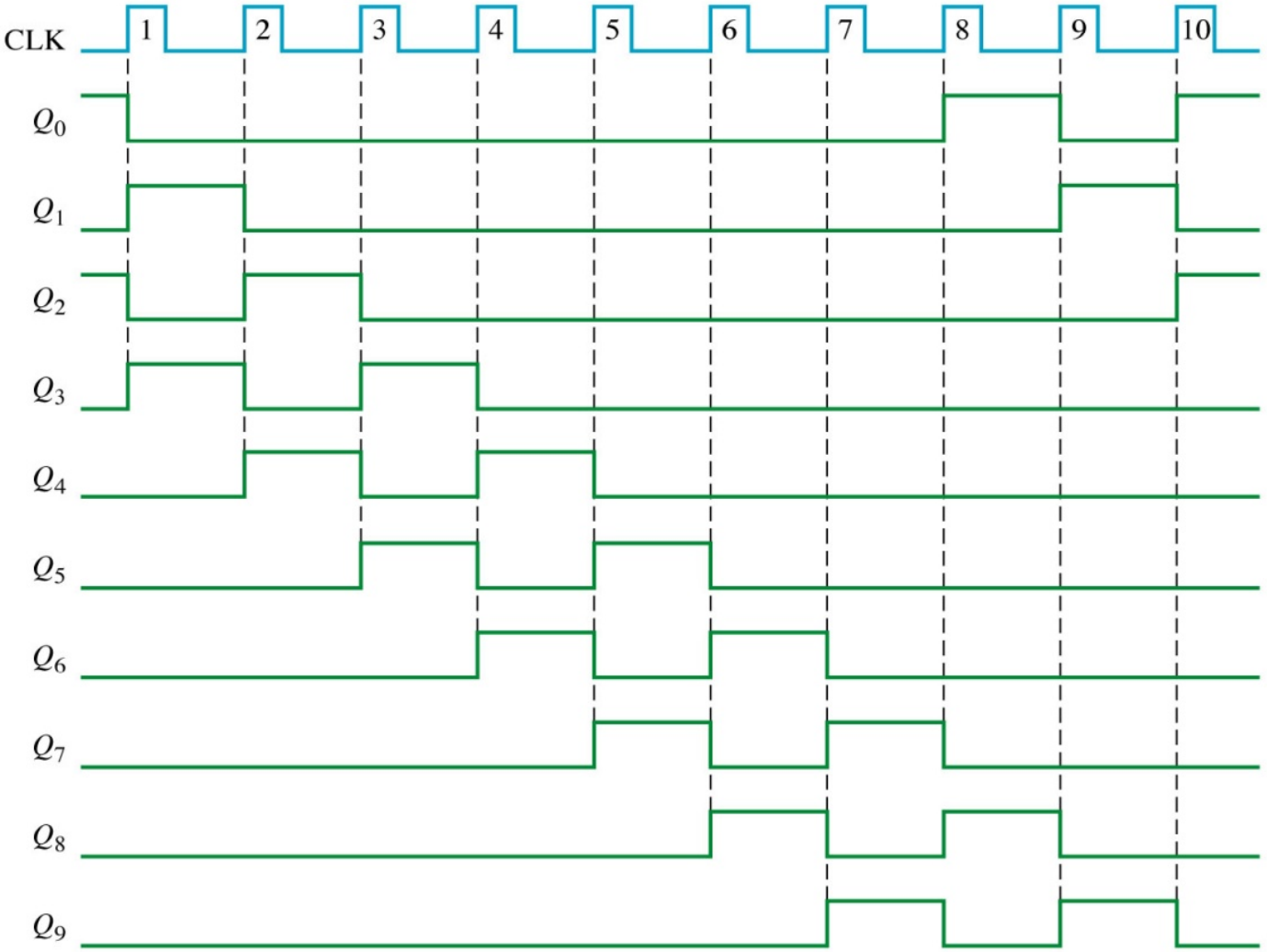
Solution:

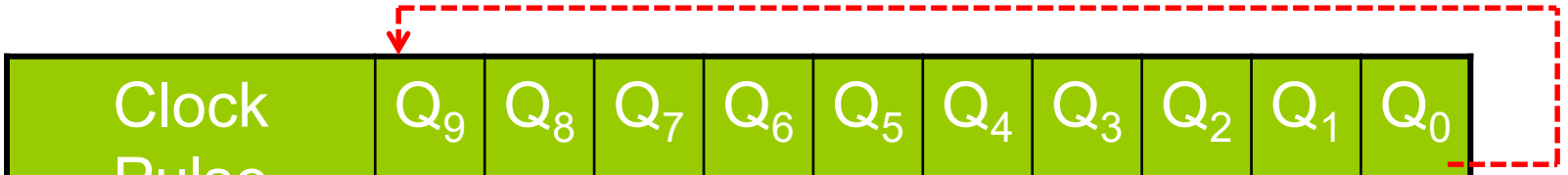
	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
MSB	0	0	0	0	0	0	0	1	0	1	LSB

D_0 1 D_1 0 D_2 1 . . . . . D_8 0 D_9 0



Extra





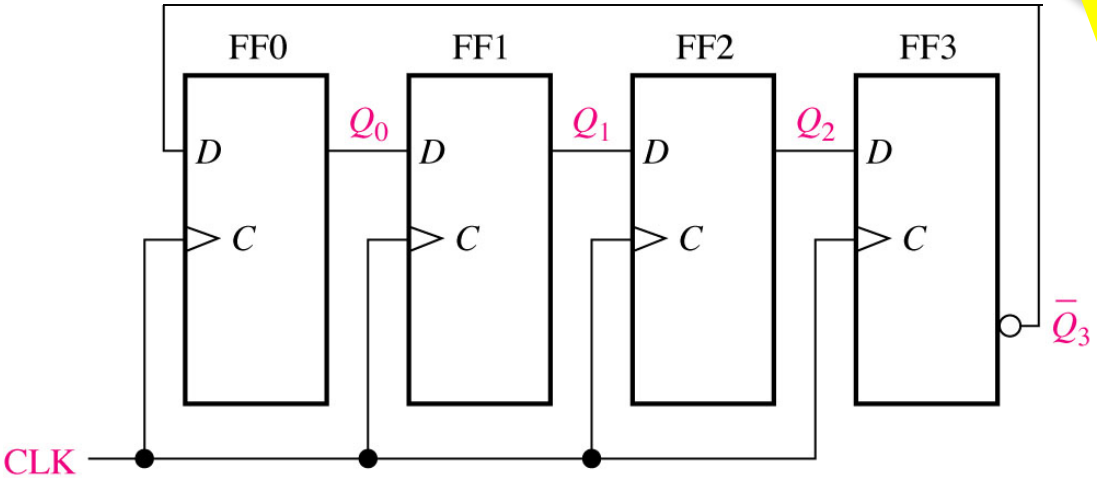
Clock Pulse	Q_9	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	1	0	1
1	1	0	0	0	0	0	0	0	1	0
2	0	1	0	0	0	0	0	0	0	1
3	1	0	1	0	0	0	0	0	0	0
4	0	1	0	1	0	0	0	0	0	0
5	0	0	1	0	1	0	0	0	0	0
6	0	0	0	1	0	1	0	0	0	0
7	0	0	0	0	1	0	1	0	0	0
8	0	0	0	0	0	1	0	1	0	0
9	0	0	0	0	0	0	1	0	1	0
10	0	0	0	0	0	0	0	1	0	1

Extra

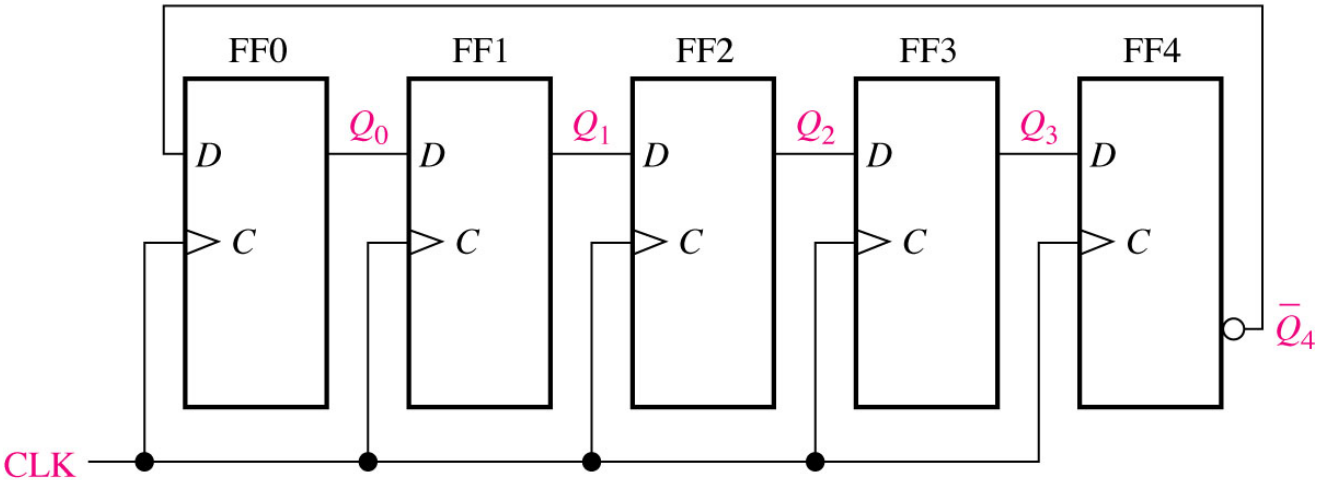
n-bit = MOD 2*n*
(state number)

Example:

- For a 4-bit ring counter, there are 4 FFs which make a MOD 8 counter.
- It will recycle after 8 clock cycles.



(a) Four-bit Johnson counter



(b) Five-bit Johnson counter

continue...

Example:

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	.	.	.	.

$\overline{Q}_3$

Extra

Complete one cycle

Repeat cycle

Extra

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0
9	.	.	.	.

Complete one cycle

Repeat cycle