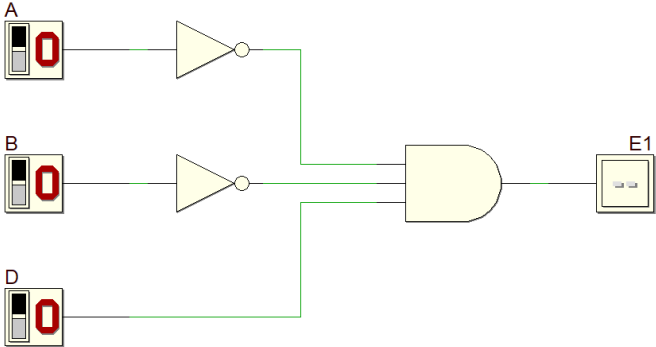
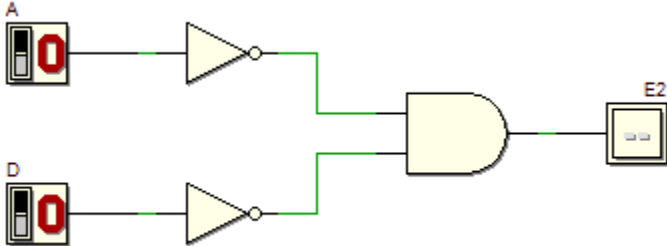


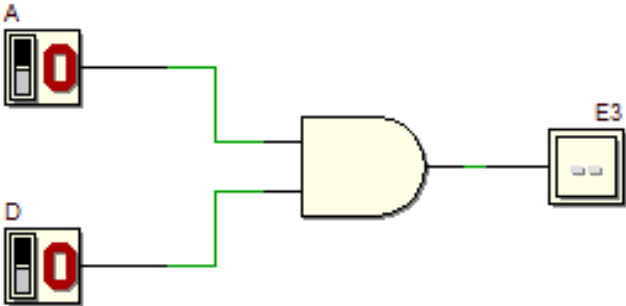
DIGITAL LOGIC LAB 2 (1-SECP)



E1

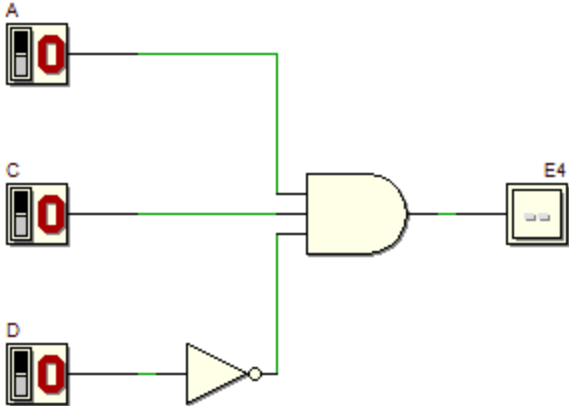


E2



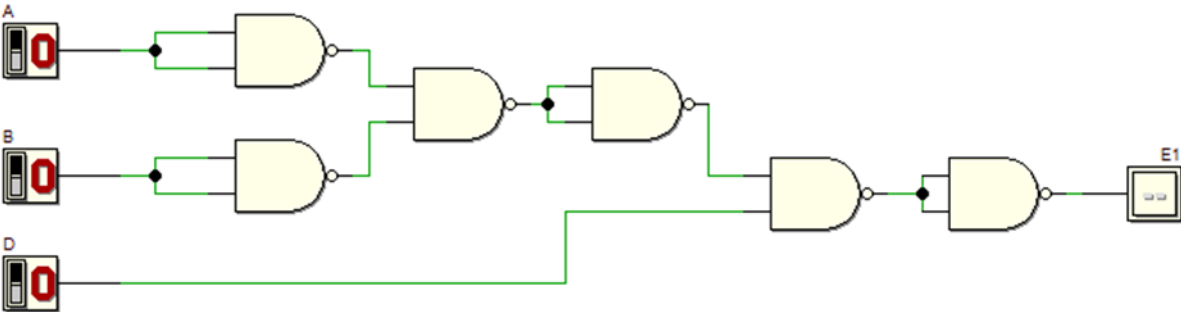
E3

DIGITAL LOGIC LAB 2 (1-SECP)

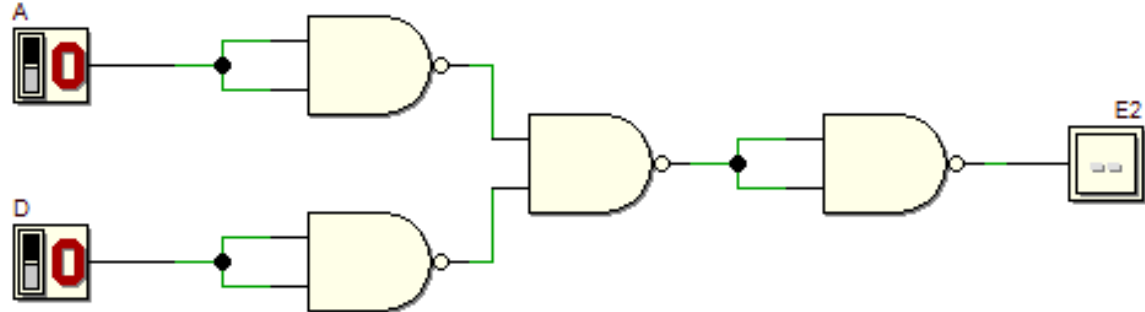


E4

NAND E1

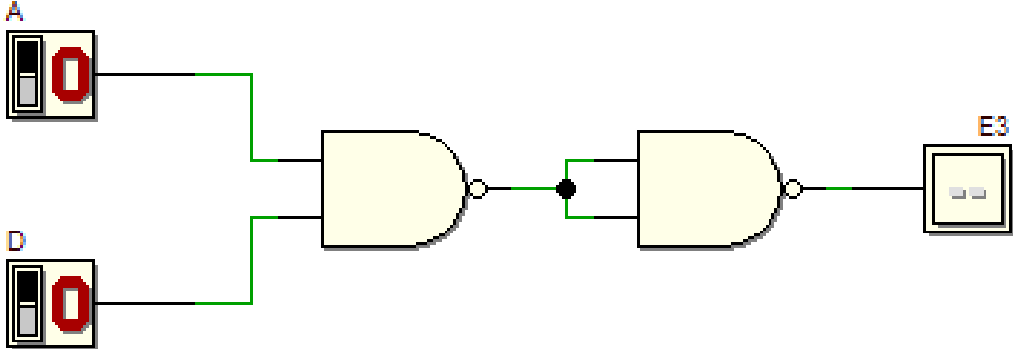


NAND E2

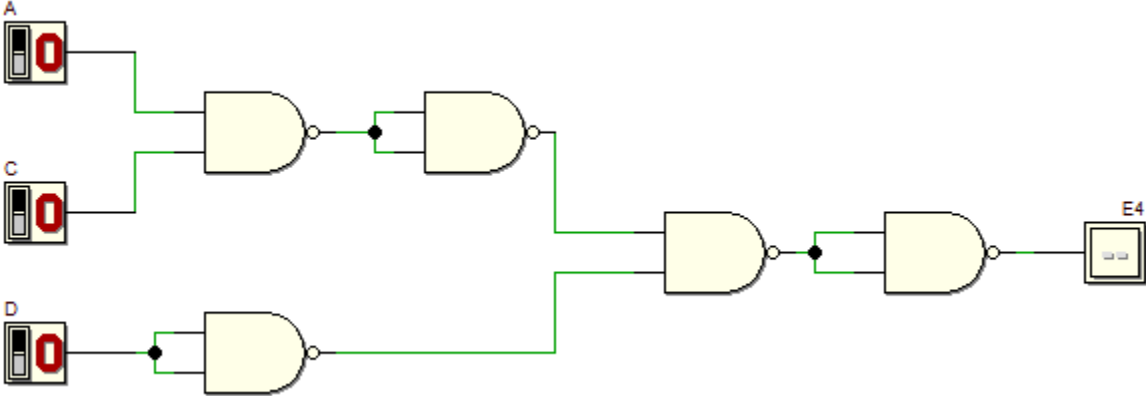


DIGITAL LOGIC LAB 2 (1-SECP)

NAND E3

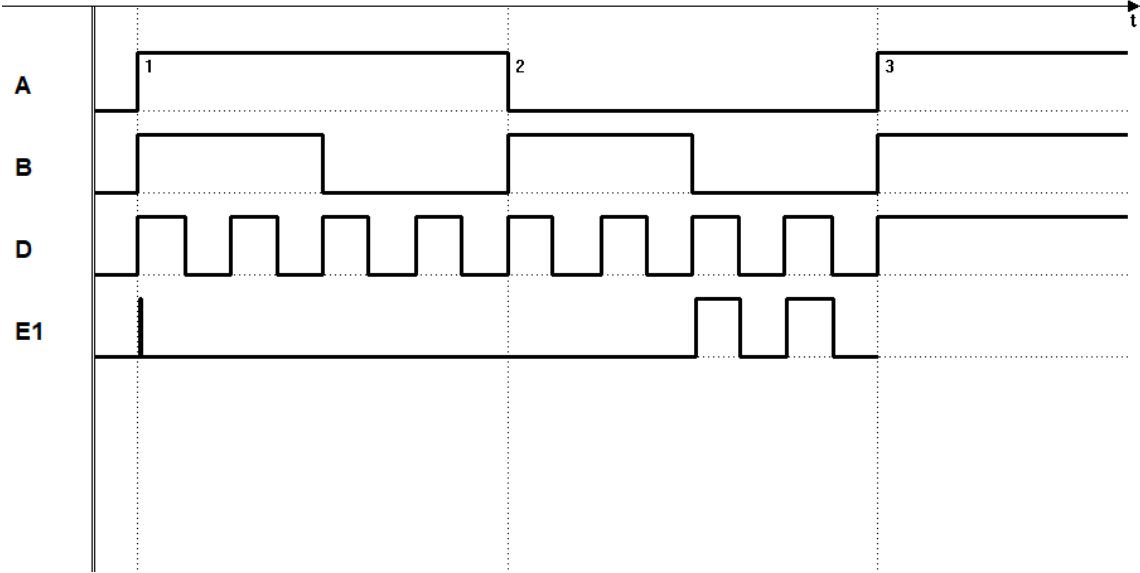


NAND E4

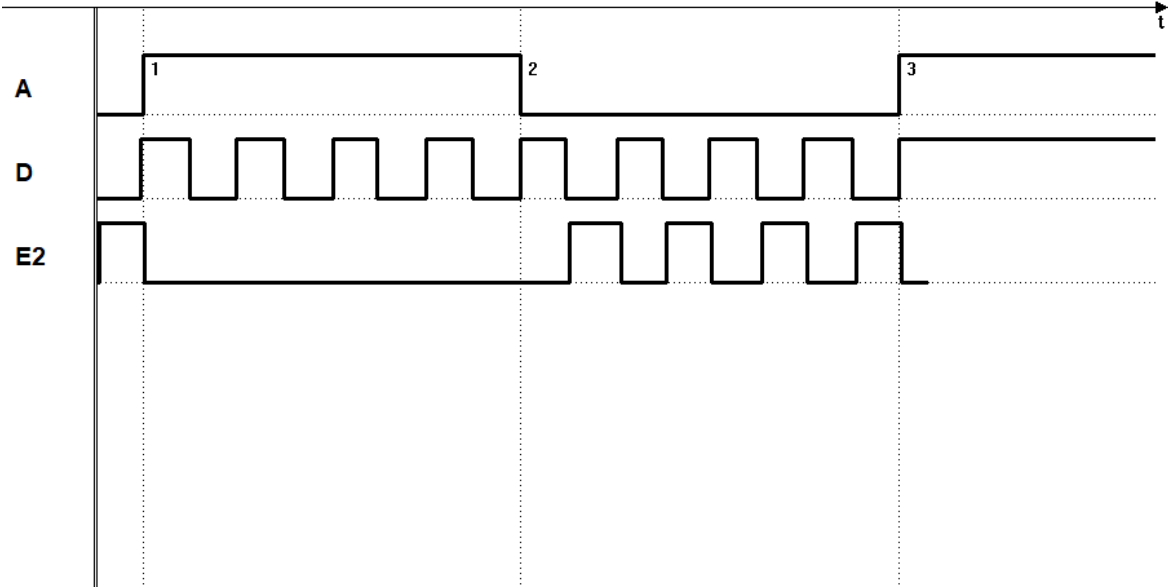


DIGITAL LOGIC LAB 2 (1-SECP)

TIMING DIAGRAM E1

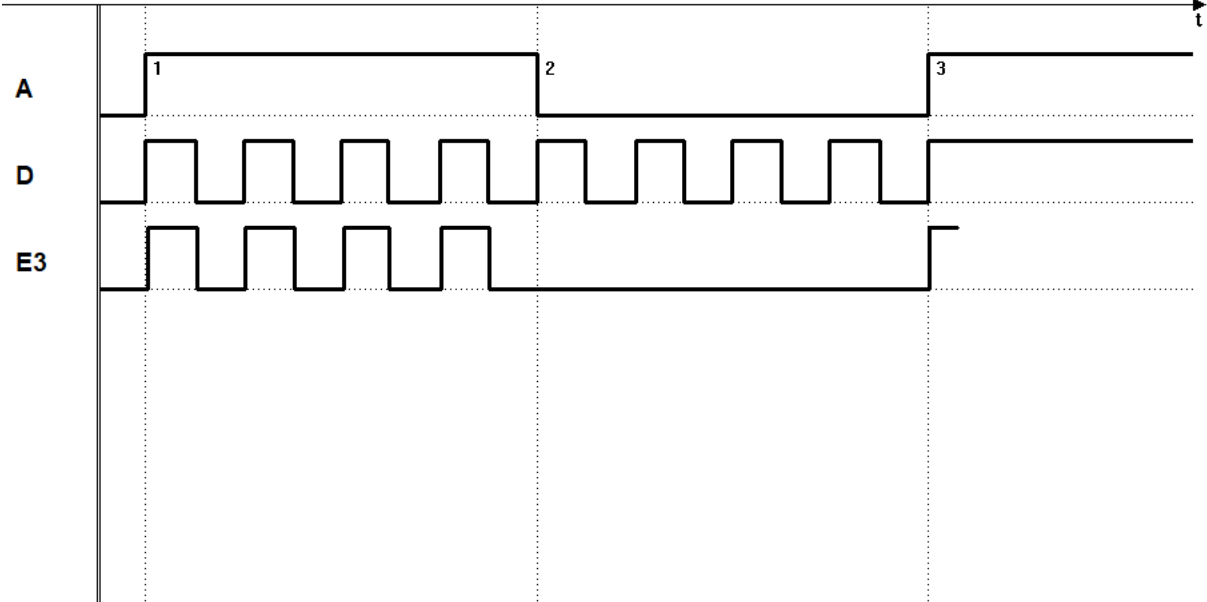


TIMING DIAGRAM E2



DIGITAL LOGIC LAB 2 (1-SECP)

TIMING DIAGRAM E3



TIMING DIAGRAM E4

